Optical Image Stabilization (OIS) / Open-Auto Focus (AF) Controller & Driver integrating an on-chip 32-bit DSP

LC898124EP3XC

WLCSP27, 3.89x1.30, 0.4P
CASE 567NJ
SCALE 4:1

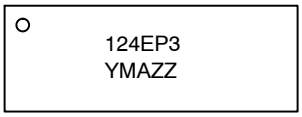
OVERVIEW

LC898124EP3XC is a system LSI integrating an onchip 32−bit DSP, an EEPROM and peripherals including analog circuits for OIS (Optical Image Stabilization) / Open−AF (Auto Focus) control and constant current drivers.

FEATURES

- On−chip 32−bit DSP
  - Built−in software for digital servo filter
  - Built−in software for Gyro filter
- Memory
  - EEPROM
  - ROM
  - SRAM
- Peripherals
  - AD converter: Input 4−ch
  - DA converter: Output 2−ch
  - 2−wire Serial I/F circuit (with clock stretch function)
  - Hall Bias circuit x2−ch
  - Hall Amp x2−ch
  - OSC (Oscillator)
  - LDO (Low Drop−Out regulator)
  - Digital Gyro I/F for various types of gyro (SPI Bus)
  - Interrupt I/F
- Driver
  - OIS
    Constant current linear driver (x2−ch, I_{full} = 200 mA)
  - OP−AF (bidirection)
    Constant current linear driver (x1−ch, I_{full} = 130 mA)
- Package
  - WLCSP27 (3.89 mm x 1.30 mm), thickness Max. 0.33 mm, with back coat
  - Pb−Free and Halogen Free compliance
- Power Supply Voltage
  - AD / DA / VGA / LDO / OSC: AVDD30 = 2.6 V to 3.3 V
  - Driver: VM = 1.8 V to 3.3 V
  - 1.8 V I/O: IOVDD = 1.7 V to 3.3 V
  - Core Logic: Generated by on−chip LDO DVDD15 = typ. 1.59 V
- This Device is Pb−Free and Halogen Free

MARKING DIAGRAM



Y = Year
M = Month
A = Assembly Site
ZZ = Lot Number

ORDERING INFORMATION

Device	Package	Shipping†
LC898124EP3XC−MH	WLCSP27 (Pb−Free / Halogen Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

BLOCK DIAGRAM

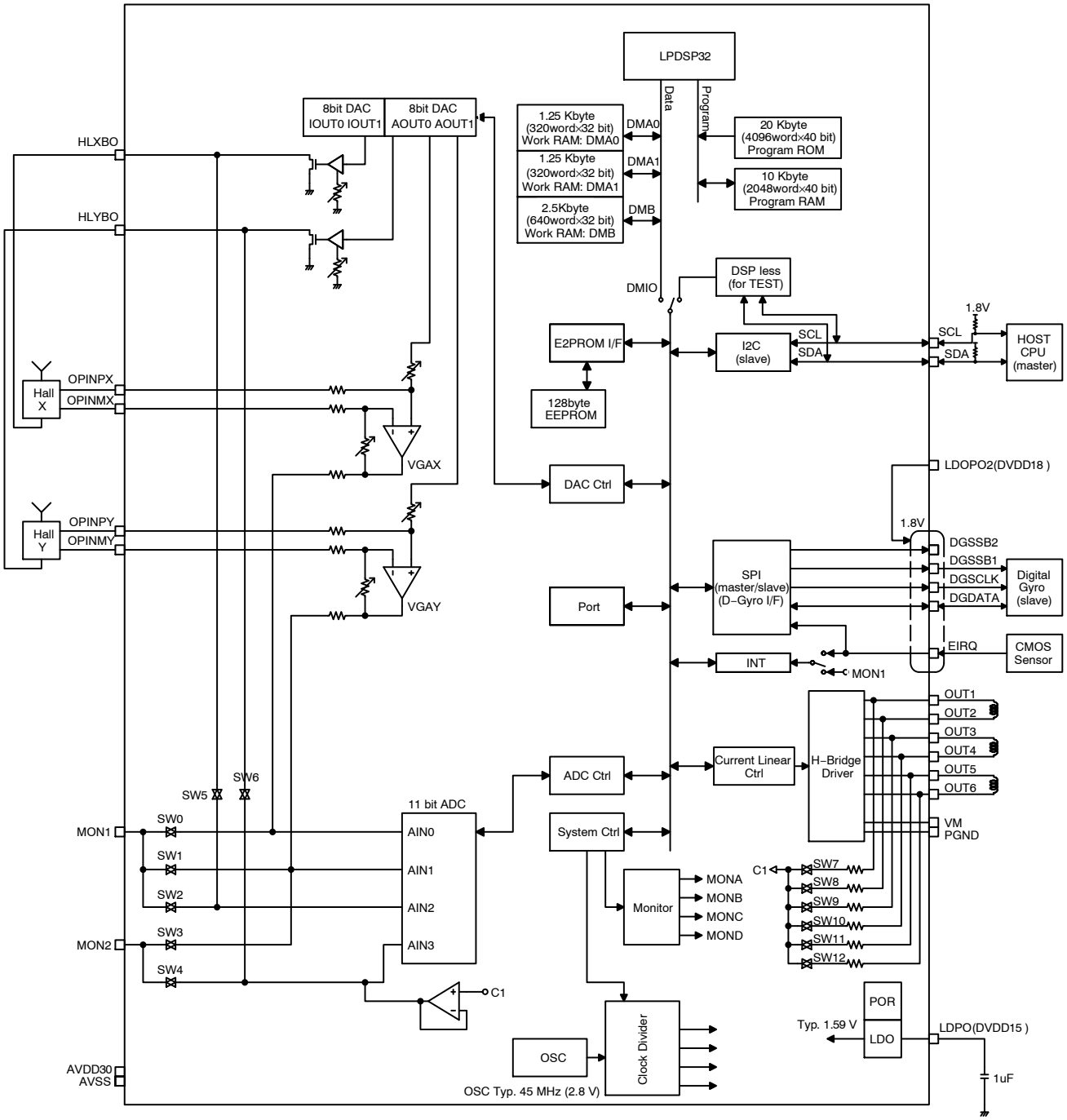


Figure 1. Block Diagram

APPLICATION DIAGRAM

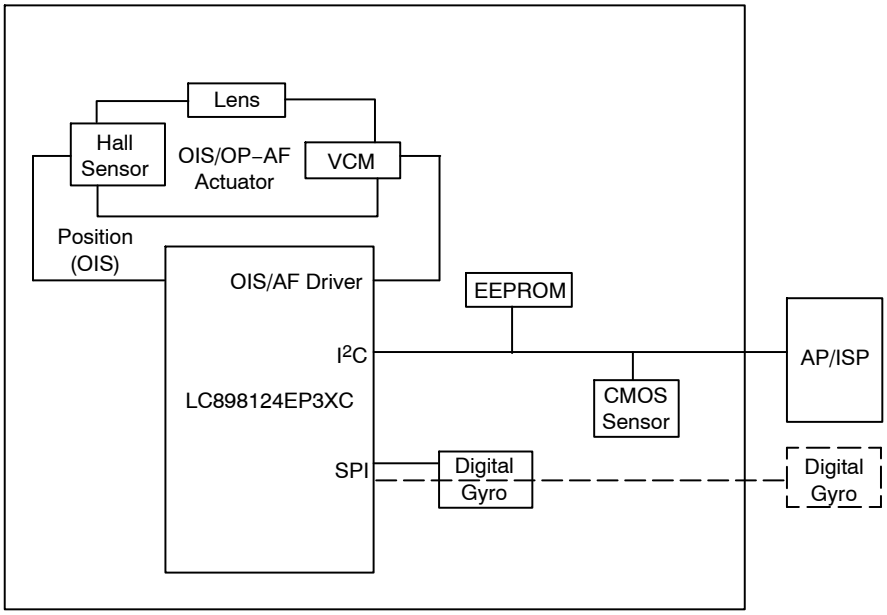


Figure 2. Application Diagram

PIN LAYOUT

Table 1. BOTTOM VIEW

C	OUT4	OUT3	OUT2	OUT1	OPINPX	HLXBO	MON2	EIRQ	DGDATA
B	VM	PGND	OPINPY	OPINMY	OPINMX	HLYBO	IOVDD	SDA	DGSCLK
A	OUT5	OUT6	AVSS	AVDD30	LDPO	MON1	DGSSB2	SCL	DGSSB1
	1	2	3	4	5	6	7	8	9

Driver VDD/VSS Internal VDD Output Driver

Table 2. PIN DESCRIPTION

NO.	Pin	I/O	I/O Spec	Primary Function	Sub Functions	Init
1	MON1	B		Servo Monitor Analog In/Out	2−wire serial Data Interrupt Input	Z
2	MON2	B		Servo Monitor Analog In/Out	2−wire serial Clock	Z
3	SCL	B	OD	2−wire serial HOST I/F Clock Slave		Z
4	SDA	B	OD	2−wire serial HOST I/F Data Slave		Z
5	IOVDD	P		I/O Power		
6	DGSSB2	B		Digital Gyro Data I/F Chip Select2 Out (3/4−wire Master)		U
7	DGSSB1	B		Digital Gyro Data I/F Chip Select1 Out (3/4−wire Master)	Digital Gyro Data I/F Chip Select In (3/4−wire Slave)	Z
8	DGSCLK	B		Digital Gyro Data I/F Clock Out (3/4−wire Master)	Digital Gyro Data I/F Clock In (3/4−wire Slave)	Z
9	EIRQ	B	OD	Interrupt Input	Digital Gyro Data I/F Data In (4−wire Master/Slave)	Z

Table 2. PIN DESCRIPTION (continued)

NO.	Pin	I/O	I/O Spec	Primary Function	Sub Functions	Init
10	DGDATA	B		Digital Gyro Data I/F Data (3−wire Master)	Digital Gyro Data I/F Data Out (4−wire Master/Slave)	Z
					Digital Gyro Data I/F Data (3−wire Slave)	
11	HLXBO	O		OIS Hall X Bias Output		Z
12	HLYBO	O		OIS Hall Y Bias Output		Z
13	OPINMX	I		OIS Hall X Opamp Input Minus		Z
14	OPINPX	I		OIS Hall X Opamp Input Plus		−
15	OPINMY	I		OIS Hall Y Opamp Input Minus		−
16	OPINPY	I		OIS Hall Y Opamp Input Plus		−
17	OUT1	O		OIS Driver Output		Z
18	OUT2	O		OIS Driver Output		Z
19	OUT3	O		OIS Driver Output		Z
20	OUT4	O		OIS Driver Output		Z
21	OUT5	O		Open−AF Driver Output		Z
22	OUT6	O		Open−AF Driver Output		Z
23	AVDD30	P		Analog Power		−
24	AVSS	P		Analog GND		−
25	VM	P		Driver Power		−
26	PGND	P		Driver GND		
27	LDPO	P		Internal V LDO Power Output		

1. Process when pins are not used:
   PIN TYPE “O” − Ensure that it is set to OPEN.
   PIN TYPE “I” − OPEN is inhibited. Ensure that it is connected to the V_{DD} or V_{SS} even when it is unused.
   (Please contact **onsemi** for more information about selection of V_{DD} or V_{SS}.)
   PIN TYPE “B” − If you are unsure about processing method on the pin description of pin layout table, please contact us.
2. Note that incorrect processing of unused pins may result in defects.

ELECTRICAL CHARACTERISTICS

Table 3. ABSOLUTE MAXIMUM RATINGS (at AVSS = 0 V, PGND = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	$V_{AD}30$ max	Ta ≤ 25°C	–0.3 to +4.6	V
	VM max	Ta ≤ 25°C	–0.3 to +4.6	
	V_{IO} max	Ta ≤ 25°C	–0.3 to +4.6	
Input/Output Voltage	$V_{AI}30$, $V_{AO}30$	Ta ≤ 25°C	–0.3 to $V_{AD}30$ +0.3	V
	$V_{MI}30$, $V_{MO}30$	Ta ≤ 25°C	–0.3 to $V_{M}30$ +0.3	
	V_{II}, V_{IOO}	Ta ≤ 25°C	–0.3 to $V_{IO}18$ +0.3	V
Storage Temperature	Tstg		–55 to +125	°C
Operating Temperature	Topr1	Read for EEPROM	–30 to +85	°C
	Topr2	Program & Erase for EEPROM	–30 to +70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. ALLOWABLE OPERATING RATINGS (at T_A =–30 to +85°C, AVSS = 0 V, PGND = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	$V_{AD}30$	2.6	2.8	3.3	V
Input Voltage Range	V_{INA}	0	–	$V_{AD}30$	V
3.0 V POWER SUPPLY (VM)					
Power Supply Voltage	$V_{M}30$	1.8	2.8	The lower of 3.3 and AVDD30 +0.5	V
Input Voltage Range	V_{INM}	0	–	$V_{M}30$	V
1.8 V POWER SUPPLY (IOVDD)					
Power Supply Voltage	V_{IO}	1.7	1.8	3.3	V
Input Voltage Range	V_{INI}	0	–	V_{IO}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. D. C. CHARACTERISTICS: INPUT/OUTPUT
(at T_A =–30 to +85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.6 to 3.3. V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit	Applicable pins
High−level Input Voltage	VIH	CMOS schmitt	0.75IOVDD			V	DGSSB1, DGSCLK
Low−level Input Voltage	VIL				0.25IOVDD	V	DGDATA,EIRQ DGSSB2
High−level Input Voltage	VIH		1.4			V	SCL,SDA
Low−level Input Voltage	VIL				0.4	V	SCL,SDA
High−level Input Voltage	VIH		0.75AVDD30			V	MON1,MON2
Low−level Input Voltage	VIL				0.25AVDD30	V	
High−level Output Voltage	VOH	IOH = –2 mA	IOVDD–0.2			V	DGSSB1, DGSCLK DGDATA, DGSSB2

Table 5. D. C. CHARACTERISTICS: INPUT/OUTPUT (continued)
(at T_A =−30 to +85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.6 to 3.3. V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit	Applicable pins
Low−level Output Voltage	VOL	IOL = 2 mA			0.2	V	DGSSB1, DGSCLK DGDATA,EIRQ DGSSB2
High−level Output Voltage	VOH	IOH = −2 mA	AVDD30−0.3			V	MON1,MON2
Low−level Output Voltage	VOL	IOL = 2 mA			0.3	V	
Low−level Output Voltage	VOL	IOL = 2 mA			0.2	V	SCL,SDA,
Analog Input Voltage	VAI		AVSS		AVDD30	V	MON1,MON2
Pull Up Resistor	Rup		20		250	kΩ	DGSSB1, DGSCLK DGDATA MON1,MON2 HLXBO,HLYBO DGSSB2
Pull Down Resistor	Rdn		20		250	kΩ	DGSSB1, DGSCLK DGDATA,EIRQ MON1,MON2 HLXBO,HLYBO DGSSB2

Table 6. DRIVER OUTPUT (at T_A = 25°C, V_{SS} = 0 V, PGND = 0 V, AVDD30 = VM = 2.8 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT1 to OUT4	Ifull	Full code	190	200	210	mA
Output Current OUT5, OUT6		Full Code OP−AF(bidirection)	123.5	130	136.5	mA
OutputON Resistance OUT1 to OUT4	Ron	Full code Total On resistance	−	2.2	−	Ω
Output ON Resistance OUT5, OUT6		Full code Total On resistance	−	2.2	−	Ω

3. Calculation method of max. current(Imax):
Rcoil∗ : Coil resistance of actuator Rb∗ : Wiring resistance of the board
VM / (Rcoil + Rb + Ron) ≥ Ifull; Imax = Ifull
VM / (Rcoil + Rb + Ron) < Ifull; Imax = VM / (Rcoil + Rb + Ron)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 7. NON−VOLATILE MEMORY CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable circuit
Endurance	EN				1000	Cycles	EEPROM
Data Retention	RT		10			Years	EEPROM
Write Time	tWT				20	ms	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC CHARACTERISTICS

V_{DD} Supply Timing

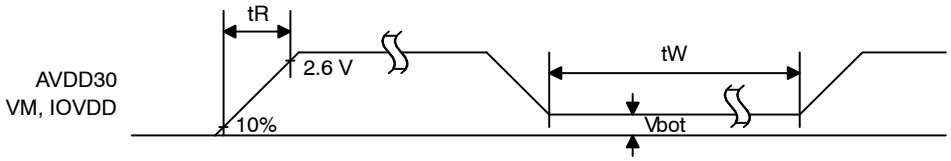


Figure 3. V_{DD} Supply Timing

Table 8. V_{DD} SUPPLY TIMING

Item	Symbol	Min	Typ	Max	Units
Rise Time	tR			3	ms
Wait Time	tW	100			ms
Bottom Voltage	Vbot			0.2	V

Injection order between AVDD30 and VM, IOVDD is below.

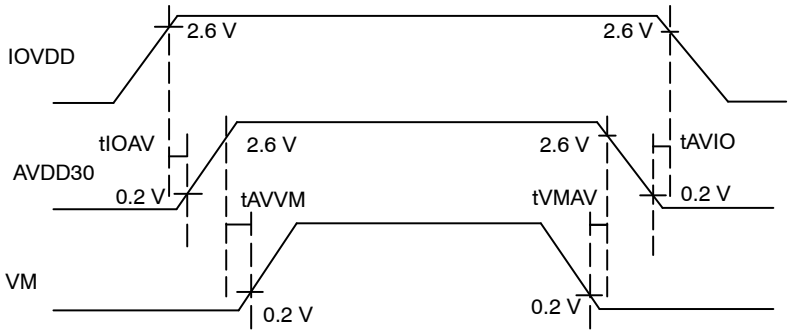


Figure 4.

Table 9. V_{DD} SUPPLY TIMING

Item	Symbol	Min	Typ	Max	Units
IOVDD ON to AVDD30 ON	tIOAV	0			ms
AVDD30 ON to VM ON	tAVVM	0			ms
VM OFF to AVDD30 OFF	tVMAV	0			ms
AVDD30 OFF to IOVDD OFF	tAVIO	0			ms

4. VM ≤ AVDD30 +0.5 V
5. When IOVDD is power OFF, it is prohibition to apply the voltage to a 1.8 V pins*.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SDA, SCL, EIRQ tolerate 3 V input at the time of power off.
The data in the EEPROM may be rewritten unintentionally if you do not keep specifications.
And it is forbidden to power off during EEPROM access. The data in the EEPROM may be rewritten unintentionally.
OIS driver and AF driver are recommended to set standby before VM power off.

AC SPECIFICATION

The figure below shows interface timing definition and following table shows electric characteristics.
The communication protocol is compatible with I^2C (Fast mode Plus).
This circuit has clock stretch function.

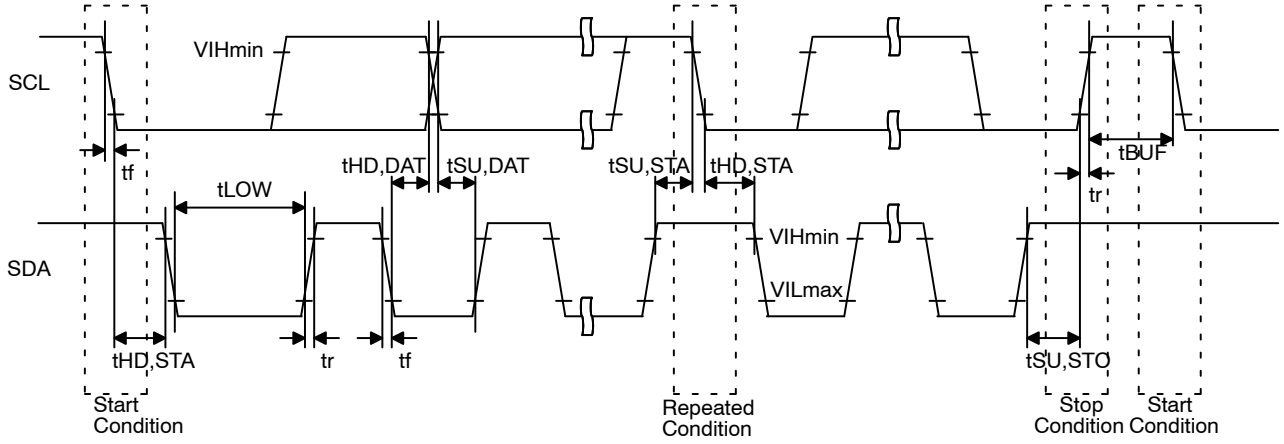


Figure 5. 2−wire Serial Interface Timing Definition

Table 10. ELECTRIC CHARACTERISTICS FOR 2−WIRE SERIAL INTERFACE (AC CHARACTERISTICS)

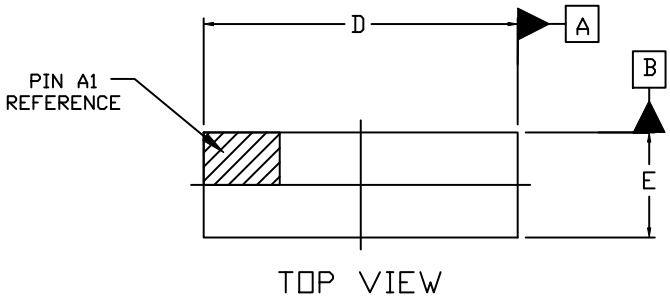
Item	Symbol	Pin name	Min	Typ	Max	Units
SCL Clock Frequency	Fscl	SCL			1000	kHz
START Condition Hold Time	tHD,STA	SCL SDA	0.26			µs
SCL Clock Low Period	tLOW	SCL	0.5			µs
SCL Clock High Period	tHIGH	SCL	0.26			µs
Setup Time for Repetition START Condition	tSU,STA	SCL SDA	0.26			µs
Data Hold Time	tHD,DAT	SCL SDA	0 (Note 6)		0.9	µs
Data Setup Time	tSU,DAT	SCL SDA	50			ns
SDA, SCL Rising Time	tr	SCL SDA			120	ns
SDA, SCL Falling Time	tf	SCL SDA			120	ns
STOP Condition Setup Time	tSU,STO	SCL SDA	0.26			µs
Bus Free Time between STOP and START	tBUF	SCL SDA	0.5			µs

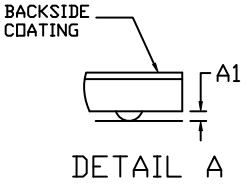
6. Although the I^2C specification defines a condition that 300 ns of hold time is required internally. This LSI is designed for a condition with typ. 40 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

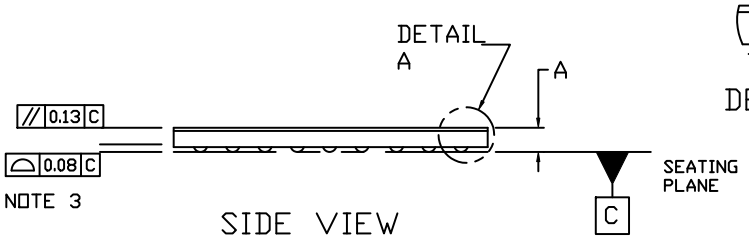
SCALE 4:1

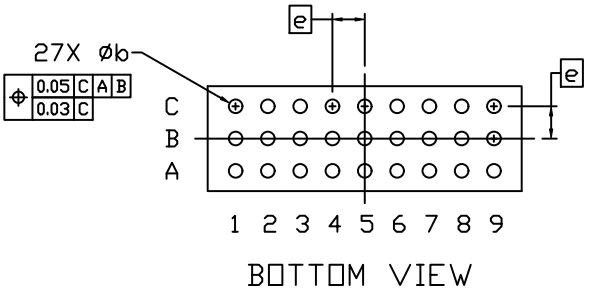
WLCSP27, 3.89x1.30, 0.4P
CASE 567NJ
ISSUE A

DATE 22 SEP 2020



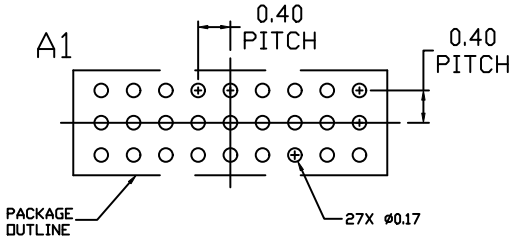






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	0.33
A1	0.04 REF		
b	0.12	0.17	0.22
D	3.84	3.89	3.94
E	1.25	1.30	1.35
e	0.40 BSC		



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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