L4949, NCV4949

100 mA, 5.0 V, Low Dropout Voltage Regulator with Reset and Sense

The L4949 is a monolithic integrated 5.0 V voltage regulator with a very low dropout and additional functions such as reset and an uncommitted voltage sense comparator.

It is designed for supplying microcontroller/microprocessor controlled systems particularly in automotive applications.

Features
- Operating DC Supply Voltage Range 5.0 V to 28 V
- Transient Supply Voltage Up to 40 V
- Extremely Low Quiescent Current in Standby Mode
- High Precision Output Voltage 5.0 V ±1%
- Output Current Capability Up to 100 mA
- Very Low Dropout Voltage Less Than 0.4 V
- Reset Circuit Sensing The Output Voltage
- Programmable Reset Pulse Delay
- Voltage Sense Comparator
- Thermal Shutdown and Short Circuit Protections
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- These are Pb–Free Devices

Figure 1. Representative Block Diagram
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Operating Supply Voltage</td>
<td>$V_{CC}$</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>Transient Supply Voltage ($t &lt; 1.0$ s)</td>
<td>$V_{CC TR}$</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td>$I_{out}$</td>
<td>Internally Limited</td>
<td>–</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{out}$</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Sense Input Current</td>
<td>$I_{SI}$</td>
<td>±1.0</td>
<td>mA</td>
</tr>
<tr>
<td>Sense Input Voltage</td>
<td>$V_{SI}$</td>
<td>$V_{CC}$</td>
<td>–</td>
</tr>
<tr>
<td>Output Voltages</td>
<td>$V_{Reset}$</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Sense Output</td>
<td>$V_{SO}$</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Output Currents</td>
<td>$I_{Reset}$</td>
<td>5.0</td>
<td>mA</td>
</tr>
<tr>
<td>Sense Output</td>
<td>$I_{SO}$</td>
<td>5.0</td>
<td>mA</td>
</tr>
<tr>
<td>Preregulator Output Voltage</td>
<td>$V_{Z}$</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>Preregulator Output Current</td>
<td>$I_{Z}$</td>
<td>5.0</td>
<td>mA</td>
</tr>
<tr>
<td>ESD Protection at any pin</td>
<td>–</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Human Body Model</td>
<td>–</td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td>Thermal Resistance, Junction-to-Air</td>
<td>$R_{JA}$</td>
<td>100</td>
<td>°C/W</td>
</tr>
<tr>
<td>P Suffix, DIP–8 Plastic Package, Case 626</td>
<td>–</td>
<td>200</td>
<td>°C/W</td>
</tr>
<tr>
<td>D Suffix, SOIC–8 Plastic Package, Case 751</td>
<td>–</td>
<td>85</td>
<td>°C/W</td>
</tr>
<tr>
<td>PD Suffix, SOIC–8 EP Plastic Package, Case 751AC (Note 1)</td>
<td>–</td>
<td>80</td>
<td>°C/W</td>
</tr>
<tr>
<td>D Suffix, SOIC–20 Plastic Package, Case 751D</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>$T_J$</td>
<td>–40 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>–65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Soldered to a 200 mm² 1 oz. copper–clad FR–4 board.

### Electrical Characteristics ($V_{CC} = 14$ V, $-40°C < T_A < 125°C$, unless otherwise specified.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage ($T_A = 25°C$, $I_{out} = 1.0$ mA)</td>
<td>$V_{out}$</td>
<td>4.95</td>
<td>5.0</td>
<td>5.05</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage ($6.0$ V $&lt; V_{CC} &lt; 28$ V, $1.0$ mA $&lt; I_{out} &lt; 50$ mA)</td>
<td>$V_{out}$</td>
<td>4.9</td>
<td>5.0</td>
<td>5.1</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage ($V_{CC} = 35$ V, $t &lt; 1.0$ s, $1.0$ mA $&lt; I_{out} &lt; 50$ mA)</td>
<td>$V_{out}$</td>
<td>4.9</td>
<td>5.0</td>
<td>5.1</td>
<td>V</td>
</tr>
<tr>
<td>Dropout Voltage ($I_{out} = 10$ mA)</td>
<td>$V_{drop}$</td>
<td>–</td>
<td>0.1</td>
<td>0.25</td>
<td>V</td>
</tr>
<tr>
<td>Dropout Voltage ($I_{out} = 50$ mA)</td>
<td>–</td>
<td>0.2</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Dropout Voltage ($I_{out} = 100$ mA)</td>
<td>–</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input to Output Voltage Difference in Undervoltage Condition ($V_{CC} = 4.0$ V, $I_{out} = 35$ mA)</td>
<td>$V_{IO}$</td>
<td>–</td>
<td>0.2</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Line Regulation ($6.0$ V $&lt; V_{CC} &lt; 28$ V, $I_{out} = 1.0$ mA)</td>
<td>$R_{line}$</td>
<td>–</td>
<td>1.0</td>
<td>20</td>
<td>mV</td>
</tr>
<tr>
<td>Load Regulation ($1.0$ mA $&lt; I_{out} &lt; 100$ mA)</td>
<td>$R_{load}$</td>
<td>–</td>
<td>8.0</td>
<td>30</td>
<td>mV</td>
</tr>
<tr>
<td>Current Limit</td>
<td>$I_{Lim}$</td>
<td>105</td>
<td>200</td>
<td>400</td>
<td>mA</td>
</tr>
<tr>
<td>Quiescent Current ($I_{out} = 0.3$ mA, $T_A &lt; 100°C$)</td>
<td>$I_{QSE}$</td>
<td>–</td>
<td>150</td>
<td>260</td>
<td>µA</td>
</tr>
<tr>
<td>Quiescent Current ($I_{out} = 100$ mA)</td>
<td>$I_Q$</td>
<td>–</td>
<td>5.0</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (continued) (**V**<sub>CC</sub> = 14 V, −40°C < T<sub>A</sub> < 125°C, unless otherwise specified.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RESET</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset Threshold Voltage</td>
<td>V&lt;sub&gt;Resth&lt;/sub&gt;</td>
<td>−</td>
<td>V&lt;sub&gt;out&lt;/sub&gt; − 0.5</td>
<td>−</td>
<td>V</td>
</tr>
<tr>
<td>Reset Threshold Hysteresis @ T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>V&lt;sub&gt;Resth,hys&lt;/sub&gt;</td>
<td>50</td>
<td>100</td>
<td>200</td>
<td>mV</td>
</tr>
<tr>
<td>Reset Pulse Delay (C&lt;sub&gt;T&lt;/sub&gt; = 100 nF, t&lt;sub&gt;R&lt;/sub&gt; ≥ 100 μs)</td>
<td>t&lt;sub&gt;ResD&lt;/sub&gt;</td>
<td>55</td>
<td>100</td>
<td>180</td>
<td>ms</td>
</tr>
<tr>
<td>Reset Reaction Time (C&lt;sub&gt;T&lt;/sub&gt; = 100 nF)</td>
<td>t&lt;sub&gt;ResR&lt;/sub&gt;</td>
<td>−</td>
<td>5.0</td>
<td>30</td>
<td>μs</td>
</tr>
<tr>
<td>Reset Output Low Voltage (R&lt;sub&gt;Reset&lt;/sub&gt; = 10 kΩ to V&lt;sub&gt;out&lt;/sub&gt;, V&lt;sub&gt;CC&lt;/sub&gt; ≥ 3.0 V)</td>
<td>V&lt;sub&gt;ResL&lt;/sub&gt;</td>
<td>−</td>
<td>−</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Reset Output High Leakage Current (V&lt;sub&gt;Reset&lt;/sub&gt; = 5.0 V)</td>
<td>I&lt;sub&gt;ResH&lt;/sub&gt;</td>
<td>−</td>
<td>−</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>Delay Comparator Threshold</td>
<td>V&lt;sub&gt;CTth&lt;/sub&gt;</td>
<td>−</td>
<td>2.0</td>
<td>−</td>
<td>V</td>
</tr>
<tr>
<td>Delay Comparator Threshold Hysteresis</td>
<td>V&lt;sub&gt;CTth_hys&lt;/sub&gt;</td>
<td>−</td>
<td>100</td>
<td>−</td>
<td>mV</td>
</tr>
<tr>
<td><strong>SENSE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sense Low Threshold (V&lt;sub&gt;S&lt;/sub&gt;&lt;sub&gt;I&lt;/sub&gt; Decreasing = 1.5 V to 1.0 V)</td>
<td>V&lt;sub&gt;SOth&lt;/sub&gt;</td>
<td>1.16</td>
<td>1.23</td>
<td>1.35</td>
<td>V</td>
</tr>
<tr>
<td>Sense Threshold Hysteresis</td>
<td>V&lt;sub&gt;SOth_hys&lt;/sub&gt;</td>
<td>20</td>
<td>100</td>
<td>200</td>
<td>mV</td>
</tr>
<tr>
<td>Sense Output Low Voltage (V&lt;sub&gt;S&lt;/sub&gt;&lt;sub&gt;I&lt;/sub&gt; ≤ 1.16 V, V&lt;sub&gt;CC&lt;/sub&gt; ≥ 3.0 V, R&lt;sub&gt;S&lt;/sub&gt;&lt;sub&gt;O&lt;/sub&gt; = 10 kΩ to V&lt;sub&gt;out&lt;/sub&gt;)</td>
<td>V&lt;sub&gt;SOL&lt;/sub&gt;</td>
<td>−</td>
<td>−</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Sense Output Leakage (V&lt;sub&gt;S&lt;/sub&gt;&lt;sub&gt;O&lt;/sub&gt; = 5.0 V, V&lt;sub&gt;S&lt;/sub&gt;&lt;sub&gt;I&lt;/sub&gt; ≥ 1.5 V)</td>
<td>I&lt;sub&gt;SOH&lt;/sub&gt;</td>
<td>−</td>
<td>−</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>Sense Input Current</td>
<td>I&lt;sub&gt;SI&lt;/sub&gt;</td>
<td>−1.0</td>
<td>0.1</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td><strong>PREREGULATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Preregulator Output Voltage (I&lt;sub&gt;Z&lt;/sub&gt; = 10 μA)</td>
<td>V&lt;sub&gt;Z&lt;/sub&gt;</td>
<td>−</td>
<td>6.3</td>
<td>−</td>
<td>V</td>
</tr>
</tbody>
</table>

### PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Supply Voltage</td>
</tr>
<tr>
<td>1</td>
<td>S&lt;sub&gt;I&lt;/sub&gt;</td>
<td>Input of Sense Comparator</td>
</tr>
<tr>
<td>3</td>
<td>V&lt;sub&gt;Z&lt;/sub&gt;</td>
<td>Output of Preregulator</td>
</tr>
<tr>
<td>4</td>
<td>C&lt;sub&gt;T&lt;/sub&gt;</td>
<td>Reset Delay Capacitor</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>6</td>
<td>Reset</td>
<td>Output of Reset Comparator</td>
</tr>
<tr>
<td>7</td>
<td>S&lt;sub&gt;O&lt;/sub&gt;</td>
<td>Output of Sense Comparator</td>
</tr>
<tr>
<td>8</td>
<td>V&lt;sub&gt;out&lt;/sub&gt;</td>
<td>Main Regulator Output</td>
</tr>
<tr>
<td></td>
<td>NC</td>
<td>No Connect</td>
</tr>
<tr>
<td></td>
<td>EPAD</td>
<td>Connect to Ground potential or leave unconnected</td>
</tr>
</tbody>
</table>
Figure 2. ESR Stability Border Vs. Output Current (Full ESR Range)

Figure 3. ESR Stability Border Vs. Output Current (Very Low ESR)

Figure 4. Output Voltage versus Junction Temperature

Figure 5. Output Voltage versus Supply Voltage

Figure 6. Dropout Voltage versus Output Current

Figure 7. Dropout Voltage versus Junction Temperature
TYPICAL CHARACTERIZATION CURVES (continued)

**Figure 8. Quiescent Current versus Output Current**

**Figure 9. Quiescent Current versus Supply Voltage**

**Figure 10. Reset Output versus Regulator Output Voltage**

**Figure 11. Reset Thresholds versus Junction Temperature**

**Figure 12. Sense Output versus Sense Input Voltage**

**Figure 13. Sense Thresholds versus Junction Temperature**

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http://onsemi.com
Supply Voltage Transient

High supply voltage transients can cause a reset output signal perturbation. For supply voltages greater than 8.0 V the circuit shows a high immunity of the reset output against supply transients of more than 100 V/\mu s. For supply voltages less than 8.0 V supply transients of more than 0.4 V/\mu s can cause a reset signal perturbation. To improve the transient behavior for supply voltages less than 8.0 V a capacitor at Pin 3 can be used. A capacitor at Pin 3 (C3 ≤ 1.0 \mu F) also reduces the output noise.

NOTE: 1. For stability: C_s ≥ 1.0 \mu F, C_O ≥ 4.7 \mu F, ESR < 10 \Omega at 10 kHz
2. Recommended for application: C_s = C_O = 10 \mu F

Figure 14. Application Schematic
The L4949 is a monolithic integrated low dropout voltage regulator. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. It is also suitable in other applications where the included functions are required. The modular approach of this device allows the use of other features and functions independently when required.

**Voltage Regulator**

The voltage regulator uses an isolated collector vertical PNP transistor as a regulating element. With this structure, very low dropout voltage at currents up to 100 mA is obtained. The dropout operation of the standby regulator is maintained down to 3.0 V input supply voltage. The output voltage is regulated up to a transient input supply voltage of 35 V.

A typical curve showing the standby output voltage as a function of the input supply voltage is shown in Figure 16. The current consumption of the device (quiescent current) is less than 200 μA.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled. The quiescent current as a function of the supply input voltage is shown in Figure 17.

**Short Circuit Protection:**

The maximum output current is internally limited. In case of short circuit, the output current is foldback current limited as described in Figure 15.

**Preregulator**

To improve transient immunity a preregulator stabilizes the internal supply voltage to 6.0 V. This internal voltage is present at Pin 3 (VZ). This voltage should not be used as an output because the output capability is very small (≤ 100 μA).

This output may be used to improve transient behavior for supply voltages less than 8.0 V. In this case a capacitor (100 nF – 1.0 μF) must be connected between Pin 3 and GND. If this feature is not used Pin 3 must be left open.
**Reset Circuit**

The block circuit diagram of the reset circuit is shown in Figure 18.

The reset circuit supervises the output voltage. The reset threshold of 4.5 V is defined by the internal reference voltage and standby output divider.

The reset pulse delay time \( t_{RD} \) is defined by the charge time of an external capacitor \( C_T \):

\[
t_{RD} = \frac{C_T \times 2.0 \text{ V}}{2.0 \mu\text{A}}
\]

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor \( C_T \) and is proportional to the value of \( C_T \). The reaction time of the reset circuit increases the noise immunity.

Output voltage drops below the reset threshold only marginally longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time will be generated for output voltage drops longer than approximately 50 \( \mu\text{s} \). The typical reset output waveforms are shown in Figure 19.

**Sense Comparator**

The sense comparator compares an input signal with an internal voltage reference of typical 1.23 V. The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after a protection diode and to provide additional information to the microprocessor such as low voltage warnings.

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**Figure 18. Reset Circuit**

**Figure 19. Typical Reset Output Waveforms**
<table>
<thead>
<tr>
<th>Device</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>L4949NG</td>
<td>T$_J$ = −40°C to +125°C</td>
<td>PDIP–8 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>L4949DG</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>L4949DR2G</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV4949DG*</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>NCV4949PDG*</td>
<td></td>
<td>SOIC–8 EP (Pb–Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>NCV4949DR2G*</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV4949PDR2G*</td>
<td></td>
<td>SOIC–8 EP (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV4949DWR2G*</td>
<td></td>
<td>SOIC–20W (Pb–Free)</td>
<td>1000 Units / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NVC4949: T$_{low}$ = −40°C, T$_{high}$ = +125°C. Guaranteed by design.

NCV prefix is for automotive and other applications requiring site and change control.
**MECHANICAL CASE OUTLINE**

**PACKAGE DIMENSIONS**

**PDIP-8**  
CASE 626-05  
ISSUE P  

**DATE 22 APR 2015**

**NOTES:**
2. CONTROLLING DIMENSION: INCHES.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

**DIMENSIONS**

<table>
<thead>
<tr>
<th>INCHES</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.015 – 0.038 – 0.30</td>
</tr>
<tr>
<td>A1</td>
<td>0.115 – 0.159 – 2.92 – 4.95</td>
</tr>
<tr>
<td>b</td>
<td>0.014 – 0.022 – 0.35 – 0.56</td>
</tr>
<tr>
<td>b2</td>
<td>0.060 – 1.52</td>
</tr>
<tr>
<td>C</td>
<td>0.008 – 0.014 – 0.20 – 0.30</td>
</tr>
<tr>
<td>D</td>
<td>0.095 – 0.400 – 0.92 – 10.16</td>
</tr>
<tr>
<td>D1</td>
<td>0.005 – 0.013 – 0.13</td>
</tr>
<tr>
<td>E</td>
<td>0.300 – 0.325 – 7.62 – 8.26</td>
</tr>
<tr>
<td>E1</td>
<td>0.240 – 0.280 – 6.10 – 7.11</td>
</tr>
<tr>
<td>e</td>
<td>0.100 BSC – 2.54 BSC</td>
</tr>
<tr>
<td>eB</td>
<td>0.015 – 0.150 – 0.381</td>
</tr>
<tr>
<td>L</td>
<td>0.115 – 0.150 – 2.92 – 3.81</td>
</tr>
<tr>
<td>M</td>
<td>10° – 10°</td>
</tr>
</tbody>
</table>

**STYLE 1:**
1. PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. VCC

**MARKING DIAGRAM**

- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "*", may or may not be present.

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NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

GENERAL MARKING DIAGRAM*

SOLDERING FOOTPRINT*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2
### STYLE 1:
- **PIN 1. Emitter**
- **PIN 2. Source**
- **PIN 3. Source**
- **PIN 4. Gate**
- **PIN 5. Gate**
- **PIN 6. Drain**
- **PIN 7. Drain**
- **PIN 8. Emitter**

### STYLE 2:
- **PIN 1. Collector, Die #1**
- **PIN 2. Collector, #2**
- **PIN 3. Collector, #2**
- **PIN 4. Emitter**
- **PIN 5. Emitter, #2**
- **PIN 6. Emitter, #2**
- **PIN 7. Base, #1**
- **PIN 8. Collector, #1**

### STYLE 3:
- **PIN 1. Drain, Die #1**
- **PIN 2. Drain, #2**
- **PIN 3. Drain, #2**
- **PIN 4. Source, #2**
- **PIN 5. Source, #2**
- **PIN 6. Source, #2**
- **PIN 7. Collector, #1**
- **PIN 8. Collector, #1**

### STYLE 4:
- **PIN 1. Anode**
- **PIN 2. Base, #1**
- **PIN 3. Base, #1**
- **PIN 4. Emitter, #2**
- **PIN 5. Emitter, #2**
- **PIN 6. Collector, #2**
- **PIN 7. Collector, #2**
- **PIN 8. Common Cathode**

### STYLE 5:
- **PIN 1. Drain**
- **PIN 2. Drain**
- **PIN 3. Drain**
- **PIN 4. Ground**
- **PIN 5. Source**
- **PIN 6. Source**
- **PIN 7. Source**
- **PIN 8. Ground**

### STYLE 6:
- **PIN 1. Source**
- **PIN 2. Drain**
- **PIN 3. Drain**
- **PIN 4. Drain**
- **PIN 5. Source**
- **PIN 6. Source**
- **PIN 7. Source**
- **PIN 8. Drain**

### STYLE 7:
- **PIN 1. Input**
- **PIN 2. External Bypass**
- **PIN 3. Third Stage Source**
- **PIN 4. Ground**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Drain**
- **PIN 8. First Stage Vd**

### STYLE 8:
- **PIN 1. Collector, Die #1**
- **PIN 2. Base, #1**
- **PIN 3. Base, #1**
- **PIN 4. Collector, #2**
- **PIN 5. Collector, #2**
- **PIN 6. Emitter, #2**
- **PIN 7. Emitter, #2**
- **PIN 8. Collector, #1**

### STYLE 9:
- **PIN 1. Emitter, Common**
- **PIN 2. Collector, Die #1**
- **PIN 3. Collector, Die #2**
- **PIN 4. Emitter, Common**
- **PIN 5. Emitter, Common**
- **PIN 6. Base, Die #2**
- **PIN 7. Base, Die #2**
- **PIN 8. Emitter, Common**

### STYLE 10:
- **PIN 1. Ground**
- **PIN 2. Bias 1**
- **PIN 3. Output**
- **PIN 4. Ground**
- **PIN 5. Ground**
- **PIN 6. Bias 2**
- **PIN 7. Input**
- **PIN 8. Drain**

### STYLE 11:
- **PIN 1. Source 1**
- **PIN 2. Gate 1**
- **PIN 3. Source 2**
- **PIN 4. Gate 2**
- **PIN 5. Drain 2**
- **PIN 6. Drain 2**
- **PIN 7. Drain 1**
- **PIN 8. Drain 1**

### STYLE 12:
- **PIN 1. Source**
- **PIN 2. Source**
- **PIN 3. Source**
- **PIN 4. Ground**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Drain**
- **PIN 8. Drain**

### STYLE 13:
- **PIN 1. N.C.**
- **PIN 2. Source**
- **PIN 3. Source**
- **PIN 4. Gate**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Drain**
- **PIN 8. Drain**

### STYLE 14:
- **PIN 1. N-Source**
- **PIN 2. Source**
- **PIN 3. P-Source**
- **PIN 4. P-Gate**
- **PIN 5. P-Drain**
- **PIN 6. P-Drain**
- **PIN 7. N-Drain**
- **PIN 8. N-Drain**

### STYLE 15:
- **PIN 1. Anode 1**
- **PIN 2. Source 1**
- **PIN 3. Source 2**
- **PIN 4. Gate 2**
- **PIN 5. Drain 2**
- **PIN 6. Drain 2**
- **PIN 7. Drain 1**
- **PIN 8. Drain 1**

### STYLE 16:
- **PIN 1. Emitter 1**
- **PIN 2. Anode 1**
- **PIN 3. Anode 1**
- **PIN 4. Base 1**
- **PIN 5. Base 2**
- **PIN 6. Collector, Die #2**
- **PIN 7. Collector, Die #2**
- **PIN 8. Collector, Die #1**

### STYLE 17:
- **PIN 1. VCC**
- **PIN 2. V2OUT**
- **PIN 3. VOUT**
- **PIN 4. TIE**
- **PIN 5. RXE**
- **PIN 6. VEE**
- **PIN 7. GND**
- **PIN 8. ACC**

### STYLE 18:
- **PIN 1. Anode**
- **PIN 2. Anode**
- **PIN 3. Source**
- **PIN 4. Gate**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Cathode**
- **PIN 8. Cathode**

### STYLE 19:
- **PIN 1. Line 1 In**
- **PIN 2. Line 1 Out**
- **PIN 3. COMMON ANODE/GND**
- **PIN 4. COMMON ANODE/GND**
- **PIN 5. COMMON ANODE/GND**
- **PIN 6. COMMON ANODE/GND**
- **PIN 7. COMMON ANODE/GND**
- **PIN 8. COMMON ANODE/GND**

### STYLE 20:
- **PIN 1. Source (N)**
- **PIN 2. Gate (N)**
- **PIN 3. Source (P)**
- **PIN 4. Gate (P)**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Drain**
- **PIN 8. Drain**

### STYLE 21:
- **PIN 1. Cathode 1**
- **PIN 2. Cathode 2**
- **PIN 3. Cathode 3**
- **PIN 4. Cathode 4**
- **PIN 5. Cathode 5**
- **PIN 6. Common Anode**
- **PIN 7. Common Anode**
- **PIN 8. Cathode 6**

### STYLE 22:
- **PIN 1. Io Line 1**
- **PIN 2. Io Line 1**
- **PIN 3. Common Cathode/Vcc**
- **PIN 4. Common Cathode/Vcc**
- **PIN 5. Common Cathode/Vcc**
- **PIN 6. Io Line 4**
- **PIN 7. Io Line 5**
- **PIN 8. Io Line 5**

### STYLE 23:
- **PIN 1. Line 1 In**
- **PIN 2. Line 1 Out**
- **PIN 3. Common Anode/Gnd**
- **PIN 4. Common Anode/Gnd**
- **PIN 5. Common Anode/Gnd**
- **PIN 6. Common Anode/Gnd**
- **PIN 7. Common Anode/Gnd**
- **PIN 8. Common Anode/Gnd**

### STYLE 24:
- **PIN 1. Base**
- **PIN 2. Emitter**
- **PIN 3. Collector/Anode**
- **PIN 4. Collector/Anode**
- **PIN 5. Cathode**
- **PIN 6. Cathode**
- **PIN 7. Collector/Anode**
- **PIN 8. Collector/Anode**

### STYLE 25:
- **PIN 1. Vin**
- **PIN 2. N/C**
- **PIN 3. REXT**
- **PIN 4. GND**
- **PIN 5. IOU**
- **PIN 6. IOU**
- **PIN 7. IOU**
- **PIN 8. IOU**

### STYLE 26:
- **PIN 1. Gnd**
- **PIN 2. Diode**
- **PIN 3. Enable**
- **PIN 4. Ilim**
- **PIN 5. Source**
- **PIN 6. Source**
- **PIN 7. Source**
- **PIN 8. Drain**

### STYLE 27:
- **PIN 1. Ilimit**
- **PIN 2. Input+**
- **PIN 3. Source**
- **PIN 4. Source**
- **PIN 5. Source**
- **PIN 6. Source**
- **PIN 7. Source**
- **PIN 8. Drain**

### STYLE 28:
- **PIN 1. Sw_to Gnd**
- **PIN 2. Dasic_Off**
- **PIN 3. Dasic_Sw Det**
- **PIN 4. Gnd**
- **PIN 5. V_Mon**
- **PIN 6. Vbulk**
- **PIN 7. Vbulk**
- **PIN 8. Vin**
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

SOIC-8 EP
CASE 751AC
ISSUE E

DATE 05 OCT 2022

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE PROTRUSION SHALL BE 0.064 IN EXCESS OF MAXIMUM MATERIAL CONDITION,
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS, MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.026 PER SIDE. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.
6. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
7. DIMENSIONS a AND b APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD Tip.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "C0071", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

G9NMEC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
* = Pb−Free Package

DOCUMENT NUMBER: 98AON14029D
DESCRIPTION: SOIC-8 EP

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NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

<table>
<thead>
<tr>
<th>DIMENSIONS</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>0.10 - 0.25</td>
</tr>
<tr>
<td>b</td>
<td>0.35 - 0.49</td>
</tr>
<tr>
<td>c</td>
<td>0.23 - 0.32</td>
</tr>
<tr>
<td>D</td>
<td>12.65 - 12.95</td>
</tr>
<tr>
<td>E</td>
<td>7.40 - 7.60</td>
</tr>
<tr>
<td>h</td>
<td>0.25 - 0.75</td>
</tr>
<tr>
<td>l</td>
<td>0.50 - 0.90</td>
</tr>
</tbody>
</table>

**RECOMMENDED SOLDERING FOOTPRINT**

**DIMENSIONS: MILLIMETERS**

**PITCH**

1.27

**NOTES:**

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**GENERIC MARKING DIAGRAM**

XXXXXXX = Specific Device Code
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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “/”, may or may not be present. Some products may not follow the Generic Marking.