

# Low-Voltage Dual-Supply 4-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

## FXLA0104

### Description

The FXLA0104 is a configurable dual-voltage supply translator for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6 V to as low as 1.1 V. The A port tracks the  $V_{CCA}$  level and the B port tracks the  $V_{CCB}$  level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

The device remains in three-state as long as either  $V_{CC} = 0$  V, allowing either  $V_{CC}$  to be powered up first. Internal power-down control circuits place the device in 3-state if either  $V_{CC}$  is removed.

The OE input, when LOW, disables both the A and B ports by placing them in a 3-state condition. The OE input is supplied by  $V_{CCA}$ .

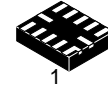
The FXLA0104 supports bi-directional translation without the need for a direction control pin. The two ports of the device have auto-direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

### Features

- Bi-Directional Interface between Two Levels: from 1.1 V to 3.6 V
- Fully Configurable: Inputs and Outputs Track  $V_{CC}$
- Non-Preferential Power-Up; Either  $V_{CC}$  May Be Powered Up First
- Outputs Switch to 3-State if Either  $V_{CC}$  is at GND
- Power-Off Protection
- Bus-Hold on Data Inputs Eliminates the Need for Pull-Up Resistors; Do Not Use Pull-Up Resistors on A or B Ports
- Control Input (OE) Referenced to  $V_{CCA}$  Voltage
- Available in the 12-Lead, 1.7 mm x 2.0 mm UMLP Package
- Direction Control Not Necessary
- 100 Mbps Throughput when Translating Between 1.8 V and 2.5 V
- ESD Protection Exceeds:
  - ◆ 6 kV HBM (per JESD22-A114 & Mil Std 883e 3015.7)
  - ◆ 2 kV CDM (per ESD STM 5.3)

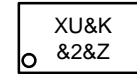
### Applications

- Cell Phone, PDA, Digital Camera, Portable GPS



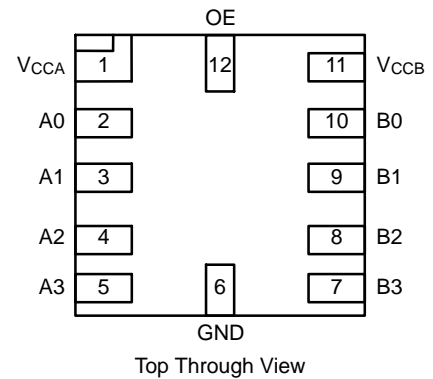
UQFN12 1.7x2.0, 0.4P  
CASE 523AE

### MARKING DIAGRAM



- XU = Specific Device Code
- &Z = Assembly Plant Code
- &2 = 2-Digit Plant Code
- &K = 2-Digits Lot Run Traceability Code

### PIN CONFIGURATION



### ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

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## PIN DEFINITIONS

Pin #	Name	Description
1	V <sub>CCA</sub>	A-Side Power Supply
2	A0	A-Side Inputs or 3-State Outputs
3	A1	A-Side Inputs or 3-State Outputs
4	A2	A-Side Inputs or 3-State Outputs
5	A3	A-Side Inputs or 3-State Outputs
6	GND	Ground
7	B3	B-Side Inputs or 3-State Outputs
8	B2	B-Side Inputs or 3-State Outputs
9	B1	B-Side Inputs or 3-State Outputs
10	B0	B-Side Inputs or 3-State Outputs
11	V <sub>CCB</sub>	B-Side Power Supply
12	OE	Output Enable Input

## FUNCTIONAL DIAGRAM

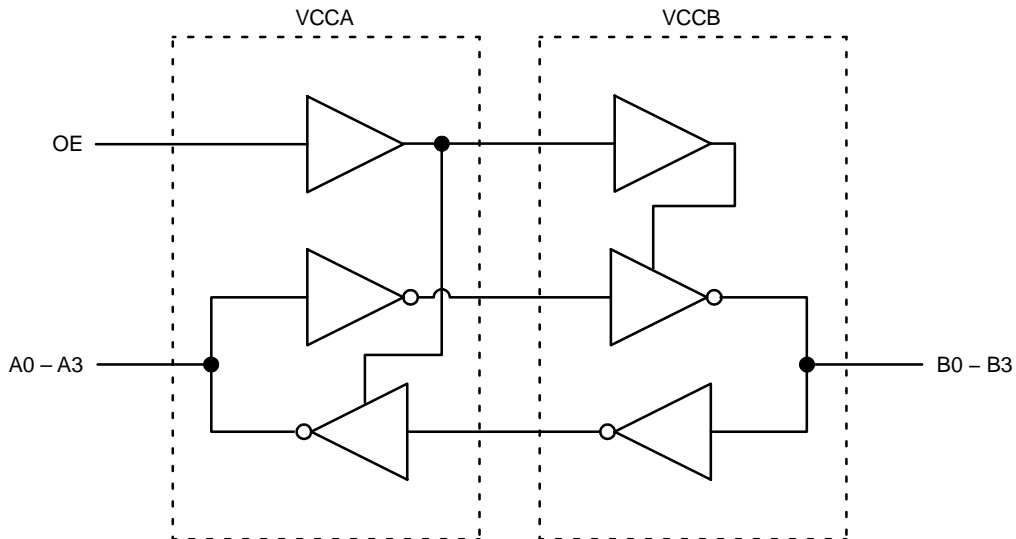


Figure 1. Functional Diagram

## FUNCTION TABLE

Control	Outputs
OE	
LOW Logic Level	3-State
High Logic Level	Normal Operation

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Condition	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	V <sub>CCA</sub>	-0.5	4.6	V
		V <sub>CCB</sub>	-0.5	4.6	
V <sub>I</sub>	DC Input Voltage	I/O Ports A and B	-0.5	4.6	V
		Control Input (OE)	-0.5	4.6	
V <sub>O</sub>	Output Voltage (Note 2)	Output 3-State	-0.5	4.6	V
		Output Active (A <sub>n</sub> )	-0.5	V <sub>CCA</sub> + 0.5	
		Output Active (B <sub>n</sub> )	-0.5	V <sub>CCB</sub> + 0.5	
I <sub>IK</sub>	DC Input Diode Current	V <sub>IN</sub> < 0 V	-	-50	mA
I <sub>OK</sub>	DC Output Diode Current	V <sub>O</sub> < 0 V, V <sub>O</sub> > V <sub>CC</sub>	-	±50	mA
I <sub>OH</sub> /I <sub>OL</sub>	DC Output Source/Sink Current		-	±50	mA
I <sub>CC</sub>	DC V <sub>CC</sub> or Ground Current (per Supply Pin)		-	±100	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
P <sub>D</sub>	Power Dissipation		-	17	mW
ESD	Electrostatic Discharge Capability	Human Body Model (per JESD22-A114 & Mil Std 883e 3015.7)	-	6	kV
		Charged Device Model (per ESD STM 5.3)	-	2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I<sub>O</sub> absolute maximum ratings must be observed.
2. All unused inputs and input/outputs must be held at V<sub>CCi</sub> or GND.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Condition	Min	Max	Unit
V <sub>CC</sub>	Power Supply	Operating V <sub>CCA</sub> or V <sub>CCB</sub>	1.1	3.6	V
V <sub>IN</sub>	Input Voltage	Ports A and B	0	V <sub>CCA</sub>	V
		Control Input (OE)	0	3.6	V
T <sub>A</sub>	Operating Temperature, Free Air		-40	+85	°C
dt/dV	Minimum Input Edge Rate	V <sub>CCA/B</sub> = 1.1 to 3.6 V	-	10	ns/V
θ <sub>JA</sub>	Thermal Resistance: Junction-to-Ambient		-	300	°C/W
θ <sub>JC</sub>	Thermal Resistance: Junction-to-Case		-	165	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**POWER-UP/POWER-DOWN SEQUENCE**

FXL translators offer an advantage in that either V<sub>CC</sub> may be powered up first. This benefit derives from the chip design. When either V<sub>CC</sub> is at 0 V, outputs are in a high-impedance state. The control input (OE) is designed to track the V<sub>CCA</sub> supply.

The recommended power-up sequence is:

1. Apply power to the first V<sub>CC</sub>.
2. Apply power to the second V<sub>CC</sub>.
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either V<sub>CC</sub>.
3. Remove power from other V<sub>CC</sub>.

**PULL-UP/PULL-DOWN RESISTORS**

*Do not use pull-up or pull-down resistors.* This device has bus-hold circuits: pull-up or pull-down resistors are not recommended because they interfere with the output state. The current through these resistors may exceed the hold drive, I<sub>I(HOLD)</sub> and/or I<sub>I(OD)</sub> bus-hold currents, resulting in data transition and/or auto-direction sensing failures. The bus-hold feature eliminates the need for extra resistors.

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## DC CHARACTERISTICS (T<sub>A</sub> = -40 to 85°C)

Symbol	Parameter	Condition	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Min	Typ	Max	Unit
V <sub>IHA</sub>	High-Level Input Voltage	Data Inputs A <sub>n</sub> Control Pin OE	2.70 to 3.60	1.10 to 3.60	2.00	-	-	V
			2.30 to 2.70		1.60	-	-	
			1.65 to 2.30		.65 x V <sub>CCA</sub>	-	-	
			1.40 to 1.65		.65 x V <sub>CCA</sub>	-	-	
			1.10 to 1.40		.90 x V <sub>CCA</sub>	-	-	
V <sub>IHB</sub>		Data Inputs B <sub>n</sub>	1.10 to 3.60	2.70 to 3.60	2.00	-	-	V
			2.30 to 2.70		1.60	-	-	
			1.65 to 2.30		.65 x V <sub>CCB</sub>	-	-	
			1.40 to 1.65		.65 x V <sub>CCB</sub>	-	-	
			1.10 to 1.40		.90 x V <sub>CCB</sub>	-	-	
V <sub>ILA</sub>	Low-Level Input Voltage	Data Inputs A <sub>n</sub> Control Pin OE	2.70 to 3.60	1.10 to 3.60	-	-	.80	V
			2.30 to 2.70		-	-	.70	
			1.65 to 2.30		-	-	.35 x V <sub>CCA</sub>	
			1.40 to 1.65		-	-	.35 x V <sub>CCA</sub>	
			1.10 to 1.40		-	-	.10 x V <sub>CCA</sub>	
V <sub>ILB</sub>		Data Inputs B <sub>n</sub>	1.10 to 3.60	2.70 to 3.60	-	-	.80	V
			2.30 to 2.70		-	-	.70	
			1.65 to 2.30		-	-	.35 x V <sub>CCB</sub>	
			1.40 to 1.65		-	-	.35 x V <sub>CCB</sub>	
			1.10 to 1.40		-	-	.10 x V <sub>CCB</sub>	
V <sub>OHA</sub>	High-Level Output Voltage (Note 3)	I <sub>OH</sub> = -4 μA	1.10 to 3.60	1.10 to 3.60	V <sub>CCA</sub> - .4	-	-	V
V <sub>OHB</sub>		I <sub>OH</sub> = -4 μA	1.10 to 3.60	1.10 to 3.60	V <sub>CCB</sub> - .4	-	-	
V <sub>OLA</sub>	Low-Level Output Voltage (Note 3)	I <sub>OL</sub> = 4 μA	1.10 to 3.60	1.10 to 3.60	-	-	.4	V
V <sub>OLB</sub>		I <sub>OL</sub> = 4 μA	1.10 to 3.60	1.10 to 3.60	-	-	.4	
I <sub>I(HOLD)</sub>	Bus-Hold Input Minimum Drive Current	V <sub>IN</sub> = 0.8 V	3.00	3.00	75.0	-	-	μA
		V <sub>IN</sub> = 2.0 V	3.00	3.00	-75.0	-	-	
		V <sub>IN</sub> = 0.7 V	2.30	2.30	45.0	-	-	
		V <sub>IN</sub> = 1.6 V	2.30	2.30	-45.0	-	-	
		V <sub>IN</sub> = 0.57 V	1.65	1.65	25.0	-	-	
		V <sub>IN</sub> = 1.07 V	1.65	1.65	-25.0	-	-	
		V <sub>IN</sub> = 0.49 V	1.40	1.40	11.0	-	-	
		V <sub>IN</sub> = .91 V	1.40	1.40	-11.0	-	-	
		V <sub>IN</sub> = 0.11 V	1.10	1.10	-	4.0	-	
		V <sub>IN</sub> = 0.99 V	1.10	1.10	-	-4.0	-	
I <sub>I(ODH)</sub>	Bus-Hold Input Overdrive High Current (Note 4)	Data Inputs A <sub>n</sub> , B <sub>n</sub>	3.60	3.60	450.0	-	-	μA
			2.70	2.70	300.0	-	-	
			1.95	1.95	200.0	-	-	
			1.60	1.60	120.0	-	-	
			1.40	1.40	80.0	-	-	

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## DC CHARACTERISTICS (T<sub>A</sub> = -40 to 85°C) (continued)

Symbol	Parameter	Condition	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Min	Typ	Max	Unit
I <sub>I(ODL)</sub>	Bus-Hold Input Overdrive Low Current (Note 5)	Data Inputs A <sub>n</sub> , B <sub>n</sub>	3.60	3.60	-450.0	-	-	μA
			2.70	2.70	-300.0	-	-	
			1.95	1.95	-200.0	-	-	
			1.60	1.60	-120.0	-	-	
			1.40	1.40	-80.0	-	-	
I <sub>I</sub>	Input Leakage Current	Control Inputs OE, V <sub>I</sub> = V <sub>CCA</sub> or GND	1.10 to 3.60	3.60	-	-	±1.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	A <sub>n</sub> V <sub>O</sub> = 0 V to 3.6 V	0	3.60	-	-	±2.0	μA
		B <sub>n</sub> V <sub>O</sub> = 0 V to 3.6 V	3.60	0	-	-	±2.0	
I <sub>OZ</sub>	3-State Output Leakage	A <sub>n</sub> , B <sub>n</sub> V <sub>O</sub> = 0 V or 3.6 V, OE = V <sub>IL</sub>	3.60	3.60	-	-	±5.0	μA
		A <sub>n</sub> V <sub>O</sub> = 0 V or 3.6 V, OE = V <sub>CCA</sub>	3.60	0	-	-	±5.0	
		B <sub>n</sub> V <sub>O</sub> = 0 V or 3.6 V, OE = 3.6 V	0	3.60	-	-	±5.0	
I <sub>CCA/B</sub>	Quiescent Supply Current (Note 6, 7)	V <sub>I</sub> = V <sub>CCI</sub> or GND; I <sub>O</sub> = 0, OE = V <sub>IH</sub>	1.10 to 3.60	1.10 to 3.60	-	-	10.0	μA
I <sub>CCZ</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND; I <sub>O</sub> = 0, OE = GND	1.10 to 3.60	1.10 to 3.60	-	-	10.0	μA
I <sub>CCA</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCB</sub> or GND; I <sub>O</sub> = 0, B-to-A Direction; OE = V <sub>IH</sub>	0	1.10 to 3.60	-	-	-10.0	μA
		V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, A-to-B Direction	1.10 to 3.60	0	-	-	10.0	
I <sub>CCB</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, A-to-B Direction, OE = V <sub>IH</sub>	1.10 to 3.60	0	-	-	-10.0	μA
		V <sub>I</sub> = V <sub>CCB</sub> or GND; I <sub>O</sub> = 0, B-to-A Direction	0	1.10 to 3.60	-	-	10.0	

3. This is the output voltage for static conditions. Dynamic drive specifications are given in the Dynamic Output Electrical Characteristics table.

4. An external drive must source at least the specified current to switch LOW-to-HIGH.

5. An external drive must source at least the specified current to switch HIGH-to-LOW.

6. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input side.

7. Reflects current per supply, V<sub>CCA</sub> or V<sub>CCB</sub>.

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## DYNAMIC OUTPUT ELECTRICAL CHARACTERISTIC

Symbol	Parameter	V <sub>CCB</sub> = 3.0 V to 3.6 V		V <sub>CCB</sub> = 2.3 V to 2.7 V		V <sub>CCB</sub> = 1.65 V to 1.95 V		V <sub>CCB</sub> = 1.4 V to 1.6 V		V <sub>CCB</sub> = 1.1 V to 1.3 V	Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	

### A PORT (A<sub>n</sub>)

OUTPUT LOAD: C<sub>L</sub> = 15 pF, R<sub>L</sub> ≥ 1 MΩ (C<sub>I/O</sub> = 4 pF), T<sub>A</sub> = -40 to 85°C

t <sub>rise</sub>	Output Rise Time A Port (Note 9)	-	3.0	-	3.5	-	4.0	-	5.0	7.5	ns
t <sub>fall</sub>	Output Fall Time A Port (Note 10)	-	3.0	-	3.5	-	4.0	-	5.0	7.5	ns
I <sub>OHD</sub>	Dynamic Output Current High (Note 9)	-11.4	-	-7.5	-	-4.7	-	-3.2	-	-1.7	mA
I <sub>OLD</sub>	Dynamic Output Current Low (Note 10)	+11.4	-	+7.5	-	+4.7	-	+3.2	-	+1.7	mA

### B PORT (B<sub>n</sub>)

OUTPUT LOAD: C<sub>L</sub> = 15 pF, R<sub>L</sub> ≥ 1 MΩ (C<sub>I/O</sub> = 5 pF), T<sub>A</sub> = -40 to 85°C

t <sub>rise</sub>	Output Rise Time B Port (Note 9)	-	3.0	-	3.5	-	4.0	-	5.0	7.5	ns
t <sub>fall</sub>	Output Fall Time B Port (Note 10)	-	3.0	-	3.5	-	4.0	-	5.0	7.5	ns
I <sub>OHD</sub>	Dynamic Output Current High (Note 9)	-12.0	-	-7.9	-	-5.0	-	-3.4	-	-1.8	mA
I <sub>OLD</sub>	Dynamic Output Current Port (Note 10)	+12.0	-	+7.9	-	+5.0	-	+3.4	-	+1.8	mA

8. Dynamic output characteristics are guaranteed, but not tested.

9. See Figure 6.

10. See Figure 7.

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## AC CHARACTERISTICS

Symbol	Parameter	V <sub>CCB</sub> = 3.0 V to 3.6 V		V <sub>CCB</sub> = 2.3 V to 2.7 V		V <sub>CCB</sub> = 1.65 V to 1.95 V		V <sub>CCB</sub> = 1.4 V to 1.6 V		V <sub>CCB</sub> = 1.1 V to 1.3 V	Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	

V<sub>CCA</sub> = 3.0 V to 3.6 V, T<sub>A</sub> = -40 to 85°C

t <sub>PLH</sub> , t <sub>PHL</sub>	A to B	0.2	4.0	0.3	4.2	0.5	5.4	0.6	6.8	6.9	ns
	B to A	0.2	4.0	0.2	4.1	0.3	5.0	0.5	6.0	4.5	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	OE to A, OE to B	–	1.7	–	1.7	–	1.7	–	1.7	1.7	μs
t <sub>SKEW</sub>	A Port, B Port (Note 11)	–	0.5	–	0.5	–	0.5	–	1.0	1.0	ns

V<sub>CCA</sub> = 2.3 V to 2.7 V, T<sub>A</sub> = -40 to 85°C

t <sub>PLH</sub> , t <sub>PHL</sub>	A to B	0.2	4.1	0.4	4.5	0.5	5.6	0.8	6.9	7.0	ns
	B to A	0.3	4.2	0.4	4.5	0.5	5.5	0.5	6.5	4.8	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	OE to A, OE to B	–	1.7	–	1.7	–	1.7	–	1.7	1.7	μs
t <sub>SKEW</sub>	A Port, B Port (Note 11)	–	0.5	–	0.5	–	0.5	–	1.0	1.0	ns

V<sub>CCA</sub> = 1.65 V to 1.95 V, T<sub>A</sub> = -40 to 85°C

t <sub>PLH</sub> , t <sub>PHL</sub>	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	7.5	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	5.4	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	OE to A, OE to B	–	1.7	–	1.7	–	1.7	–	1.7	1.7	μs
t <sub>SKEW</sub>	A Port, B Port (Note 11)	–	0.5	–	0.5	–	0.5	–	1.0	1.0	ns

V<sub>CCA</sub> = 1.4 V to 1.6 V, T<sub>A</sub> = -40 to 85°C

t <sub>PLH</sub> , t <sub>PHL</sub>	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	7.9	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	6.1	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	OE to A, OE to B	–	1.7	–	1.7	–	1.7	–	1.7	1.7	μs
t <sub>SKEW</sub>	A Port, B Port (Note 11)	–	1.0	–	1.0	–	1.0	–	1.0	1.0	ns
		Typ		Typ		Typ		Typ		Typ	

V<sub>CCA</sub> = 1.1 V to 1.3 V, T<sub>A</sub> = -40 to 85°C

t <sub>PLH</sub> , t <sub>PHL</sub>	A to B	4.6	4.8	5.4	6.2	9.2	ns
	B to A	6.8	7.0	7.4	7.8	9.1	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	OE to A, OE to B	1.7	1.7	1.7	1.7	1.7	μs
t <sub>SKEW</sub>	A Port, B Port (Note 11)	1.0	1.0	1.0	1.0	1.0	ns

11. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A<sub>n</sub> or B<sub>n</sub>) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 9). Skew is guaranteed, but not tested.

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## MAXIMUM DATA RATE ( $T_A = -40$ to $85^\circ\text{C}$ ) (Note 12, 13)

$V_{CCA}$	$V_{CCB} = 3.0\text{ V}$ to $3.6\text{ V}$	$V_{CCB} = 2.3\text{ V}$ to $2.7\text{ V}$	$V_{CCB} = 1.65\text{ V}$ to $1.95\text{ V}$	$V_{CCB} = 1.4\text{ V}$ to $1.6\text{ V}$	$V_{CCB} = 1.1\text{ V}$ to $1.3\text{ V}$	Unit
	Min	Min	Min	Min	Typ	
$V_{CCA} = 3.00$ to $3.60\text{ V}$	140	120	100	80	40	Mbps
$V_{CCA} = 2.30$ to $2.70\text{ V}$	120	120	100	80	40	Mbps
$V_{CCA} = 1.65$ to $1.95\text{ V}$	100	100	80	60	40	Mbps
$V_{CCA} = 1.40$ to $1.60\text{ V}$	80	80	60	60	40	Mbps
	Typ	Typ	Typ	Typ	Typ	
$V_{CCA} = 1.10$ to $1.30\text{ V}$	40	40	40	40	40	Mbps

12. Maximum data rate is guaranteed, but not tested.

13. Maximum data rate is specified in megabits per second (see Figure 8). It is equivalent to two times the F–toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50 MHz.

## CAPACITANCE

Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$ Typical	Unit	
$C_{IN}$	Input Capacitance Control Pin (OE)	$V_{CCA} = V_{CCB} = \text{GND}$	3	pF	
$C_{I/O}$	Input/Output Capacitance	$V_{CCA} = V_{CCB} = 3.3\text{ V}$ , OE = GND	$A_n$	4	pF
			$B_n$	5	
$C_{pd}$	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3\text{ V}$ , $V_I = 0\text{ V}$ or $V_{CC}$ , $f = 10\text{ MHz}$	25	pF	

## I/O Architecture Benefit

The FXLA0104 I/O architecture benefits the end user, beyond level translation, in the following three ways:

**Auto Direction** without an external direction pin.

**Drive Capacitive Loads.** Automatically shifts to a higher current drive mode only during “Dynamic Mode” or HL / LH transitions.

**Lower Power Consumption.** Automatically shifts to low–power mode during “Static Mode” (no transitions), lowering power consumption.

The FXLA0104 does not require a direction pin. Instead, the I/O architecture detects input transitions on both side and automatically transfers the data to the corresponding output. For example, for a given channel, if both A and B side are at a static LOW, the direction has been established as  $A \rightarrow B$ , and a LH transition occurs on the B port; the FXLA0104 internal I/O architecture automatically changes direction from  $A \rightarrow B$  to  $B \rightarrow A$ .

During HL / LH transitions, or “Dynamic Mode,” a strong output driver drives the output channel in parallel with a weak output driver. After a typical delay of approximately 10 ns – 50 ns, the strong driver is turned off, leaving the weak driver enabled for holding the logic state of the channel. This weak driver is called the “bus hold.” “Static Mode” is when

only the bus hold drives the channel. The bus hold can be overridden in the event of a direction change. The strong driver allows the FXLA0104 to quickly charge and discharge capacitive transmission lines during dynamic mode. Static mode conserves power, where  $I_{CC}$  is typically  $<5\ \mu\text{A}$ .

## Bus Hold Minimum Drive Current

Specifies the minimum amount of current the bus hold driver can source/sink. The bus hold minimum drive current ( $I_{IHOLD}$ ) is  $V_{CC}$  dependent and guaranteed in the DC Electrical tables. The intent is to maintain a valid output state in a static mode, but that can be overridden when an input data transition occurs.

## Bus Hold Input Overdrive Drive Current

Specifies the minimum amount of current required (by an external device) to overdrive the bus hold in the event of a direction change. The bus hold overdrive ( $I_{IODH}$ ,  $I_{IOLD}$ ) is  $V_{CC}$  dependent and guaranteed in the DC Electrical tables.

## Dynamic Output Current

The strength of the output driver during LH / HL transitions is referenced on page 6, *Dynamic Output Electrical Characteristics*,  $I_{OHD}$ , and  $I_{OLD}$ .



# FXLA0104

## Test Diagrams

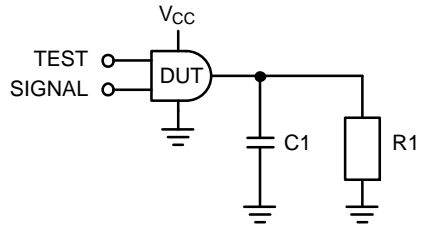


Figure 2. Test Circuit

Table 1. AC TEST CONDITIONS

Test	Input Signal	Output Enable Control
$t_{PLH}$ , $t_{PHL}$	Data Pulses	$V_{CCA}$
$t_{PZL}$	0 V	LOW to HIGH Switch
$t_{PZH}$	$V_{CCI}$	LOW to HIGH Switch

Table 2. AC LOAD

$V_{CCo}$	C1	R1
1.2 V $\pm$ 0.1 V	15 pF	1 M $\Omega$
1.5 V $\pm$ 0.1 V	15 pF	1 M $\Omega$
1.8 V $\pm$ 0.15 V	15 pF	1 M $\Omega$
2.5 V $\pm$ 0.2 V	15 pF	1 M $\Omega$
3.3 V $\pm$ 0.3 V	15 pF	1 M $\Omega$

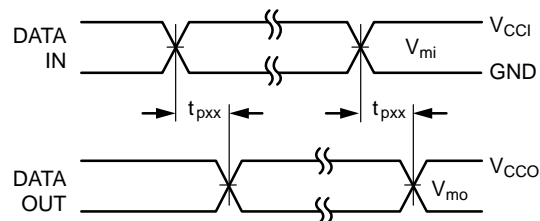
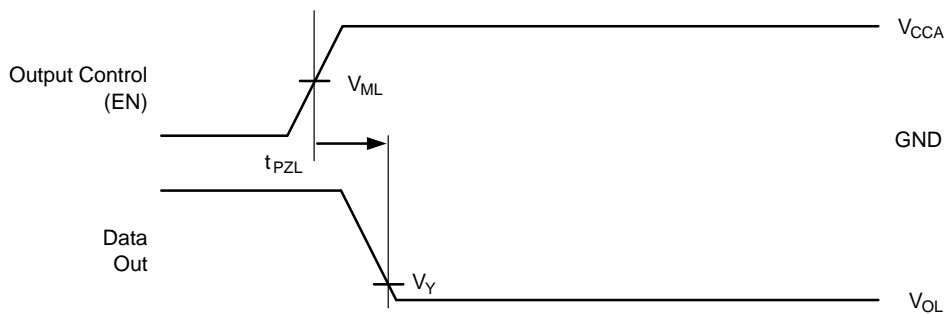


Figure 3. Waveform for Inverting and Non-Inverting Functions

NOTES:

- 14. Input  $t_R = t_F = 2.0$  ns, 10% to 90%.
- 15. Input  $t_R = t_F = 2.5$  ns, 10% to 90%, at  $V_I = 3.0$  V to 3.6 V only.

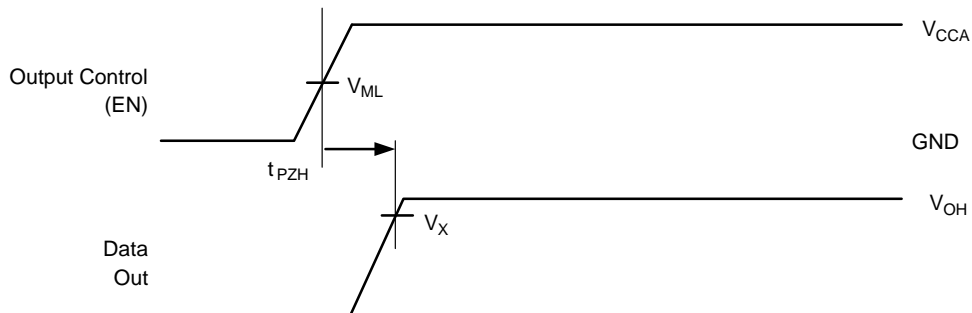
# FXLA0104



**Figure 4. 3-State Output Low Enable**

**NOTES:**

- 16. Input  $t_R = t_F = 2.0$  ns, 10% to 90%.
- 17. Input  $t_R = t_F = 2.5$  ns, 10% to 90%, at  $V_I = 3.0$  V to 3.6 V only.



**Figure 5. 3-State Output High Enable**

**NOTES:**

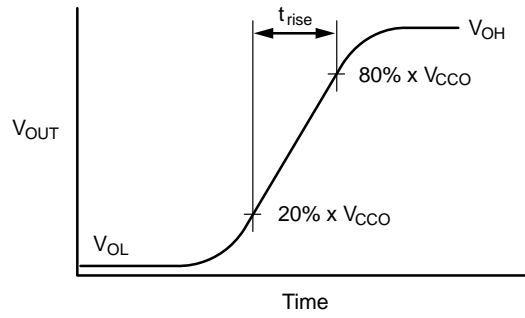
- 18. Input  $t_R = t_F = 2.0$  ns, 10% to 90%.
- 19. Input  $t_R = t_F = 2.5$  ns, 10% to 90%, at  $V_I = 3.0$  V to 3.6 V only.

**Table 3. TEST MEASURE POINTS**

Symbol	V <sub>DD</sub>
V <sub>MI</sub> (Note 20)	V <sub>CCI</sub> / 2
V <sub>MO</sub>	V <sub>CC0</sub> / 2
V <sub>X</sub>	0.9 x V <sub>CC0</sub>
V <sub>Y</sub>	0.1 x V <sub>CC0</sub>

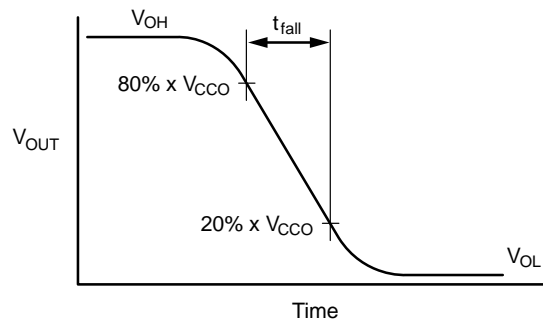
20. V<sub>CCI</sub> = V<sub>CCA</sub> for control pin OE or V<sub>MI</sub> (V<sub>CCA</sub> / 2).

# FXLA0104



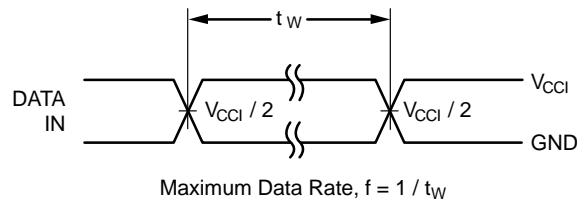
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \cdot V_{CCO}}{t_{RISE}}$$

**Figure 6. Active Output Rise Time and Dynamic Output Current High**

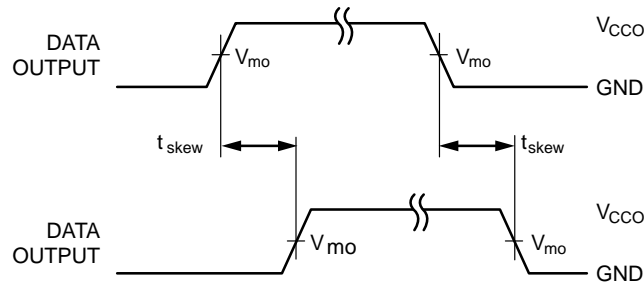


$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \cdot V_{CCO}}{t_{FALL}}$$

**Figure 7. Active Output Fall Time and Dynamic Output Current Low**



**Figure 8. Maximum Data Rate**



**Figure 9. Output Skew Time**

**NOTES:**

21.  $t_{SKEW} = (t_{pHLmax} - t_{pHLmin})$  or  $(t_{pLHmax} - t_{pLHmin})$

# FXLA0104

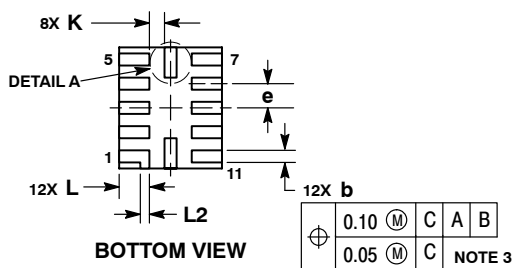
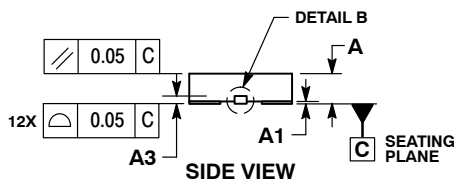
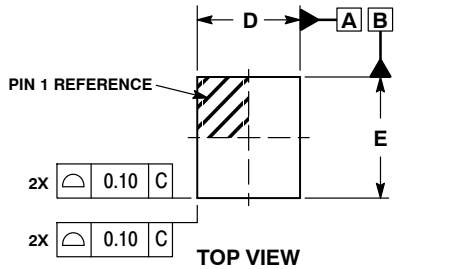
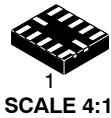
## ORDERING INFORMATION

Part Number	Operating Temperature Range	Top Mark	Package	Shipping <sup>†</sup>
FXLA0104QFX	-40 to 85°C	XU	12-Lead, 1.7 mm x 2.0 mm Ultrathin Molded Leadless Package (UMLP) (Pb-Free, Halide Free)	5000 Units / Tape & Reel

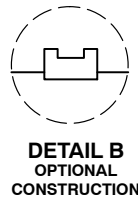
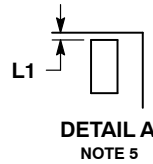
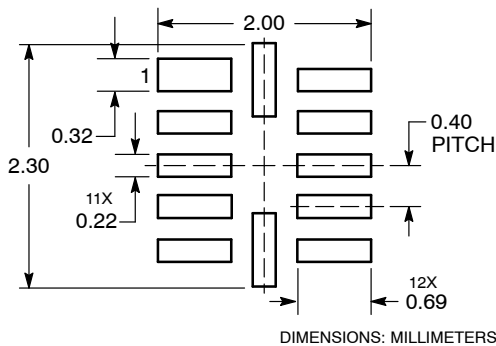
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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CASE 523AE  
ISSUE A

DATE 11 JUN 2007



**MOUNTING FOOTPRINT**  
**SOLDERMASK DEFINED**

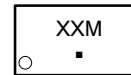


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

**GENERIC MARKING DIAGRAM\***



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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