

Schottky Rectifier

20 A, 50 V Ultra-Low VF

FSV2050V

Features

- Ultra Low Forward Voltage Drop
- Low Thermal Resistance
- Very Low Profile: Typical Height of 1.1 mm
- Green Molding Compound as per IEC61249 Standard
- Non-DAP Option Only
- Qualified with Reflow (J-STD-020) and Solder Temperature 260°C Classification
- Lead Free in Compliance with EU RoHS 2011/65/EU Directive
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

Specifications

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

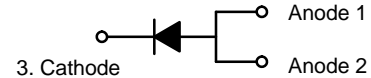
Symbol	Parameter	Value	Unit
V_{RRM}	Peak Repetitive Reverse Voltage	50	V
V_{RWM}	Working Peak Reverse Voltage	50	V
V_{RMS}	RMS Reverse Voltage	35	V
V_R	DC Blocking Voltage	50	V
$I_{F(AV)}$	Average Rectified Peak Forward Surge Current	20	A
I_{FSM}	Non-Repetitive Peak Forward Surge Current	320	A
T_J	Operating Junction Temperature Range	-55 to +150	°C
T_{STG}	Storage Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

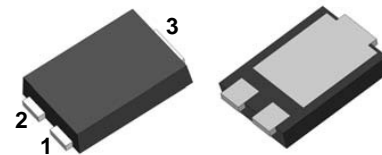


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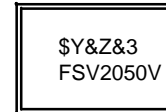


Schottky Rectifier



TO-277-3LD
CASE 340BQ

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Date Code (Year & Week)
FSV2050V = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FSV2050V

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Note 1)

Symbol	Characteristic	Minimum Land Pattern	Maximum Land Pattern	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	100	40	$^\circ\text{C/W}$
Ψ_{JL}	Junction-to-Lead Thermal Characteristics, Thermocouple Soldered to Anode	15	12	$^\circ\text{C/W}$
	Junction-to-Lead Thermal Characteristics, Thermocouple Soldered to Cathode	6	5	

1. The thermal resistances ($R_{\theta JA}$ & Ψ_{JL}) are characterized with device mounted on the following FR4 printed circuit boards, as shown in Figure 1 and Figure 2. PCB size: 76.2 x 114.3 mm. Minimum land pattern size: 4.9 x 4.8 mm (big pattern, x1), 1.4 x 1.52 mm (small pattern, x2). Maximum land pattern size: 30 x 30 mm (pattern, x2). Force line trace size = 55 mils, sense line trace size = 4 mils.



Figure 1. Minimum Land Pattern of 2 oz Copper

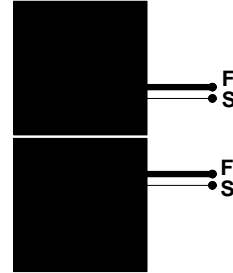


Figure 2. Maximum Land Pattern of 2 oz Copper

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_R	Breakdown Voltage	$I_R = 500 \mu\text{A}$	50	55.3	–	V
V_F	Forward Voltage Drop	$I_F = 20 \text{ A}$	–	485	550	mV
I_R	Reverse Current	$V_R = 50 \text{ V}$	–	60.3	320	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping†
FSV2050V	FSV2050V	TO-277-3LD (Pb-Free/Halogen Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FSV2050V

TYPICAL PERFORMANCE CHARACTERISTICS

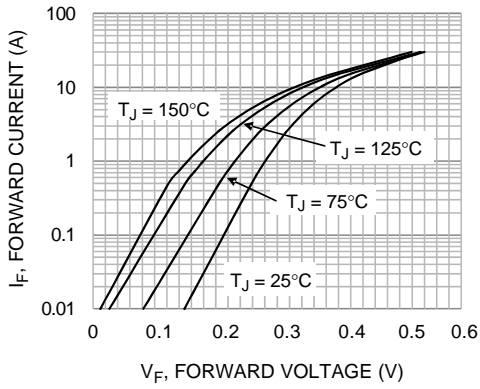


Figure 3. Typical Forward Characteristics

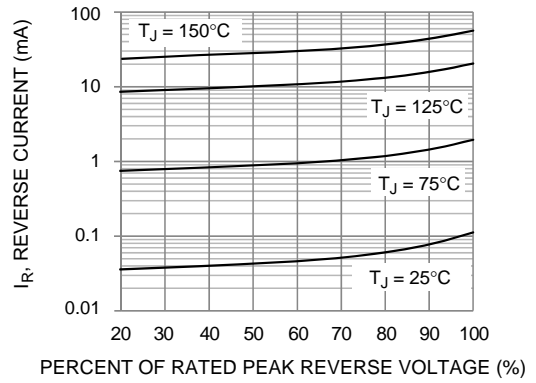


Figure 4. Typical Reverse Characteristics

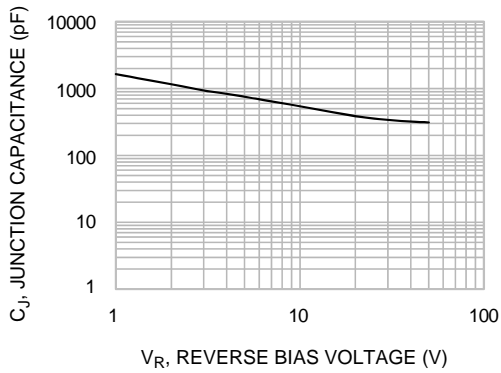


Figure 5. Typical Junction Capacitance

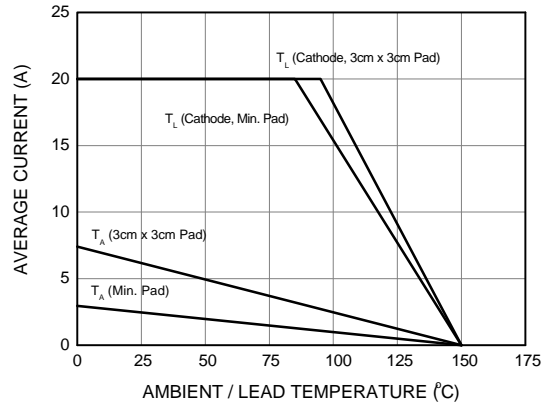


Figure 6. Forward Current Derating Curve

MECHANICAL CASE OUTLINE

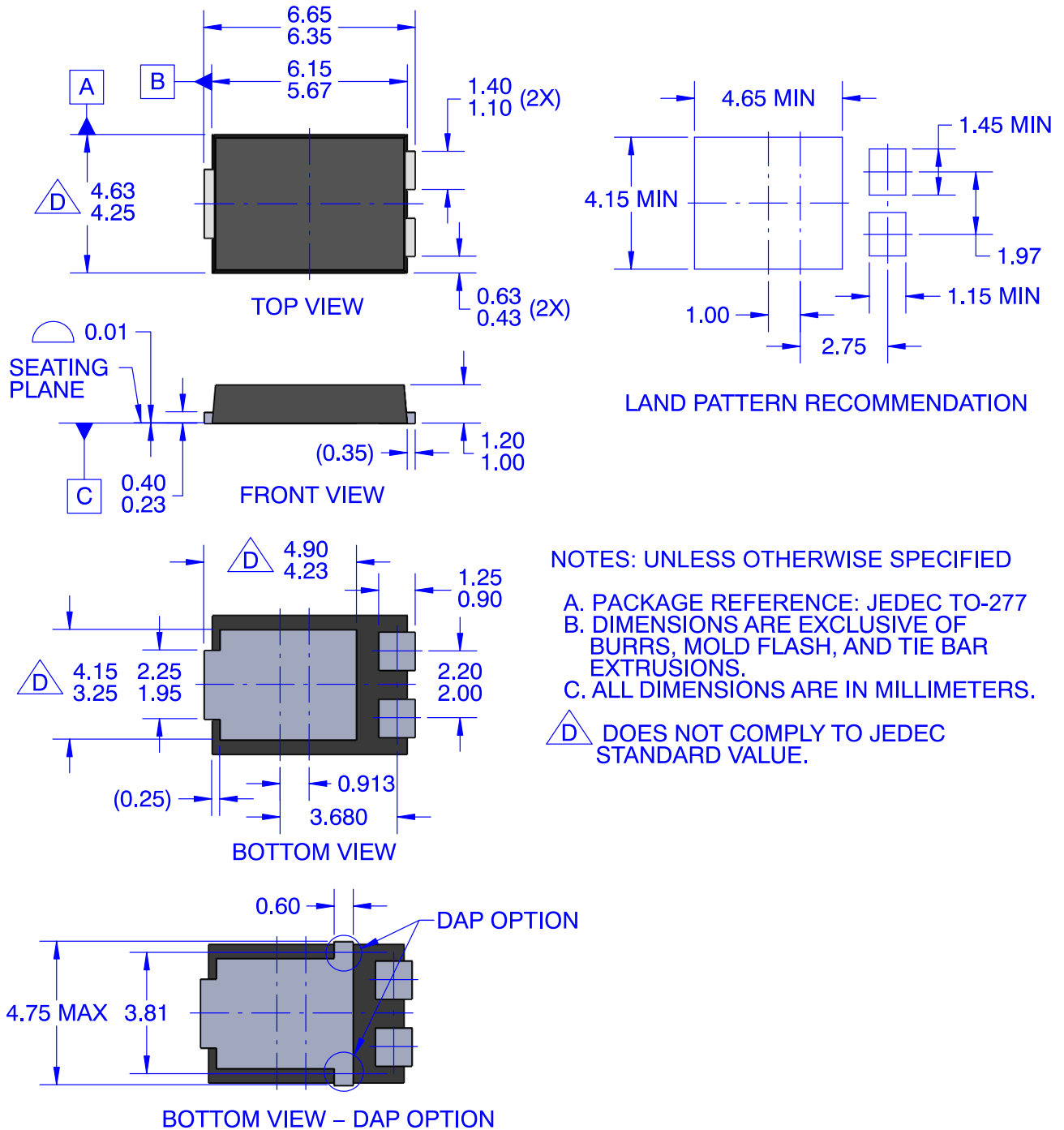
PACKAGE DIMENSIONS

ON Semiconductor®



TO-277-3LD
CASE 340BQ
ISSUE O

DATE 30 SEP 2016



NOTES: UNLESS OTHERWISE SPECIFIED

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- D. DOES NOT COMPLY TO JEDEC STANDARD VALUE.

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