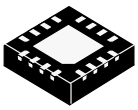
4:1 High-Speed USB Multiplexer/Switch

FSUSB74

WQFN 16 3X3, 0.5P
CASE 510BS



UQFN 16 1.8X2.6, 0.6P
CASE 523BF

Description

The FSUSB74 is a Bi−directional, Low−Power, High−Speed USB 2.0 4:1 MUX. It is Optimized for Switching from four High−Speed (480Mbps) sources or any combination of High−Speed and full−/low−speed USB/UART sources to one USB 2.0 connector.

Applications

- MP3 Portable Media Players
- Cellular Phones, Smart Phones
- Netbooks, Mobile Internet Devices (MID)

Related Resources

- FSUSB74 Demonstration Board
- FSUSB74 Evaluation Board

Features

Switch Type	4:1
USB	USB 2.0 High−Speed Compliant USB 2.0 Full−Speed Compliant
R_{ON}	6.5 Ω
C_{ON}	7.5 pF
ESD (IEC61000−4−2)	15 kV (Air) 8 kV (Contact)
V_{CC}	2.7 to 4.4 V
I_{CCSLP}	<1 μA
I_{CCACT}	9 μA
Package	16− Lead UMLP 1.80 x 2.60 x 0.55mm, 0.40mm Pitch 16−Lead MLP 3 x 3 x 0.7mm, 0.5mm Pitch
Ordering Information	FSUSB74UMX (UMLP) FSUSB74MPX (MLP)

MARKING DIAGRAM

LC,FSUSB74 = Device Code
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Lot Traceability Code
FSUSB74 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FSUSB74MPX	WQFN−16 (Pb−Free)	3000 / Tape & Reel
FSUSB74UMX	UQFN−16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL APPLICATION

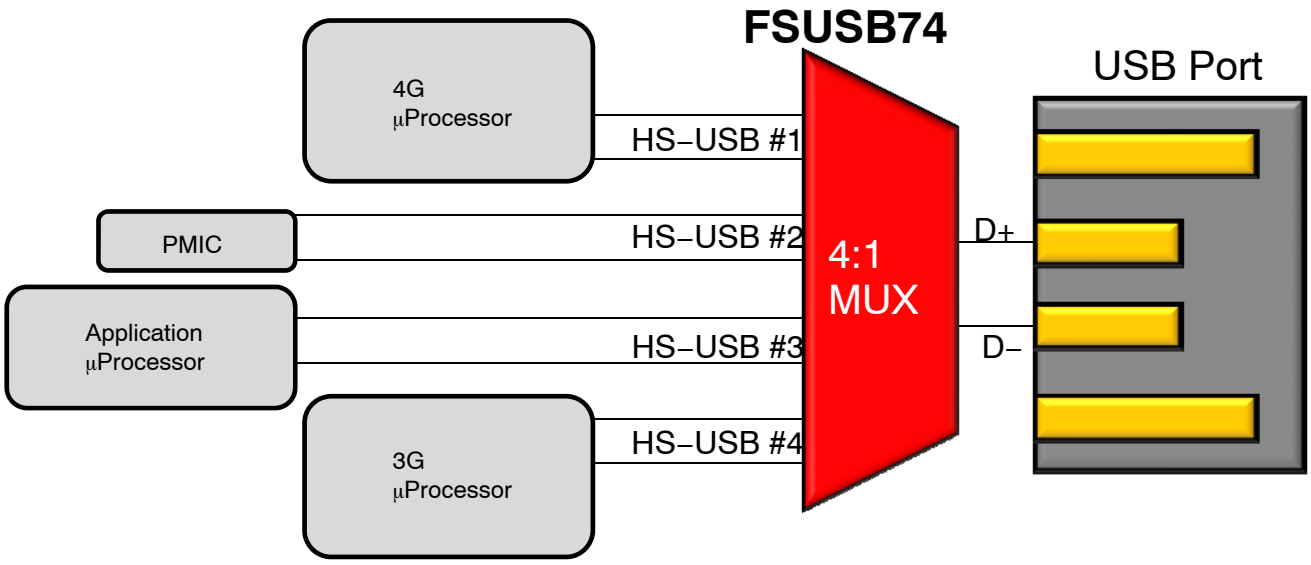


Figure 1. Mobile Phone Example

PIN CONFIGURATIONS

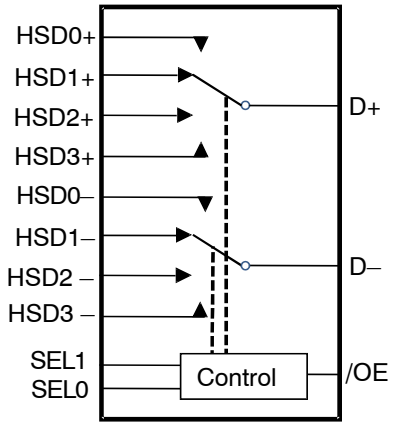


Figure 2. UMLP Analog Symbol

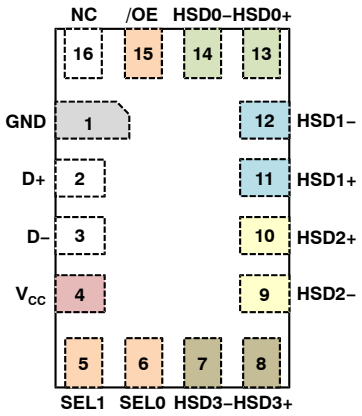


Figure 3. UMLP (Top View)

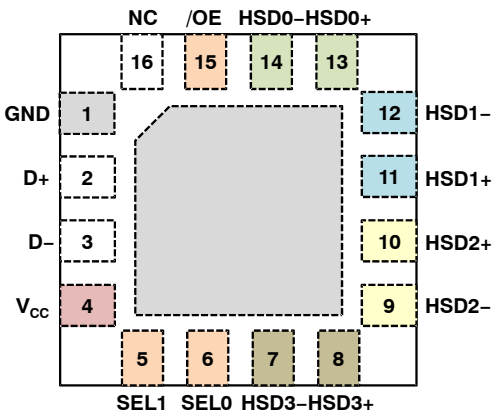


Figure 4. MLP (Top View)

PIN DESCRIPTIONS

Pin No.	Name	Type	Description
1	GND	Ground	Ground
2	D+	I/O	D+ common port (HS or FS USB)
3	D−	I/O	D− common port (HS or FS USB)
4	V_{CC}	Power Supply	Supply Voltage
5	SEL1	Input	Path Selection Control Input (see truth table below)
6	SEL0	Input	Path Selection Control Input (see truth table below)
7	HSD3−	I/O	D− from fourth source path (HS or FS USB)
8	HSD3+	I/O	D+ from fourth source path (HS or FS USB)
9	HSD2−	I/O	D− from third source path (HS or FS USB)
10	HSD2+	I/O	D+ from third source path (HS or FS USB)
11	HSD1+	I/O	D+ from second source path (HS or FS USB)
12	HSD1−	I/O	D− from second source path (HS or FS USB)
13	HSD0+	I/O	D+ from first source path (HS or FS USB)
14	HSD0−	I/O	D− from first source path (HS or FS USB)
15	/OE	Input	D− from first source path (HS or FS USB)
16	NC	−	No Connect

TRUTH TABLE

/OE	SEL1	SEL0	Function
1	**X**	**X**	D+, D- Switch Paths Open
0	0	0	D+ = HSD0 +, D- = HSD0-
0	0	1	D+ = HSD1+, D− = HSD1−
0	1	0	D+ = HSD2+, D− = HSD2−
0	1	1	D+ = HSD3+, D− = HSD3−

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		−0.5	5.25	V
V_{CNTRL}	DC Input Voltage (SEL1, SEL0, /OE, SELS)[1]		−0.50	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[1]		−0.50	5.25	V
I_{IK}	DC Input Diode Current		−50	−	mA
T_{STG}	Storage Temperature		−65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J−STD−020A)		−	1	Level
ESD	IEC61000−4−2 System on USB connector pins D+ & D−	Air Gap	15	−	kV
		Contact	8	−	
	Human Body Model, JEDEC: JESD22−A114	D+,D− to GND	6	−	
		Power to GND	12	−	
		All Other Pins	2	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	4.4	V
V_{CNTRL} (Note 2)	Control Input Voltage (SEL1, SEL0, /OE, and SELS)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	−0.5	4.4	V
T_A	Operating Temperature	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. The control input must be held HIGH or LOW; it must not float.

DC ELECTRICAL CHARACTERISTICS (All typical values are for V_{CC} = 3.3 V at 25°C unless otherwise specified.)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = −40°C to 85°C			Unit
				Min.	Typ.	Max.	
R_{ON} (Note 3)	HS Switch On Resistance	V_{SW} = 0.4 V, I_{ON} = −8 mA, Figure 5	3.3		6.5	9.0	Ω
ΔR_{ON} (Note 3)	HS Delta Ron (Note 4)	V_{SW} = 0.4 V, I_{ON} = −8 mA	3.3		0.5	0.5	Ω
I_{IN}	Control Input Leakage	All Combinations of /OE,SEL1 & SEL0 in the Truth Table (1 = V_{CC}, 0 = 0 V)	4.4	−1	–	–	μA
I_{OZ}	Off State Leakage	0 ≤ Dn, HSD0n, HSD1n, HSD2n, HSD3n ≤ 4.4 V	4.4	−1	–	–	μA
I_{OFF}	Power−Off Leakage Current (All I/O Ports)	V_{SW} = 0 V to 4.4 V, V_{CC} = 0 V, Figure 6	0	−1	–	–	μA
I_{CCSLP}	Sleep Mode Supply Current	/OE = V_{CC}	4.4	–	–	–	μA
I_{CCACT}	Active Mode Supply Current	All Active Modes in Truth Table	4.4	–	9	18	μA
I_{CCT}	Increase in I_{CC} Current per Control Input and V_{CC}	V_{CNTRL} = 1.8 V	4.4	–	3.3	4.0	μA
		V_{CNTRL} = 1.2 V	4.4	–	4.9	6.0	μA
V_{IK}	Clamp Diode Voltage	I_{IN} = −18 mA	2.5	–	–	−1.2	V
V_{IH}	Control Input Voltage High	SEL1, SEL0, /OE	2.5 to 4.4	1.0	–	–	V
V_{IL}	Control Input Voltage Low	SEL1, SEL0, /OE	2.5 to 4.4	–	–	0.35	V

3. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
4. Guaranteed by characterization.

AC ELECTRICAL CHARACTERISTICS (All typical values are for V_{CC} = 3.3 V at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = −40°C to 85°C			Unit
				Min.	Typ.	Max.	
t_{ON}	Turn−On Time when Switching from One USB Path (or Disabled i.e. /OE=1) to Another USB Path	R_L = 50 Ω, C_L = 35 pF, V_{SW} = 0.8 V, Figure 7, Figure 8	2.5 to 4.4	126	–	400	μs
t_{OFF}	Turn−Off Time, Turning Off Any of the USB Paths	R_L = 50 Ω, C_L = 35 pF, V_{SW} = 0.8 V, Figure 7, Figure 8	2.5 to 4.4	–	–	80	ns
t_{PD}	Propagation Delay (Note 5)	C_L = 5 pF, R_L = 50 Ω, Figure 7, Figure 9	3.3	–	0.25	–	ns
t_{RF}	Slow Turn−On/Off Switch Paths (Note 5)	C_L = 5 pF, Dn at 0 V or 3.6 V, 40.5 Ω in series with switch 10% to 90%	3.3	–	4.5	–	ns
t_{BBM}	Break−Before−Make Time (Note 5)	R_L = 50 Ω, C_L = 35 pF, V_{SW1} = V_{SW2} = 0.8 V, Figure 11	2.5 to 4.4	126	–	400	μs
O_{IRR}	Off Isolation (Note 5)	R_L = 50 Ω, f = 240MHz, Figure 13	2.5 to 4.4	–	−40	–	dB
X_{talk}	Channel−to−Channel Crosstalk (Note 5)	R_L = 50 Ω, f = 240MHz, Figure 14	2.5 to 4.4	–	−40	–	dB
$t_{SK(P)}$	Pulse Skew (Note 5)	V_{SW} = 0.2 V $diff_{PP}$, Figure 10, C_L = 5 pF	2.5 to 4.4	–	25	–	ps
$t_{SK(I)}$	Skew Between Differential Signals Within a Pair (Note 5)	V_{SW} = 0.2 V $diff_{PP}$, Figure 10, C_L = 5 pF	2.5 to 4.4	–	25	–	ps

5. Guaranteed by characterization.

CAPACITANCE CHARACTERISTICS (All typical values are for V_{CC} = 3.3 V at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Typical	Unit
C_{IN}	Input Capacitance (Note 6)		0	3	pF
C_{ON}	D+/D− On Capacitance (Note 6)	Any Switch Path Enabled, f = 1MHz, Figure 16	3.3	7.5	
C_{OFF}	HSD0n, HSD1n, HSD2n, HSD3n Off Capacitance (Note 6)	If V_{CC} = 3.3 V, then /OE = 3.3 V; f = 1MHz, Figure 15	0 or 3.3	2.2	

6. Guaranteed by characterization.

TEST DIAGRAMS

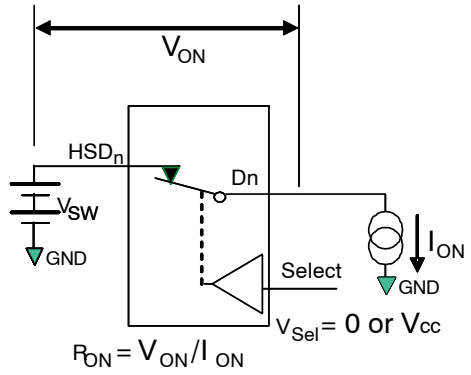
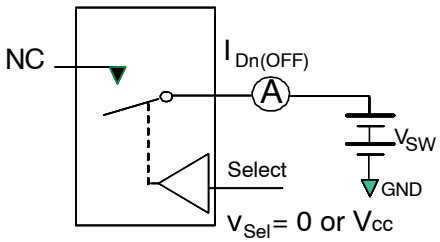
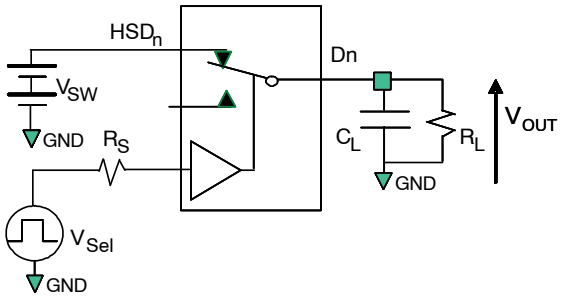


Figure 5. On Resistance



**Eachswitchportistestedseparately

Figure 6. Off Leakage



RL, RS, and CL are functions of the application environment (see AC Tables for specific values)
CL includes test fixture and stray capacitance.

Figure 7. AC Test Circuit Load

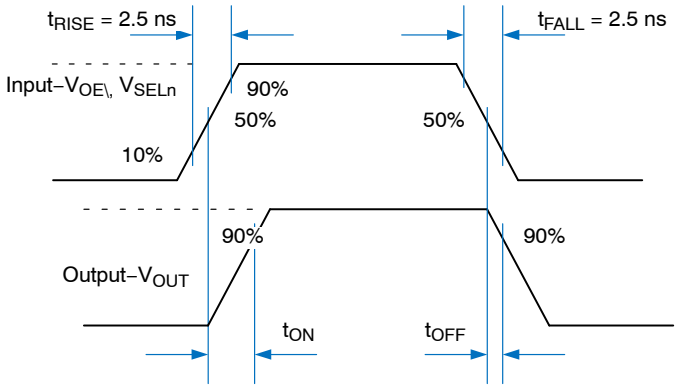


Figure 8. Turn–On / Turn–Off Waveforms

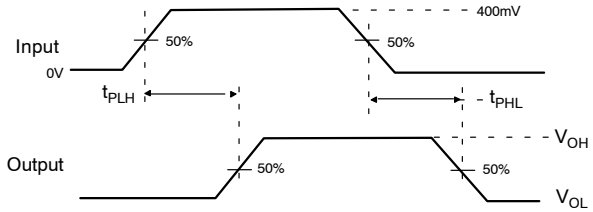


Figure 9. Propagation Delay (t_R t_F – 500 ps)

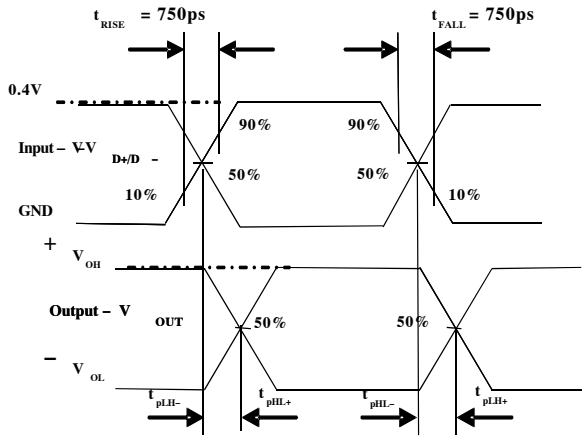
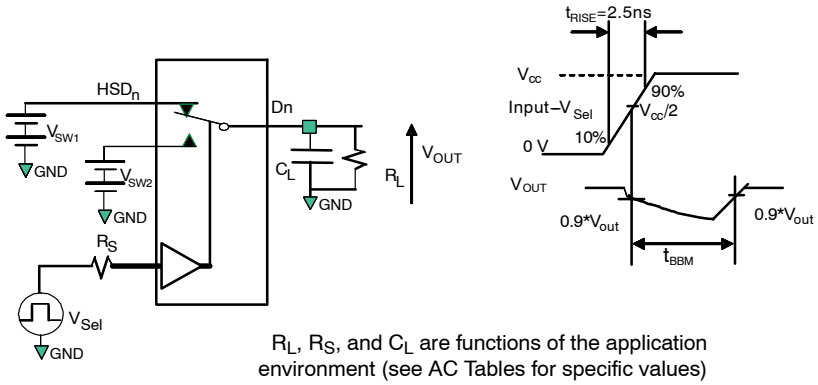


Figure 10. Skew Test Waveforms

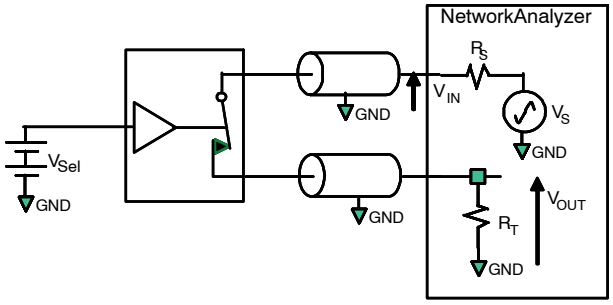
$t_{SK(P)} = |t_{PLH-} - t_{PHL-}|$ or $|t_{PLH+} - t_{PHL+}|$
$t_{SK(I)} = |t_{PLH-} - t_{PHL+}|$ or $|t_{PLH+} - t_{PHL-}|$

TEST DIAGRAMS



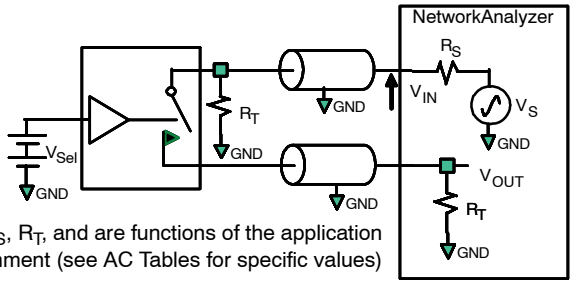
R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 11. Break−Before−Make Interval Timing



R_S, R_T, and are functions of the application environment (see AC Tables for specific values)

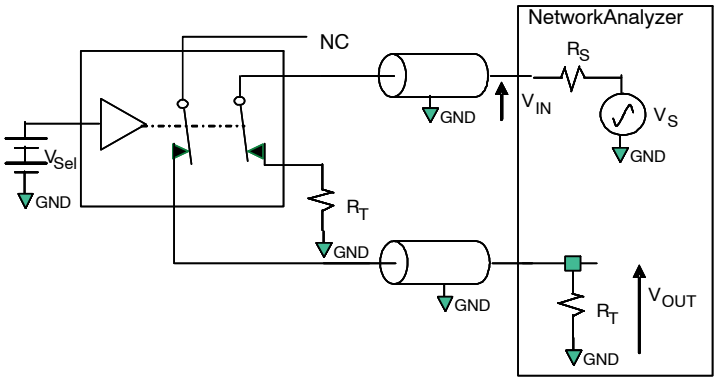
Figure 12. Bandwidth



R_S, R_T, and are functions of the application environment (see AC Tables for specific values)

Off isolation = 20 Log (V_{OUT} / V_{IN})

Figure 13. Channel Off Isolation



Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 14. Non−Adjacent Channel−to−Channel Crosstalk

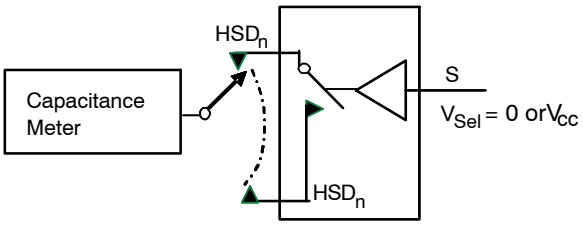


Figure 15. Channel Off Capacitance

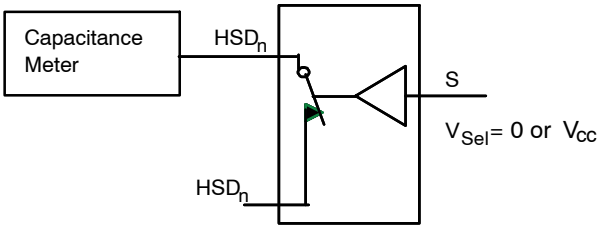


Figure 16. Channel On Capacitance

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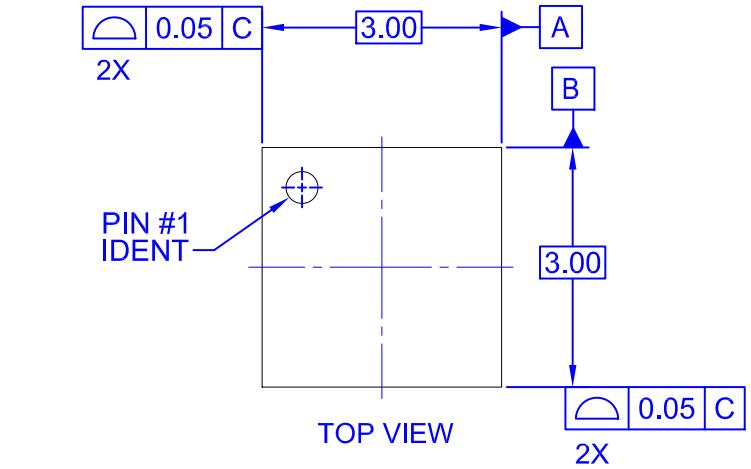
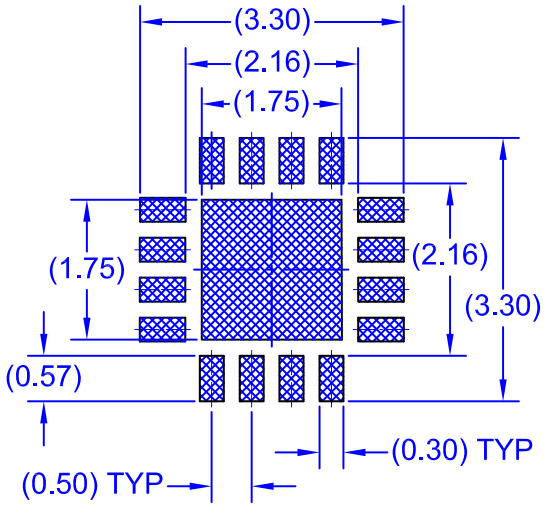
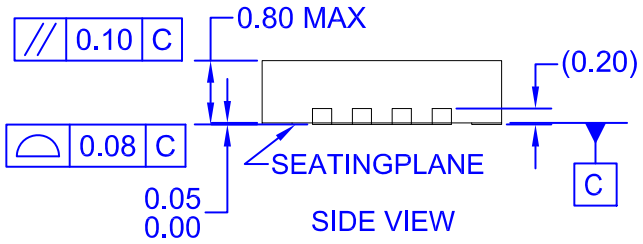
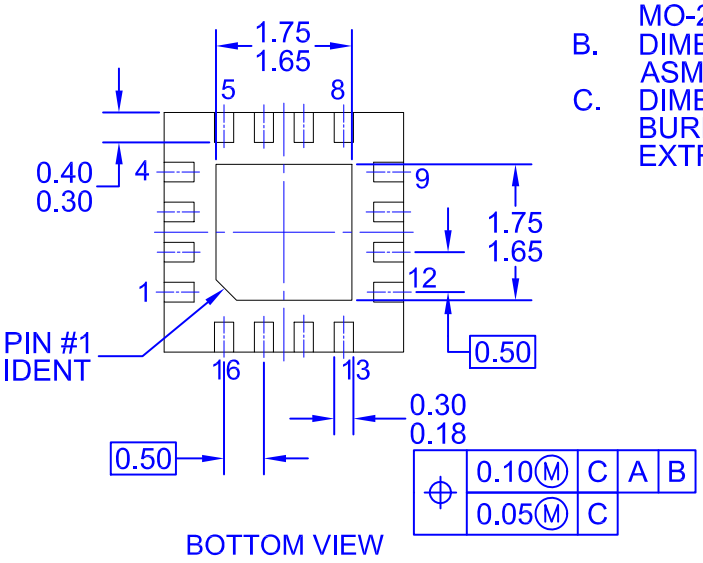




RECOMMENDED LAND PATTERN



NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-220
B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



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ISSUE O

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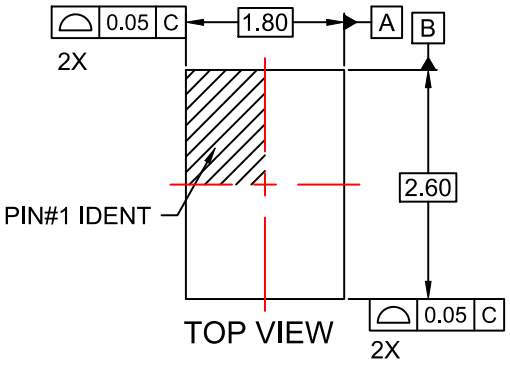
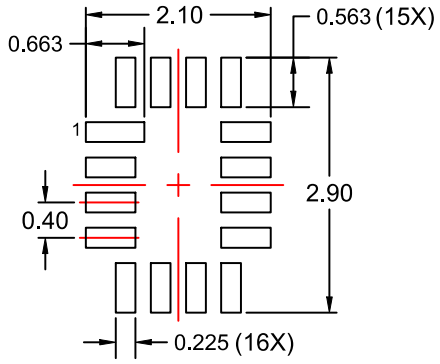
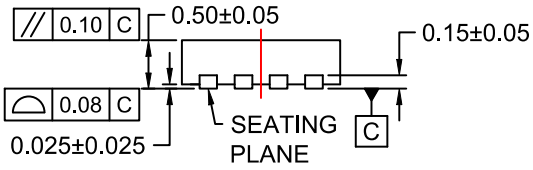


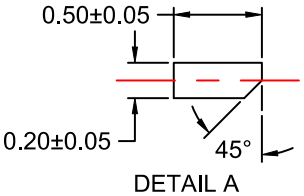
TOP VIEW



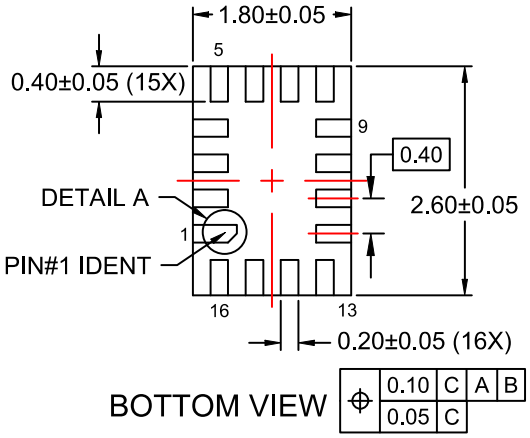
RECOMMENDED
LAND PATTERN



SIDE VIEW

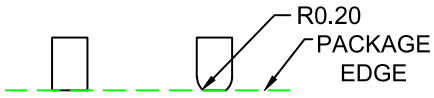


DETAIL A
SCALE : 2X



BOTTOM VIEW

LEAD SHAPE AT PACKAGE EDGE



LEAD
OPTION 1
SCALE : 2X

LEAD
OPTION 2
SCALE : 2X

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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