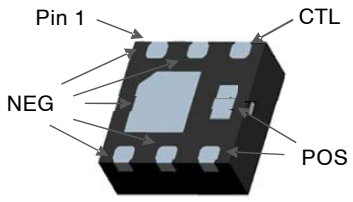
Low-Side Reverse Bias / Reverse Polarity Protector

15 mΩ, −20 V

FR015L3EZ



WDFN6 2x2, 0.65P
(MicroFET)
CASE 511CZ

MARKING DIAGRAM

&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
019L	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Description

Reverse bias is an increasingly common fault event that may be generated by user error, improperly installed batteries, automotive environments, erroneous connections to third−party chargers, negative “hot plug” transients, inductive transients, and readily available negatively biased rouge USB chargers.

onsemi circuit protection is proud to offer a new type of reverse bias protection devices. The FR devices are low resistance, series switches that, in the event of a reverse bias condition, shut off power and block the negative voltage to help protect downstream circuits.

The FR devices are optimized for the application to offer best in class reverse bias protection and voltage capabilities while minimizing size, series voltage drop, and normal operating power consumption.

In the event of a reverse bias application, FR015L3EZ devices effectively provide a full voltage block and can easily protect −0.3 V rated silicon.

From a power perspective, in normal bias, a 15 mΩ FR device in a 0.1 A application will generate only 1.5 mV of voltage drop or 0.15 mW of power loss. In reverse bias, FR devices dissipate less than 10 μW in a 3 V reverse bias event. This type of performance is not possible with a diode solution.

Benefits extend beyond the device. Due to low power dissipation, not only is the device small, but heat sinking requirements and cost can be minimized as well.

Features

- Up to −20 V Reverse−Bias Protection
- Nano Seconds of Reverse−Bias Blocking Response Time
- +12 V 24−Hour “Withstand” Rating
- 15 mΩ Typical Series Resistance at 3.0 V
- 18 mΩ Typical Series Resistance at 2.1 V
- Integrated TVS Over Voltage Suppression
- MicroFET 2 x 2 mm Package Size
- USB V_{BUS} Compatible
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- 3 V+ Battery Operated Systems
- Reverse Battery Protection
- 2 to 5 Cell Alkaline Battery Operated Systems
- USB 1.0, 2.0 and 3.0 Devices
- USB Charging
- Mobile Devices
- Mobile Medical

Applications (Continued)

- Toys
- Any DC Barrel Jack Powered Device
- Any DC Devices subject to Negative Hot Plug or Inductive Transients

DIAGRAMS

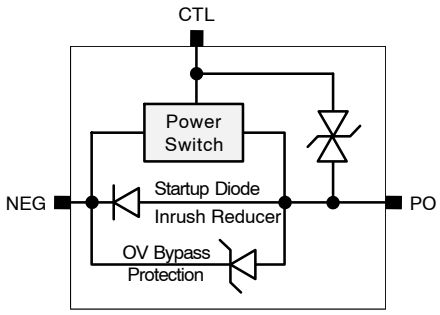


Figure 1. Block Diagram

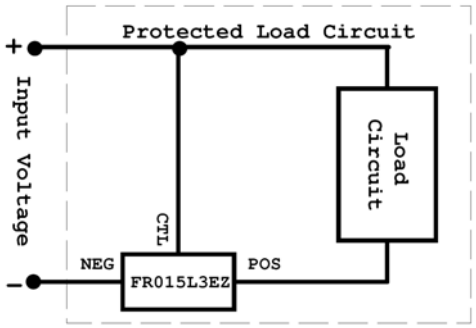
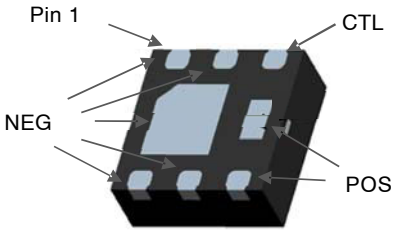


Figure 2. Typical Schematic

PIN CONFIGURATION



MicroFET 2x2 mm

Figure 3. Pin Assignments

PIN DEFINITIONS

Name	Pin	Description
POS	4	The ground of the load circuit to be protected. Current flows into this pin during normal bias operation.
CTL	3	The control pin of the device. A positive voltage on this pin with regard to NEG pin turns the switch on and a negative voltage turns the switch to a high impedance state.
NEG	1, 2, 5, 6	The ground of the input power source. Current flows out of this pin during normal bias operation.

ABSOLUTE MAXIMUM RATINGS (Values are at T_A = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
$V+_{MAX\_OP}$	Steady−State Normal Operating Voltage between CTL and NEG Pins (V_{IN} = $V+_{MAX\_OP}$, I_{IN} = 1.5 A, Switch On)			+8	V
$V+_{24}$	24−Hour Normal Operating Voltage Withstand Capability between CTL and NEG Pins (V_{IN} = $V+_{24}$, I_{IN} = 1.5 A, Switch On) (Note 1)			12	
$V-_{MAX\_OP}$	Steady−State Reverse Bias Standoff Voltage between CTL and NEG Pins (V_{IN} = $V-_{MAX\_OP}$)			−20	
I_{IN}	Input Current	V_{IN} = 3 V, Continuous (Note 2) *(See Figure 4)*		8	A
T_J	Operating Junction Temperature			150	°C
P_D	Power Dissipation	T_A = 25°C (Note 2) *(See Figure 4)*		2.4	W
		T_A = 25°C (Note 2) *(See Figure 5)*		0.9	
I_{DIODE_CONT}	Steady−State Diode Continuous Forward Current from POS to NEG			2	A
I_{DIODE_PULSE}	Pulsed Diode Forward Current from POS to NEG (300 μs Pulse)			190	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114		2500	V
		Charged Device Model, JESD22−C101		2000	
		System Model, IEC61000−4−2	POS is Shorted to CTL	Contact	5000
				Air	7000
			No External Connection between POS and CTL	Contact	300
				Air	3000

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The V_{+24} rating is NOT a survival guarantee. It is a statistically calculated survivability reference point taken on qualification devices, where the predicted failure rate is less than 0.01% at the specified voltage for 24 hours. It is intended to indicate the device's ability to withstand transient events that exceed the recommended operating voltage rating. Specification is based on qualification devices tested using accelerated destructive testing at higher voltages, as well as production pulse testing at the V_{+24} level. Production device field life results may vary. Results are also subject to variation based on implementation, environmental considerations, and circuit dynamics. Systems should never be designed with the intent to normally operate at V_{+24} levels. *Contact* ***onsemi*** *for additional information*.
2. The device power dissipation and thermal resistance (R_θ) are characterized with device mounted on the following FR4 printed circuit boards, as shown in Figure 4 and Figure 5.

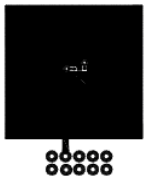


Figure 4. 1 Square Inch of 2−ounce Copper

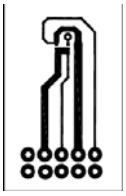


Figure 5. Minimum Pads of 2−ounce Copper

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2) *(See Figure 4)*	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2) *(See Figure 5)*	150	

ELECTRICAL CHARACTERISTICS (Values are at T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
POSITIVE BIAS CHARACTERISTICS						
R_{ON}	Device Resistance, Switch On	V_{IN} = +1.7 V, I_{IN} = 1.5 A	–	22	30	mΩ
		V_{IN} = +2.1 V, I_{IN} = 1.5 A	–	18	25	
		V_{IN} = +3 V, I_{IN} = 1.5 A	–	15	20	
		V_{IN} = +5 V, I_{IN} = 1.5 A	–	14	19	
		V_{IN} = +3 V, I_{IN} = 1.5 A, T_J = 125°C	–	22	30	
V_{ON}	Input Voltage, V_{IN}, at which Voltage at POS, V_{POS}, Reaches a Certain Level at Given Current	I_{IN} = 100 mA, V_{POS} = 50 mV, V_{NEG} = 0 V	0.7	1.0	1.3	V
$\Delta V_{ON} / \Delta T_J$	Temperature Coefficient of V_{ON}		–	–1.7	–	mV/°C
I_{DIODE_CONT}	Continuous Diode Forward Current	$V_{CTL} = V_{POS}$	–	–	2	V
V_F	Diode Forward Voltage	$V_{CTL} = V_{POS}$, I_{DIODE} = 3 A, Pulse width < 300 μs	0.65	0.80	0.95	V
I_{BIAS}	Bias Current Flowing out of NEG Pin during Normal Bias Operation	V_{CTL} = 8 V, V_{NEG} = 0 V, No Load	–	–	10	μA
NEGATIVE BIAS CHARACTERISTICS						
$V_{-\ MAX\_OP}$	Reverse Bias Breakdown Voltage	I_{IN} = –250 μA, $V_{CTL} = V_{POS}$ = 0 V	–	–	–20	V
$\Delta V_{-\ MAX\_OP} / \Delta T_J$	Reverse Bias Breakdown Voltage Temperature Coefficient		–	16	–	mV/°C
I_-	Leakage Current from NEG to POS in Reverse–Bias Condition	V_{NEG} = 16 V, $V_{CTL} = V_{POS}$ = 0 V	–	–	1	μA
t_{RN}	Time to Respond to Negative Bias Condition	V_{NEG} = 2.7 V, V_{CTL} = 0 V, C_{LOAD} = 10 μF, Reverse Bias Startup Inrush Current = 0.2 A	–	–	50	ns
INTEGRATED TVS PERFORMANCE						
V_Z	Breakdown Voltage @ I_T	I_T = 1 mA	12	13	14.5	V
I_R	Leakage Current from CTL to POS, NEG is Open	$V_{CTL} - V_{POS}$ = 8 V	–	2	10	μA
		$V_{CTL} - V_{POS}$ = –8 V	–	–2	–10	
I_{PPM}	Max Pulse Current from CTL to POS, IEC61000–4–5 8x20 μs Pulse, NEG is Open	$V_{CTL} > V_{POS}$	–	–	0.6	A
		$V_{CTL} < V_{POS}$	–	–	0.4	
V_C	Clamping Voltage from CTL to POS	$V_{CTL} > V_{POS}$	–	–	15.0	V
		$V_{CTL} < V_{POS}$	–	–	14.3	
DYNAMIC CHARACTERISTICS						
C_I	Input Capacitance between CTL and NEG	V_{IN} = 3 V, $V_{NEG} = V_{POS}$ = 0 V, f = 1 MHz	–	900	–	pF
C_S	Switch Capacitance between POS and NEG		–	133	–	
C_O	Output Capacitance between CTL and POS		–	967	–	
R_C	Control Internal Resistance		–	2	–	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified.)

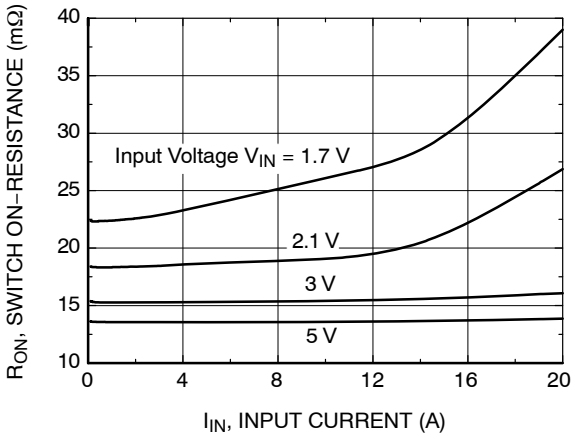


Figure 6. Switch On Resistance vs. Switch Current

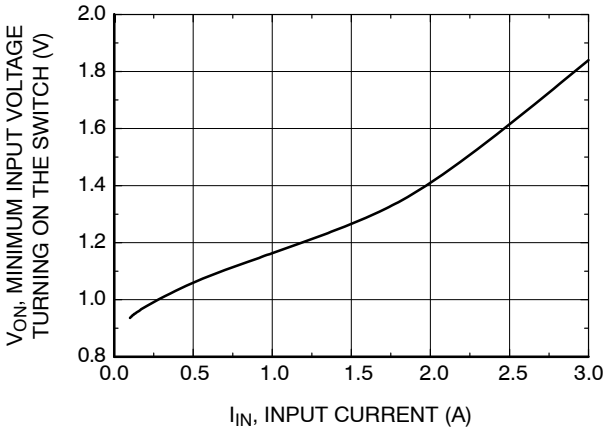


Figure 7. Minimum Input Voltage to Turn On Switch vs. Current at 50 mV Switch Voltage Drop

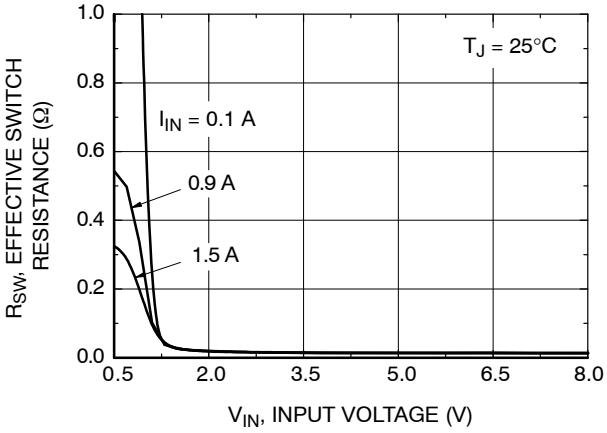


Figure 8. Effective Switch Resistance R_{SW} vs. Input Voltage V_{IN}

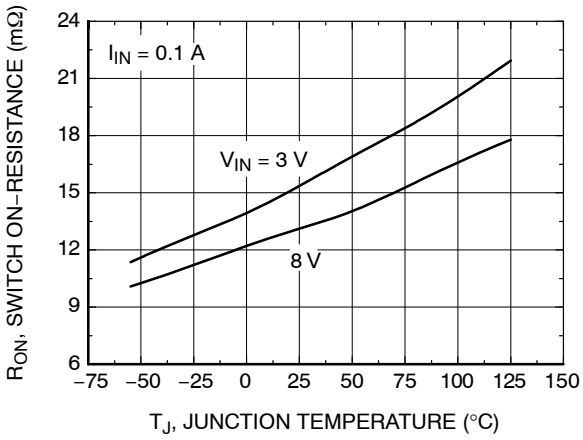


Figure 9. Switch On Resistance vs. Junction Temperature at 0.1 A

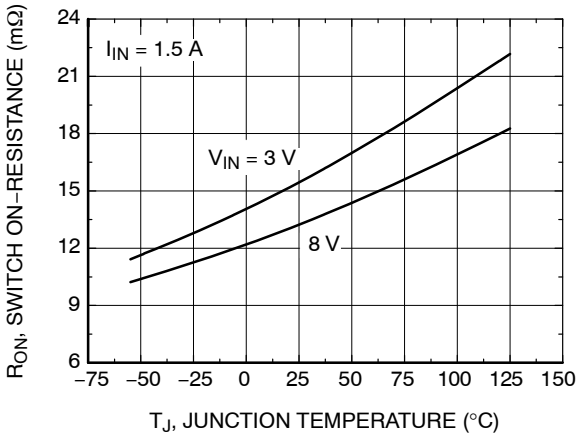


Figure 10. Switch On Resistance vs. Junction Temperature at 1.5 A

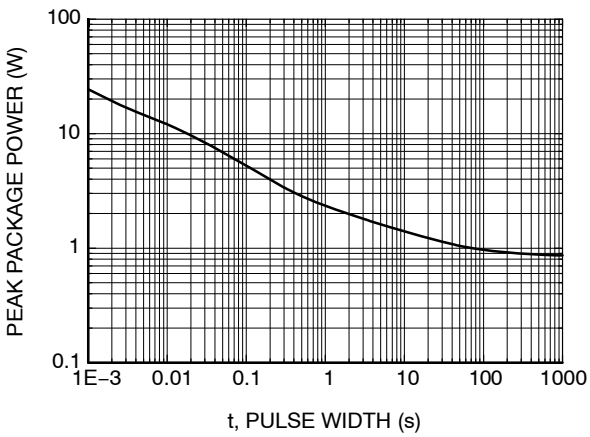


Figure 11. Single−Pulse Maximum Power vs. Time

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified.) (Continued)

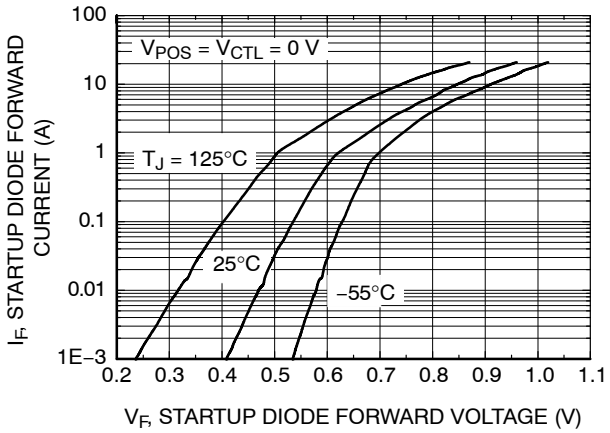


Figure 12. Startup Diode Current vs. Forward Voltage

APPLICATION TEST CONFIGURATIONS

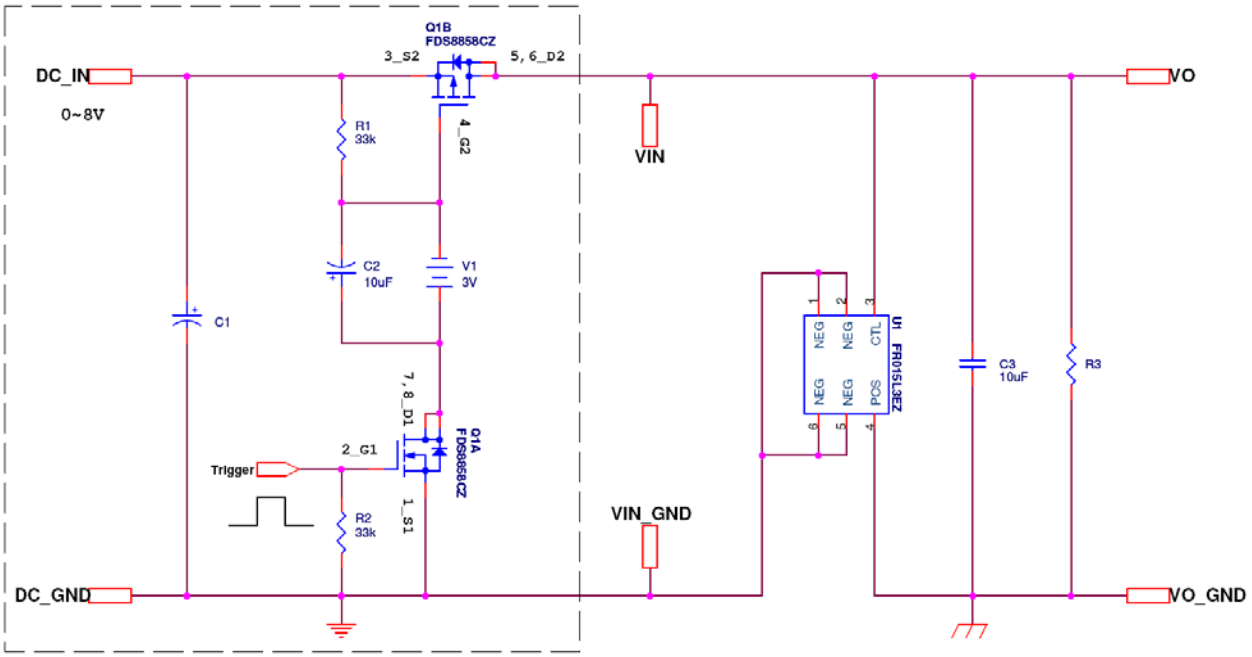


Figure 13. Startup Test Circuit – Normal Bias with FR015L3EZ Device

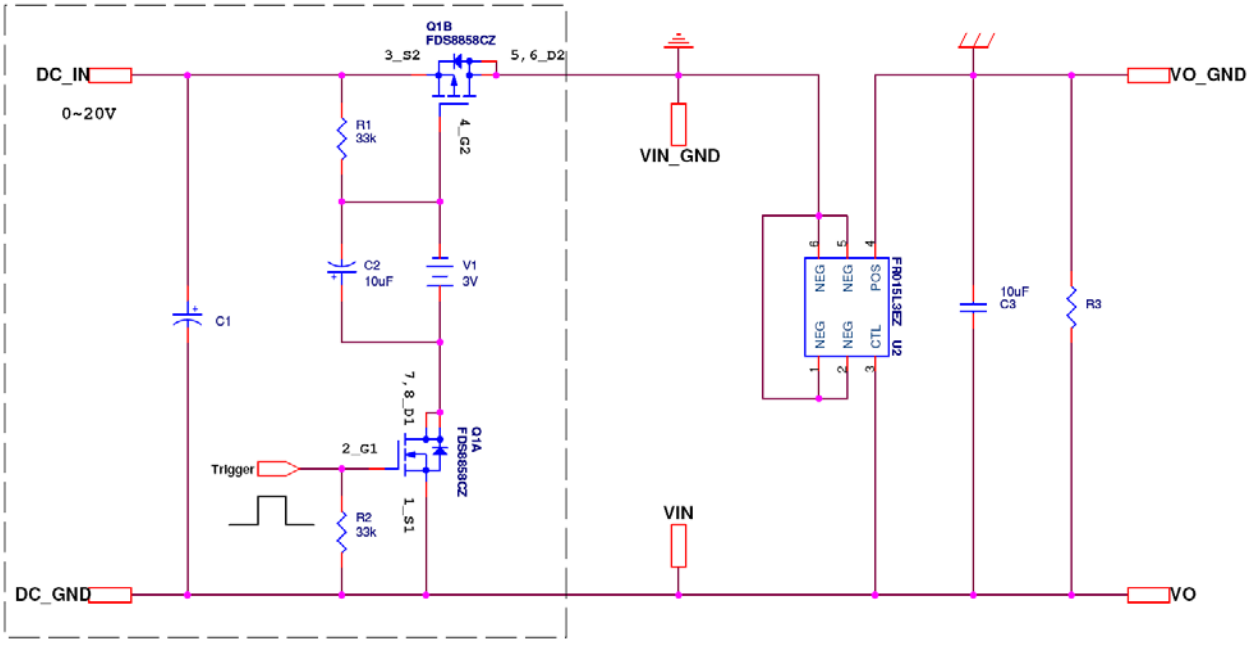


Figure 14. Startup Test Circuit – Reverse Bias with FR015L3EZ Device

APPLICATION TEST CONFIGURATIONS (Continued)

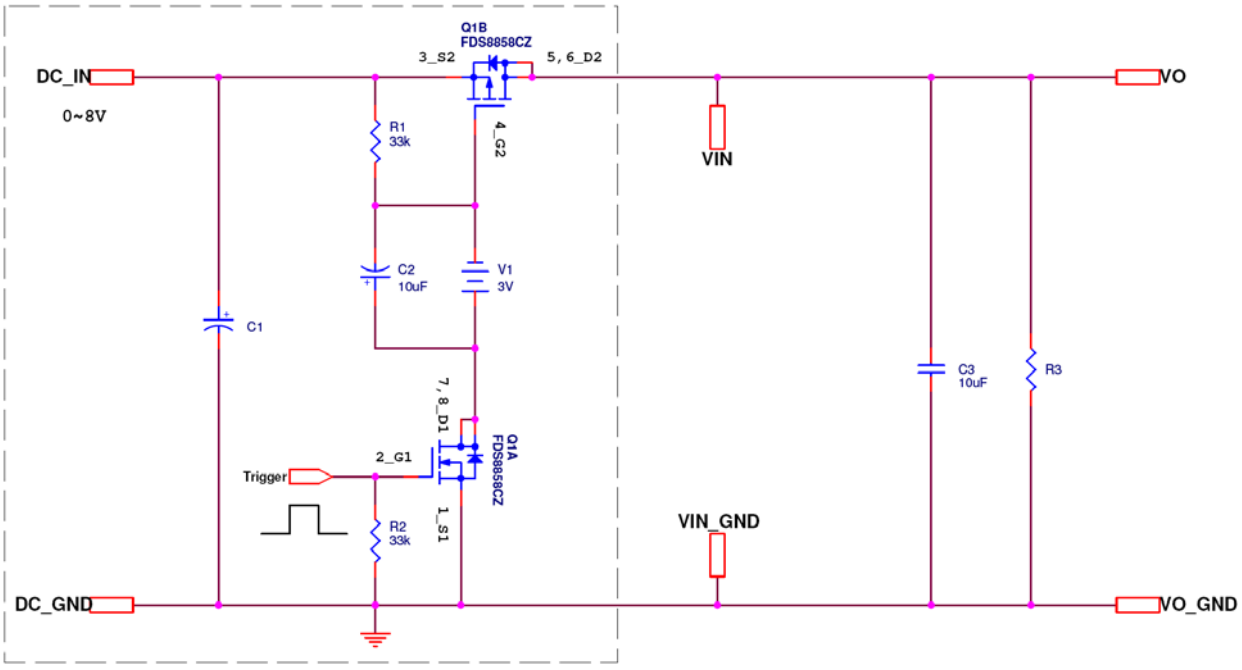


Figure 15. Startup Test Circuit – No Reverse Polarity Protection

TYPICAL APPLICATION WAVEFORMS

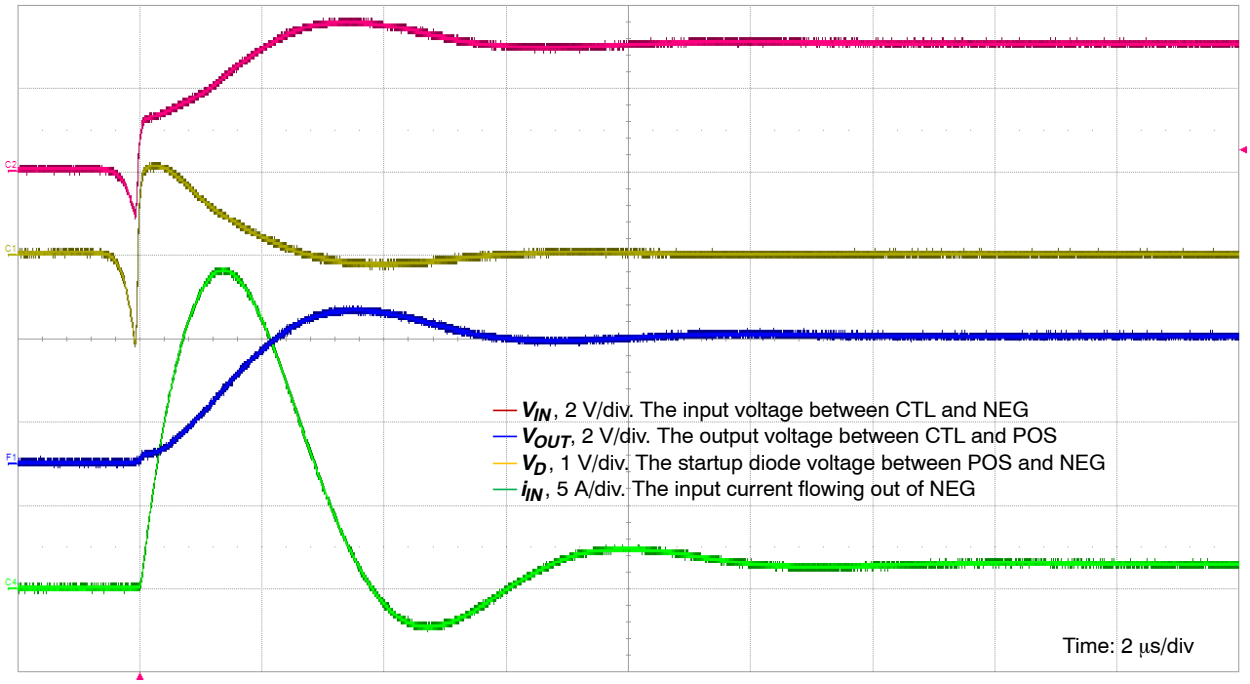


Figure 16. Normal Bias Startup Waveform, V_{IN} = 3 V, V_1 = 3 V, C_1 = 5200 μF, C_2 = C_3 = 10 μF, R_1 = R_2 = 33 kΩ, R_3 = 2 Ω

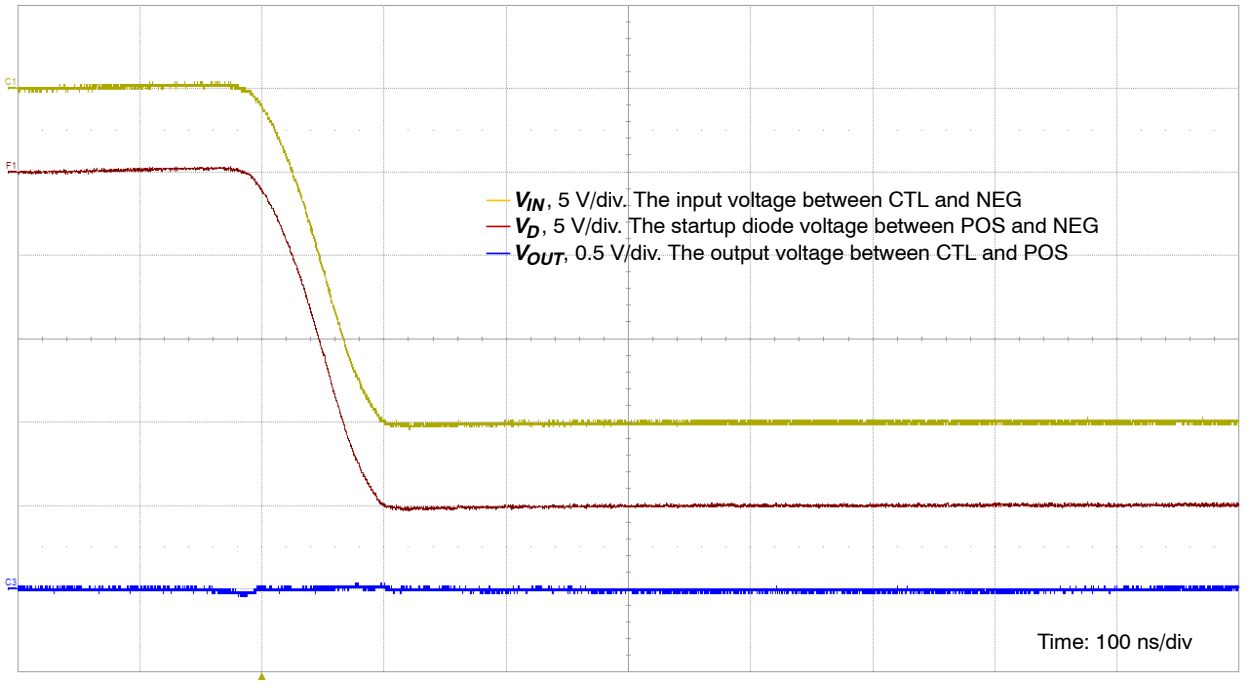


Figure 17. Reverse Bias Startup Waveform, V_{IN} = 3 V, V_1 = 3 V, C_1 = 5200 μF, C_2 = C_3 = 10 μF, R_1 = R_2 = 33 kΩ, R_3 = 2 Ω

TYPICAL APPLICATION WAVEFORMS (Continued)

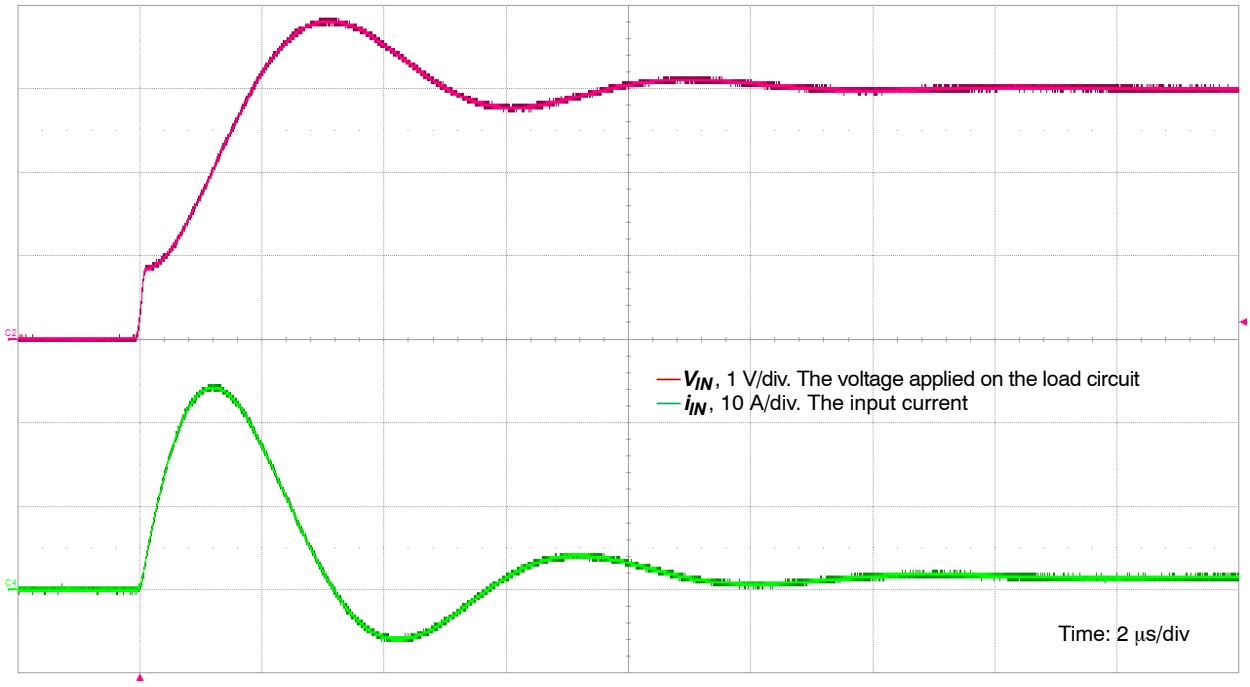


Figure 18. Startup Waveform without FR015L3EZ Device, V_{IN} = 3 V, V_1 = 3 V, C_1 = 5200 μF, C_2 = C_3 = 10 μF, R_1 = R_2 = 33 kΩ, R_3 = 2 Ω

APPLICATION INFORMATION

The FR015L3EZ is capable of being turned on at a voltage as low as 1.5V, therefore is especially suitable for low voltage application like AA, AAA or single lithium−ion battery operated devices. The voltage and current waveforms in Figure 16 and Figure 18 are both captured with a 2 Ω load at 3 V input.

When the DC power source is connected to the circuit *(refer to Figure 1 and Figure 2)*, the built−in startup diode initially conducts the current such that the load circuit powers up. Due to the initial diode voltage drop, the FR015L3EZ effectively reduces the peak inrush current of a hot plug event. Under these test conditions, the input inrush current reaches about 19 A peak. While the current flows, the input voltage increases. The speed of this input voltage increase depends on the time constant formed by the load resistance R_3 and load capacitance C_3, assuming the input voltage source holds itself during turn on. The larger the time constant, the slower the input voltage increase. As the input voltage approaches a level equal to the protector's turn−on voltage, V_{ON}, the protector turns on and operates in Low−Resistance Mode as defined by V_{IN} and operating current I_{IN}.

In the event of a negative voltage transient between CTL and NEG, or when the DC power source, V_{IN}, is reversely connected to the circuit, while no residual voltage presents between CTL and POS, the device blocks the flow of current and holds off the voltage, thereby protecting the load circuit. Figure 17 shows the startup waveforms while a passive load circuit is reversely biased. It can be clearly seen that the output voltage is near 0 or at a level that is harmless to the load circuit.

Figure 18 shows the voltage and current waveforms when no reverse bias protection is implemented. In Figure 16, while the reverse bias protector is present, the input voltage, V_{IN}, and the output voltage, V_O, are separated and look different. When this reverse bias protector is removed, V_{IN} and V_O merge, as shown in Figure 18 as V_{IN}. This V_{IN} is also the voltage applied to the load circuit. It can be seen that, with reverse bias protection, the voltage applied to the load and the current flowing into the load look very much the same as without reverse bias protection.

In Figure 16, negative voltage spikes are seen on V_{IN} and V_D before V_{IN} starts to rise from 0; and in both Figures 16 and 18, negative input current is seen after FR015L3EZ is fully turned on. These phenomena are a combined effect of parasitic inductance and all the capacitors in the input voltage control circuit enclosed in the broken line as shown in Figures 13 to 15. This is not a problem as long as the load circuit doesn't see a negative voltage at anytime, which is what the reverse bias protector is meant for. Indeed, we can see from Figures 16 and 18, the output voltage on the load circuit is always equal to or greater than 0 V.

Benefits of Reverse Bias Protection

The most important benefit is, of course, to prevent accidently reverse−biased voltage from damaging the load circuit. Another benefit is that the peak startup inrush current can be reduced. How fast the input voltage rises, the input/output capacitance, the input voltage, and how heavy the load is determine how much the inrush current can be reduced. In this specific 3 V / 2 A application, for example, the inrush current has been reduced from 24 A to 19 A, a 21% reduction. This can offer a system designer the option of increasing C_3 while keeping “effective” load circuit capacitance down.

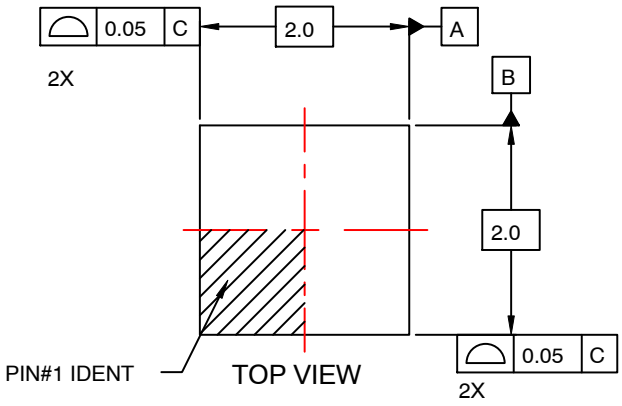
ORDERING INFORMATION

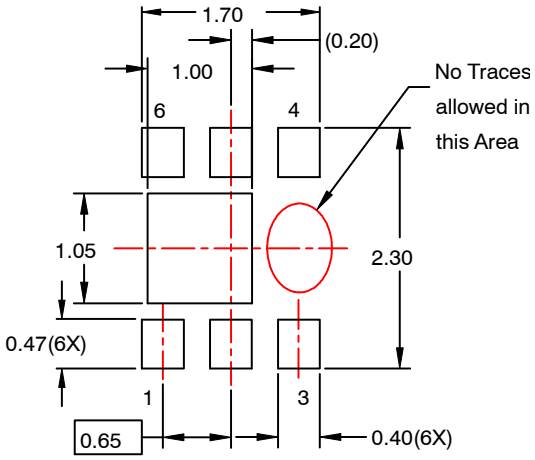
Part Number	Operating Temperature Range	Top Mark	Package	Shipping†
FR015L3EZT	−55°C ~ 125°C	019L	6−Lead, Molded Leadless Package (MLP), Dual, Non−JEDEC, 2 mm Square, Single−Tied DAP (Pb−Free. Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

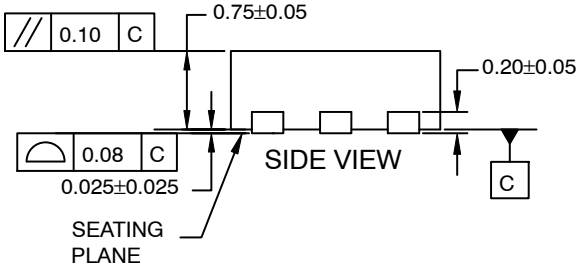
WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

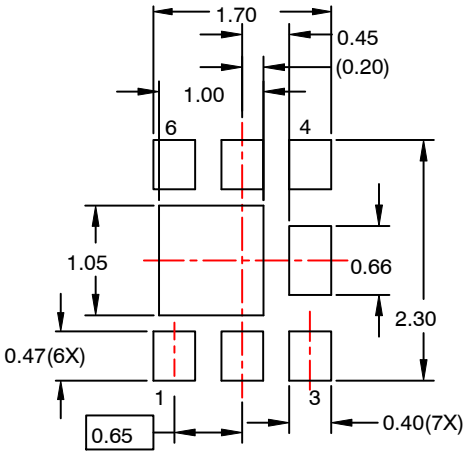
DATE 31 JUL 2016



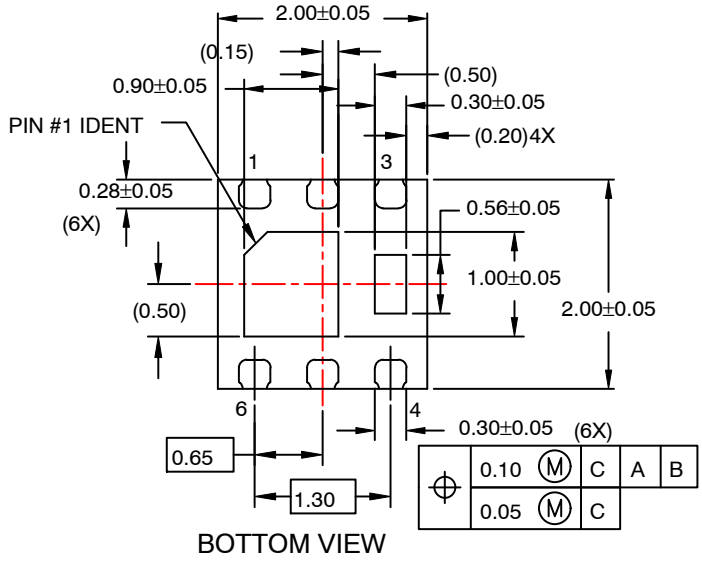


RECOMMENDED
LAND PATTERN OPT 1





RECOMMENDED
LAND PATTERN OPT 2



NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO−229 REGISTRATION

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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