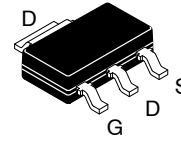


MOSFET – P-Channel QFET®

-200 V, -0.67 A, 2.7 Ω

FQT3P20



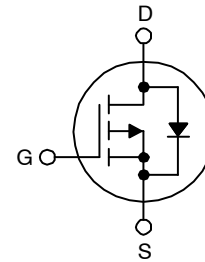
SOT-223
CASE 318H-01

Description

This P-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -0.67 A, -200 V, $R_{DS(on)} = 2.7 \Omega$ (Max) @ $V_{GS} = 10$ V, $I_D = 0.335$ A
- Low Gate Charge (Typ. 6.0 nC)
- Low C_{rss} (Typ. 7.5 pF)
- This is a Pb-Free Device



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	-200	V
I_D	Drain Current Continuous ($T_C = 25^\circ\text{C}$) Continuous ($T_C = 70^\circ\text{C}$)	-0.67 -0.53	A
I_{DM}	Drain Current - Pulsed (Note 1)	-2.7	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	150	mJ
I_{AR}	Avalanche Current (Note 1)	-0.67	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.25	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-5.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) Derate above 25°C	2.5 0.02	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

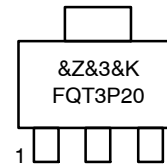
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $L = 500$ mH, $I_{AS} = -0.67$ A, $V_{DD} = -50$ V, $R_G = 25 \Omega$, Starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq -2.8$ A, $di/dt \leq 300$ A/ μs , $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	$^\circ\text{C}/\text{W}$

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Date Code
&K = Lot Run Traceability Code
FQT3P20 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FQT3P20TF	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FQT3P20

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

OFF CHARACTERISTIC

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = –250 μA	–200	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C	–	–0.18	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = –200 V, V _{GS} = 0 V	–	–	–1	μA
		V _{DS} = –160 V, T _C = 125°C	–	–	–10	
I _{GSSF}	Gate–Body Leakage Current, Forward	V _{GS} = –30 V, V _{DS} = 0 V	–	–	–100	nA
I _{GSSR}	Gate–Body Leakage Current, Reverse	V _{GS} = 30 V, V _{DS} = 0 V	–	–	100	

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = –250 μA	–3.0	–	–5.0	V
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = –10 V, I _D = –0.335 A	–	2.06	2.7	Ω
g _{FS}	Forward Transconductance	V _{DS} = –40 V, I _D = –0.335 A	–	0.7	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = –25 V, V _{GS} = 0 V, f = 1.0 MHz	–	190	250	pF
C _{oss}	Output Capacitance		–	45	60	pF
C _{rss}	Reverse Transfer Capacitance		–	7.5	10	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn–On Delay Time	V _{DD} = –100 V, I _D = –2.8 A, R _G = 25 Ω (Note 4)	–	8.5	25	ns
t _r	Turn–On Rise Time		–	35	80	ns
t _{d(off)}	Turn–Off Delay Time		–	12	35	ns
t _f	Turn–Off Fall Time		–	25	60	ns
Q _g	Total Gate Charge	V _{DS} = –160 V, I _D = –2.8 A, V _{GS} = –10 V (Note 4)	–	6.0	8.0	nC
Q _{gs}	Gate–Source Charge		–	1.7	–	nC
Q _{gd}	Gate–Drain Charge		–	2.9	–	nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current	–	–	–0.67	A	
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current	–	–	–2.7	A	
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –0.67 A	–	–	–5.0	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = –2.8 A, dI _F /dt = 100 A/μs	–	100	–	ns
Q _{rr}	Reverse Recovery Charge		–	0.34	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

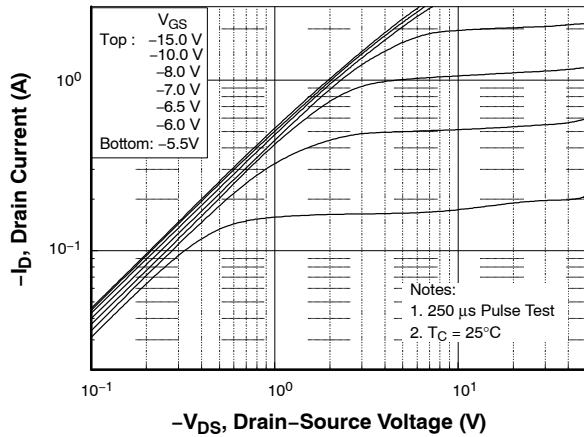


Figure 1. On-Region Characteristics

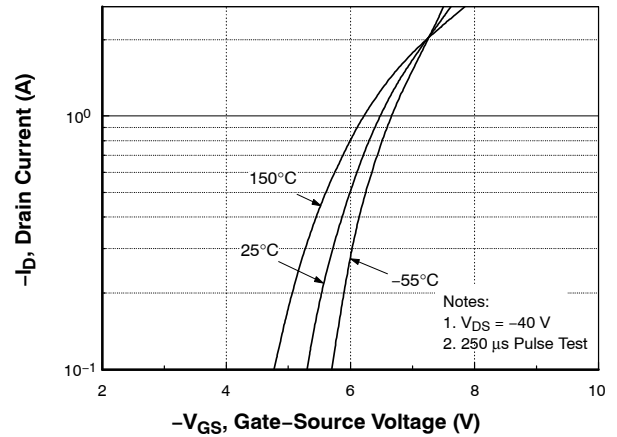


Figure 2. Transfer Characteristics

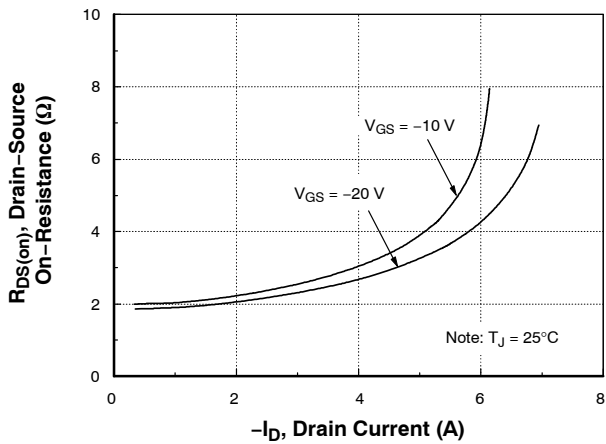


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

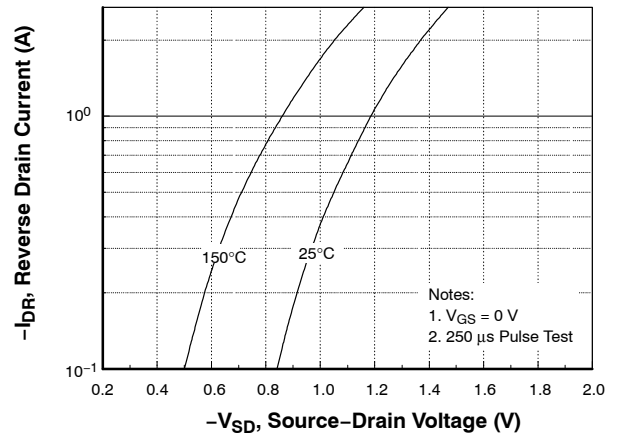


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

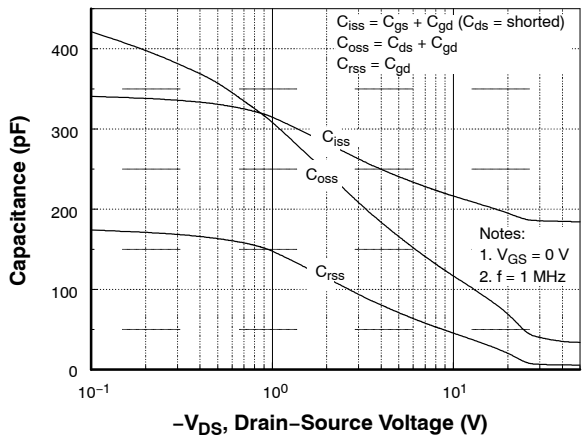


Figure 5. Capacitance Characteristics

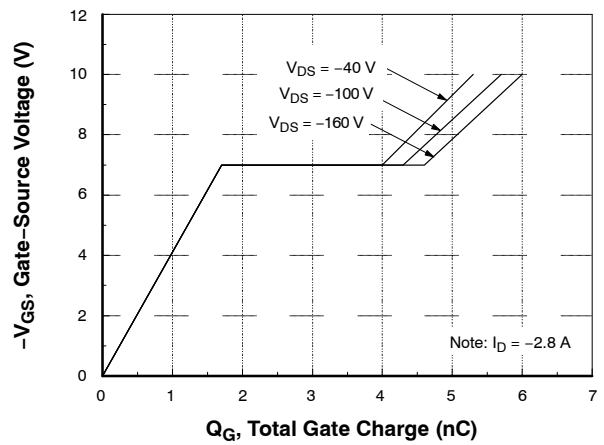


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (Continued)

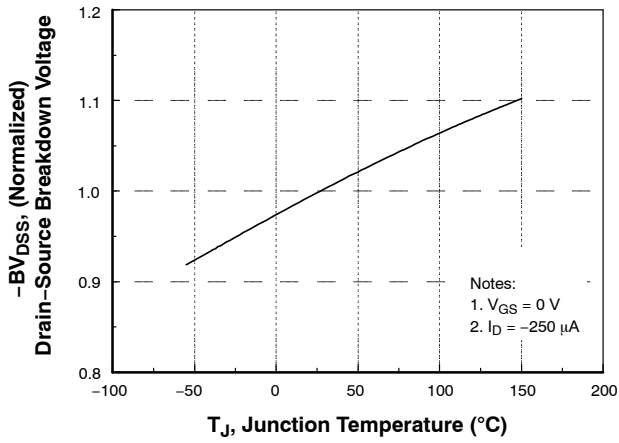


Figure 7. Breakdown Voltage Variation vs. Temperature

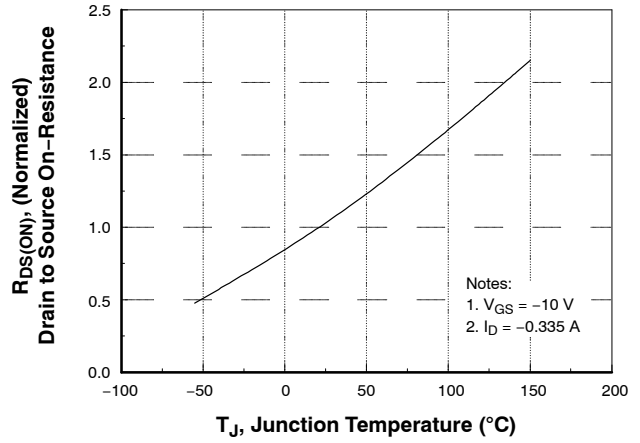


Figure 8. On-Resistance Variation vs. Temperature

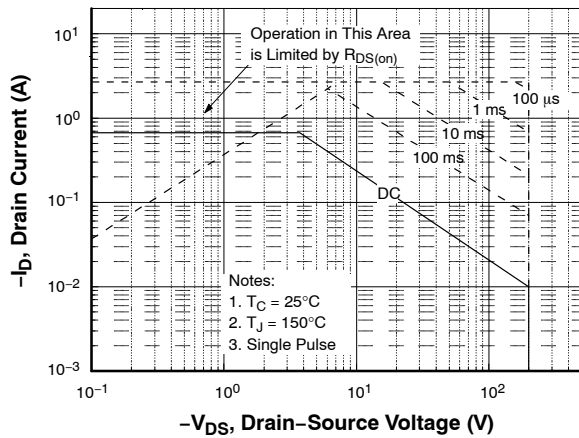


Figure 9. Maximum Safe Operating Area

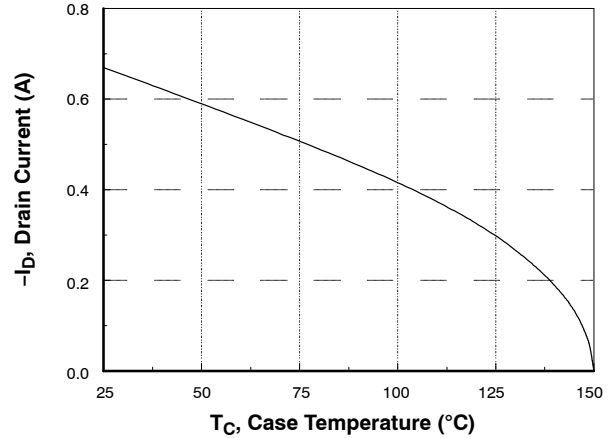


Figure 10. Maximum Drain Current vs. Case Temperature

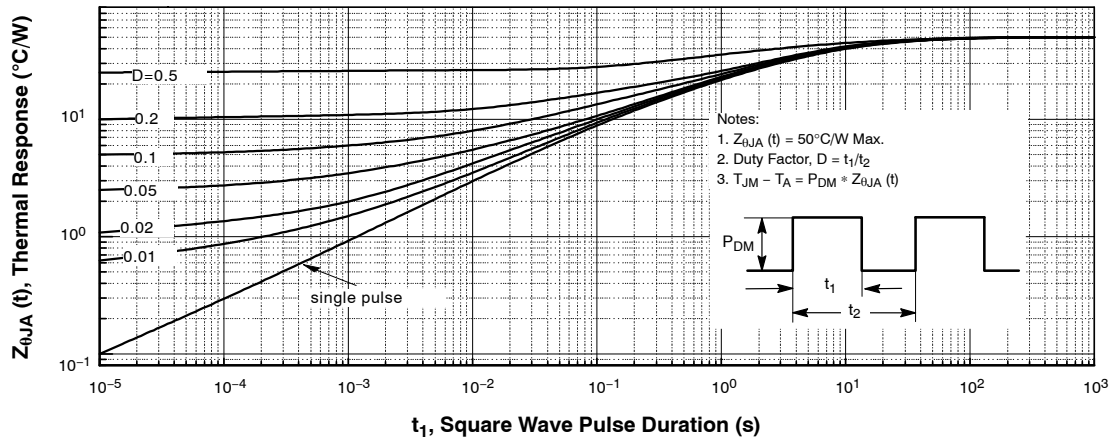


Figure 11. Transient Thermal Response Curve

FQT3P20

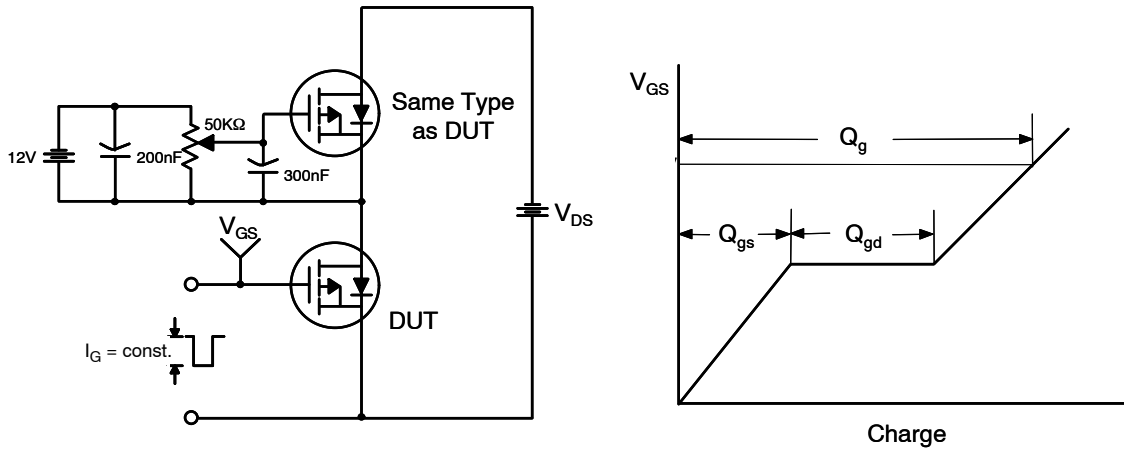


Figure 12. Gate Charge Test Circuit & Waveform

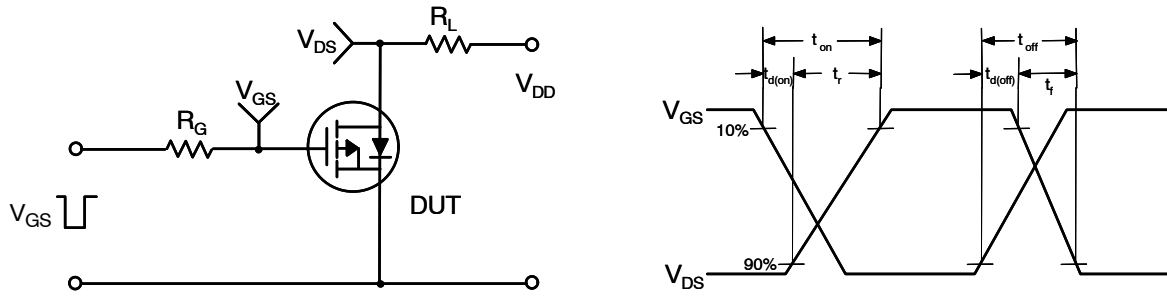


Figure 13. Resistive Switching Test Circuit & Waveforms

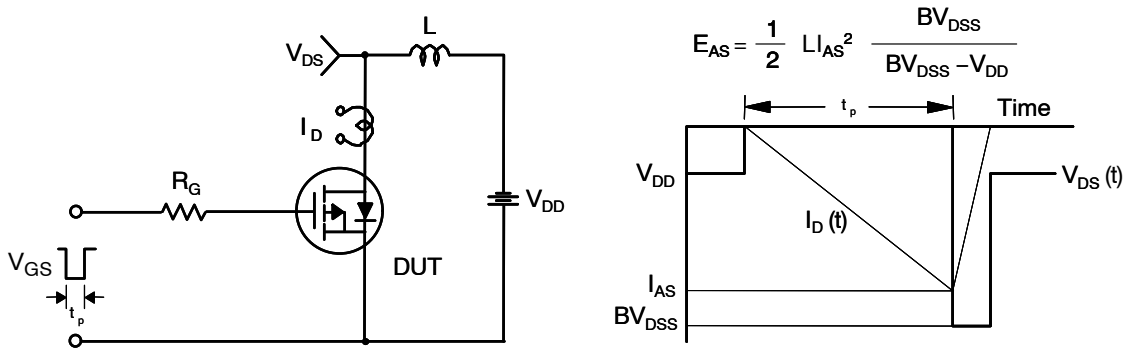


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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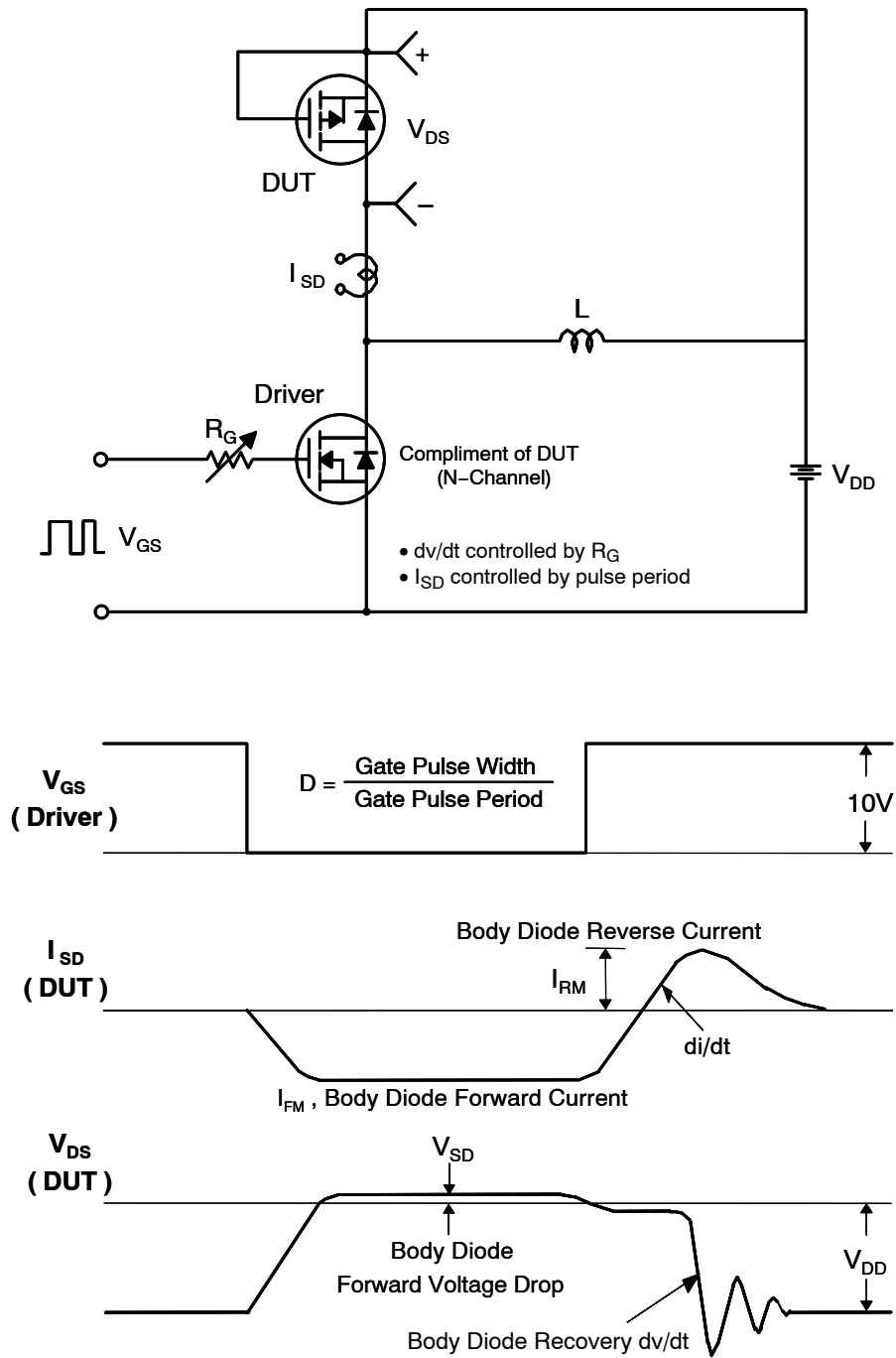
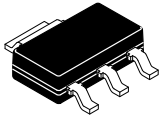


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

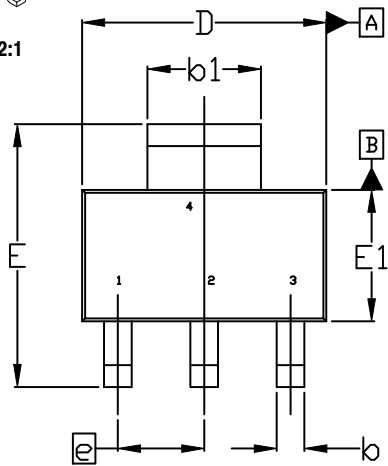
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SCALE 2:1

SOT-223
CASE 318H
ISSUE B

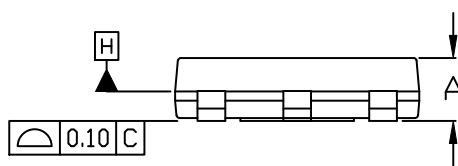
DATE 13 MAY 2020



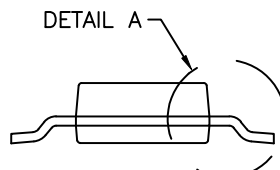
TOP VIEW

$\text{C} \text{ A} \text{ B}$

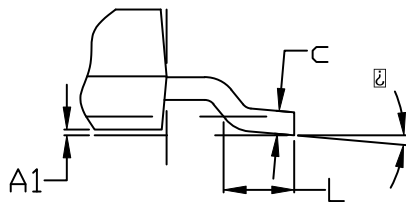
NOTE 7



SIDE VIEW



END VIEW



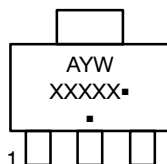
DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
\square	0°	---	10°

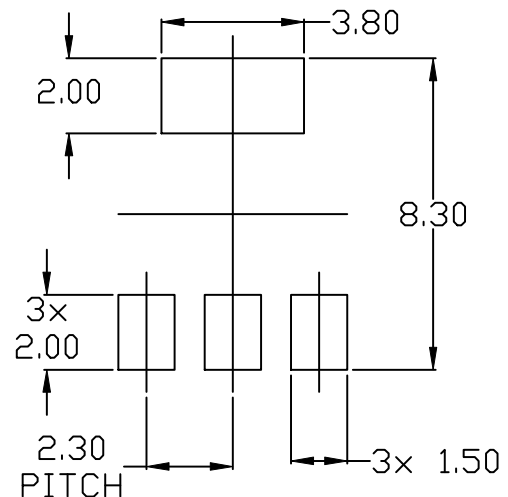
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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DESCRIPTION:	SOT-223	PAGE 1 OF 1

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