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July 2013

FQPF2N80YDTU

N-Channel QFET® MOSFET

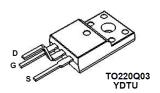
8\$0 V, 1.5 A, * " Ω

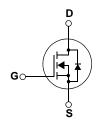
Description

produced using Fairchild Semiconductor®'s proprietary

Low Gate Charge (Typ. 12 nC) planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to $\,^{\bullet}$ Low C_{rss} (Typ. 5.5 pF) reduce on-state resistance, and to provide superior • 100% Avalanche Tested switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features





Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FQPF2N80YDTU	Unit
V _{DSS}	Drain-Source Voltage		800	V
I _D	Drain Current - Continuous (T _C = 25°	°C)	1.5	А
	- Continuous (T _C = 100°C)		0.95	А
I _{DM}	Drain Current - Pulsed	(Note 1)	6.0	А
V _{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	5.2	mJ
I _{AR}	Avalanche Current	(Note 1)	1.5	А
E _{AR}	Repetitive Avalanche Energy	(Note 1)	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.0	V/ns
P_D	Power Dissipation (T _C = 25°C)		35	W
	- Derate above 25°C		0.28	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQPF2N80YDTU	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	3.57	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	800			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.9		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V			10	μΑ
		V _{DS} = 640 V, T _C = 125°C			100	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10 V, I _D =0.75 A		4.9	6.3	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 0.75 A		2.2		S
C _{oss} C _{rss}	Output Capacitance Reverse Transfer Capacitance	f = 1.0 MHz		45 5.5	60 7.0	pF pF
Orss	Reverse Hansier Capacitance			5.5	7.0	рг
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 2.4 A,		12	35	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		30	70	ns
t _{d(off)}	Turn-Off Delay Time			25	60	ns
t _f	Turn-Off Fall Time	(Note 4)		28	65	ns
Qg	Total Gate Charge	$V_{DS} = 640 \text{ V}, I_{D} = 2.4 \text{ A},$		12	15	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		2.6		nC
Q _{gd}	Gate-Drain Charge	(Note 4)		6.0		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				1.5	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				6.0	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 1.5 \text{ A}$			1.4	V
V SD	Ziani Coaroc Zioac i cinara romage					
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 2.4 A,		480		ns

Typical Characteristics

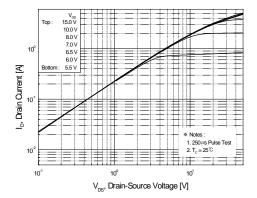


Figure 1. On-Region Characteristics

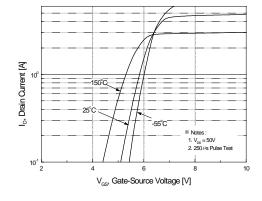


Figure 2. Transfer Characteristics

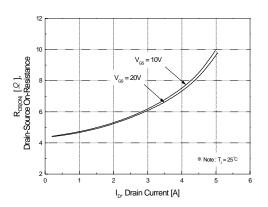


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

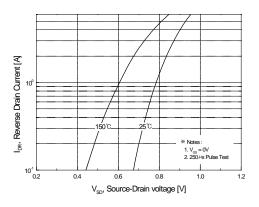


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

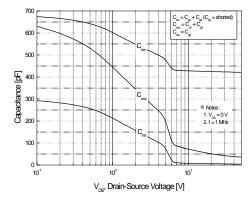


Figure 5. Capacitance Characteristics

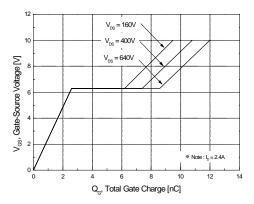


Figure 6. Gate Charge Characteristics

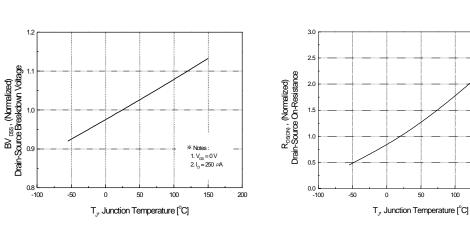


Figure 7. Breakdown Voltage Variation vs Temperature

Typical Characteristics (Continued)

Figure 8. On-Resistance Variation vs Temperature

1. V_{GS} = 10 V 2. I_D = 1.2 A

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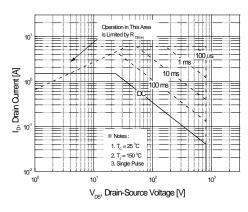


Figure 9. Maximum Safe Operating Area

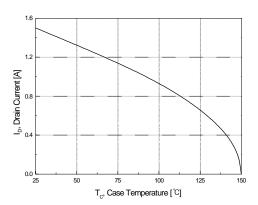


Figure 10. Maximum Drain Current vs Case Temperature

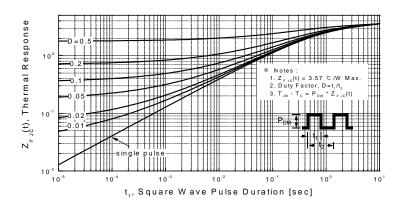
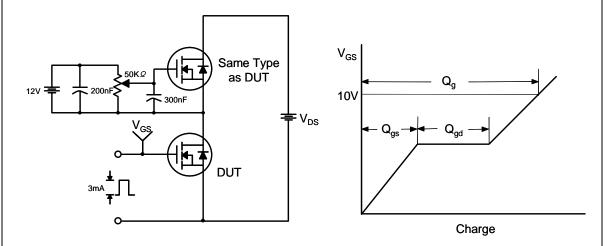
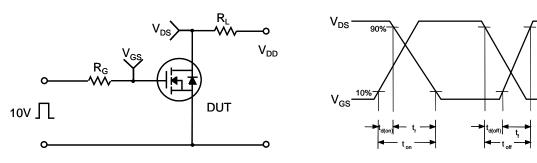


Figure 11. Transient Thermal Response Curve

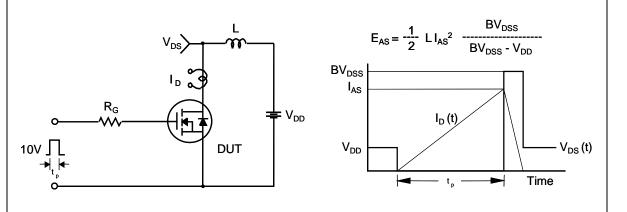
Gate Charge Test Circuit & Waveform

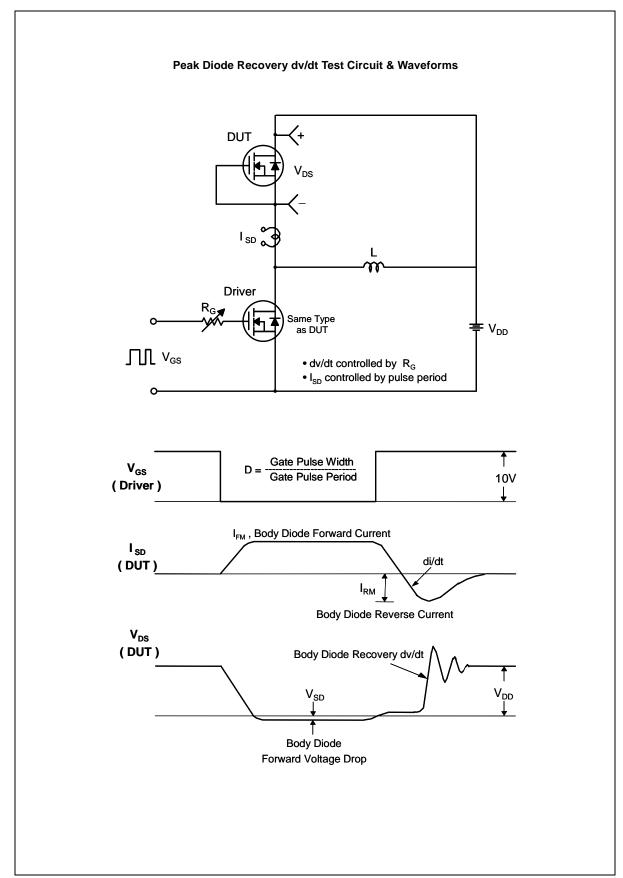


Resistive Switching Test Circuit & Waveforms



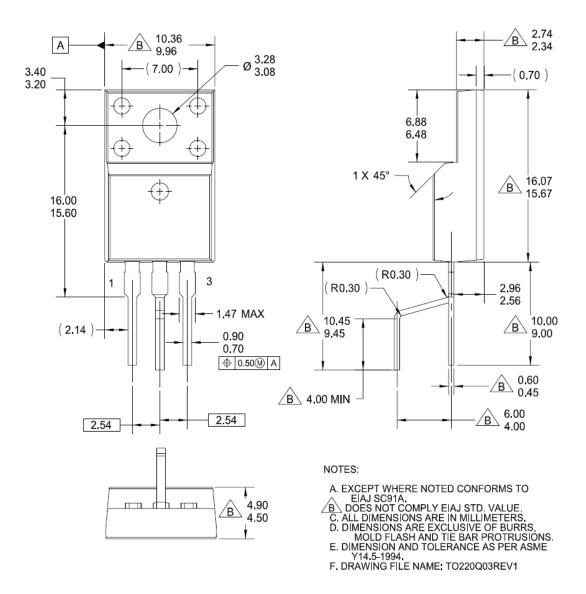
Unclamped Inductive Switching Test Circuit & Waveforms





Mechanical Dimensions

TO220Q03



TO-220F 3L - TO220, MOLDED, 3LD, FULL PACK, EIAJ SC91, Y FORMED LEAD

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Dimensions in Millimeters





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