

MOSFET – N-Channel, QFET, FRFET®

500 V, 13 A, 540 mΩ

FQPF13N50CF

Description

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 13 A, 500 V, $R_{DS(on)} = 540 \text{ m}\Omega$ (Max) @ $V_{GS} = 10 \text{ V}$, $I_D = 6.5 \text{ A}$
- Low Gate Charge (Typ. 43 nC)
- Low C_{rss} (Typ. 20 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

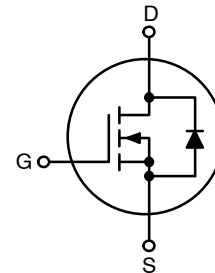
ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	500	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$) – Continuous ($T_C = 100^\circ\text{C}$)	13	A
		8	A
I_{DM}	Drain Current – Pulsed (Note 1)	52	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	530	mJ
I_{AR}	Avalanche Current (Note 1)	13	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	19.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) – Derate Above 25°C	48	W
		0.39	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 seconds	300	$^\circ\text{C}$

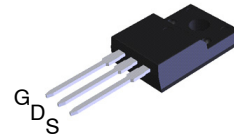
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $L = 5.6 \text{ mH}$, $I_{AS} = 13 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 13 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

V_{DS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
500 V	540 mΩ @ 10 V	13 A



N-Channel MOSFET



TO-220 Fullpack, 3-Lead
/ TO-220F-3SG
CASE 221AT

MARKING DIAGRAM



FQPF13N50CF = Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FQPF13N50CF	TO-220F (Pb-Free)	1000 / Tube

FQPF13N50CF

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.58	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.5	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{V}, V_{GS} = 0 \text{V}$	-	-	10	μA
		$V_{DS} = 400 \text{V}, T_C = 125^\circ\text{C}$	-	-	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{V}, V_{DS} = 0 \text{V}$	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{V}, V_{DS} = 0 \text{V}$	-	-	-100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{V}, I_D = 6.5 \text{A}$	-	0.43	0.54	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40 \text{V}, I_D = 6.5 \text{A}$	-	15	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{V}, V_{GS} = 0 \text{V}, f = 1.0 \text{MHz}$	-	1580	2055	pF
C_{oss}	Output Capacitance		-	180	235	pF
C_{rss}	Reverse Transfer Capacitance		-	20	25	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250 \text{V}, I_D = 13 \text{A}, R_G = 25 \Omega$ (Note 4)	-	25	60	ns
t_r	Turn-On Rise Time		-	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		-	130	270	ns
t_f	Turn-Off Fall Time		-	100	210	ns
Q_g	Total Gate Charge	$V_{DS} = 400 \text{V}, I_D = 13 \text{A}, V_{GS} = 10 \text{V}$ (Note 4)	-	43	56	nC
Q_{gs}	Gate-Source Charge		-	7.5	-	nC
Q_{gd}	Gate-Drain Charge		-	18.5	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current	-	-	13	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	-	-	52	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{V}, I_S = 13 \text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{V}, I_S = 13 \text{A}, dI_F/dt = 100 \text{A}/\mu\text{s}$	-	100	160	ns
Q_{rr}	Reverse Recovery Charge		-	0.35	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature.

FQPF13N50CF

TYPICAL CHARACTERISTICS

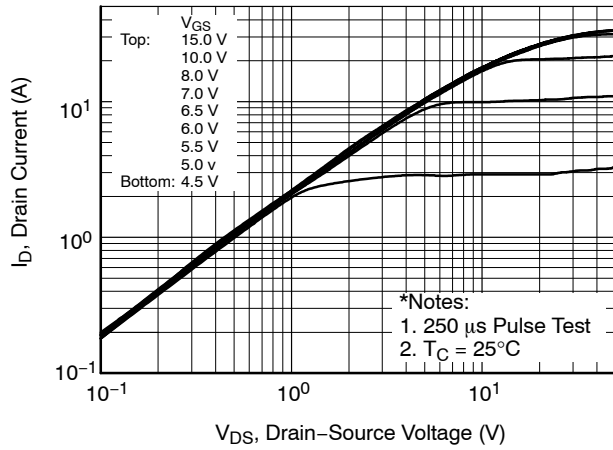


Figure 1. On-Region Characteristics

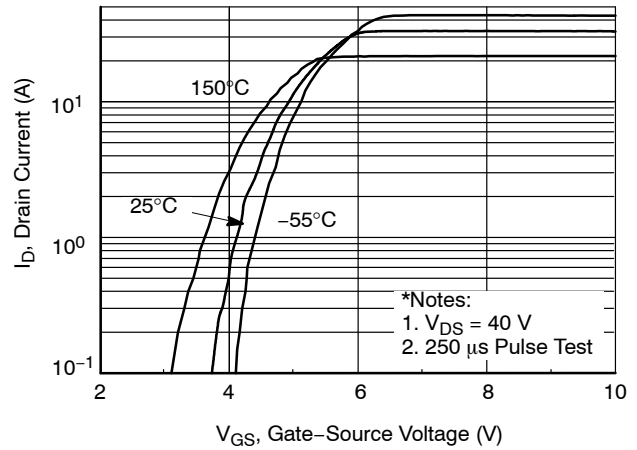


Figure 2. Transfer Characteristics

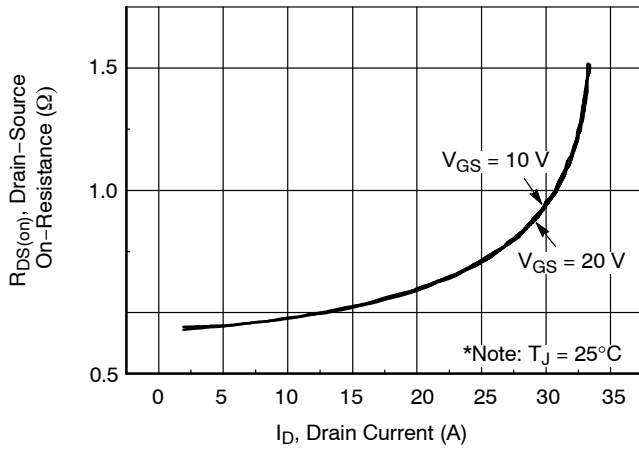


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

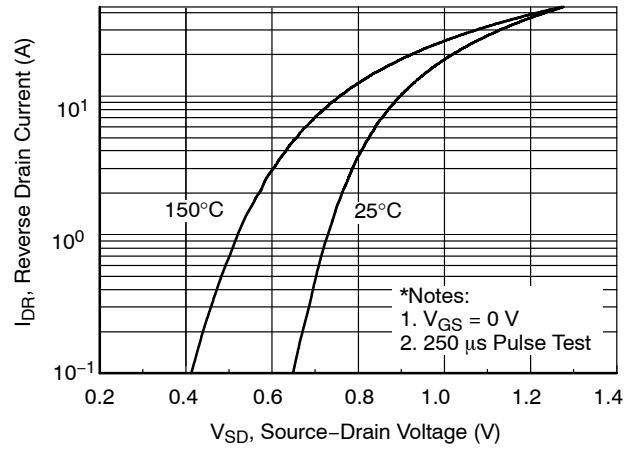


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

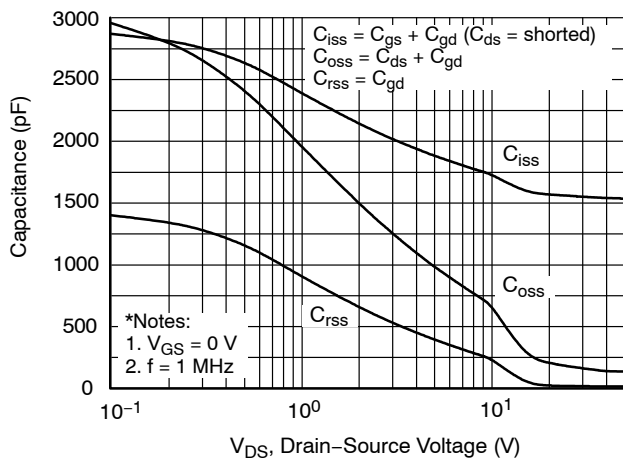


Figure 5. Capacitance Characteristics

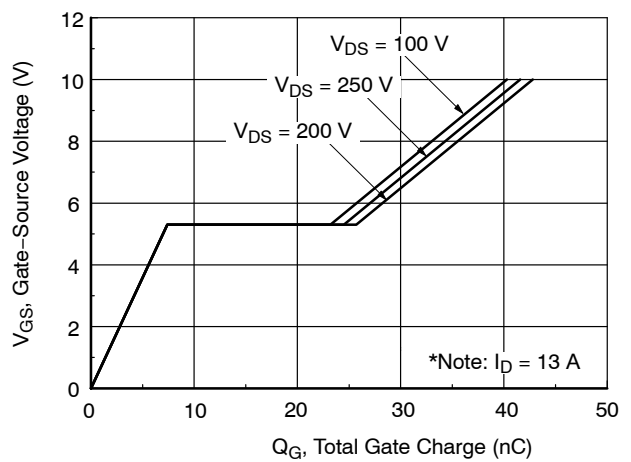


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS (continued)

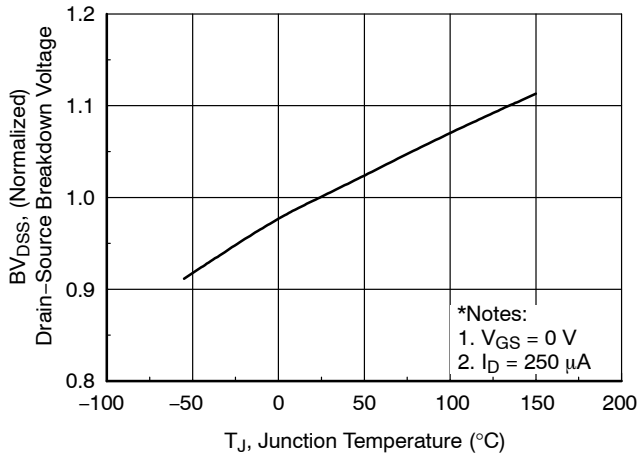


Figure 7. Breakdown Voltage Variation vs Temperature

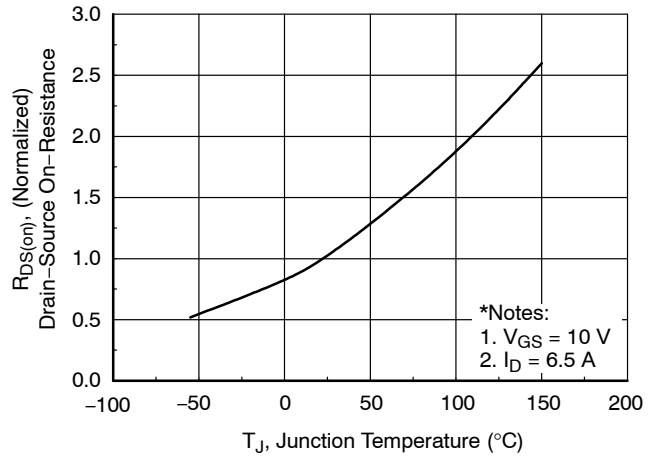


Figure 8. On-Resistance Variation vs Temperature

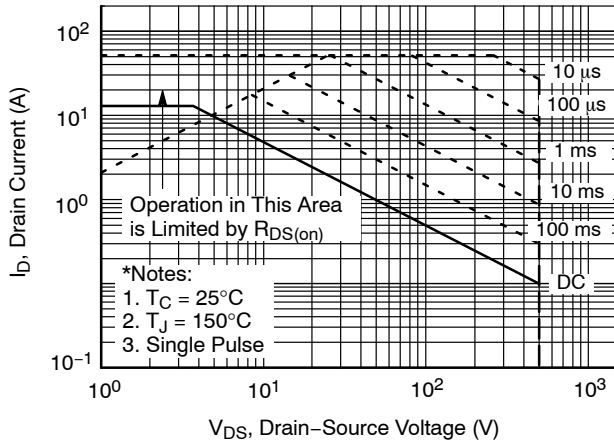


Figure 9. Maximum Safe Operating Area

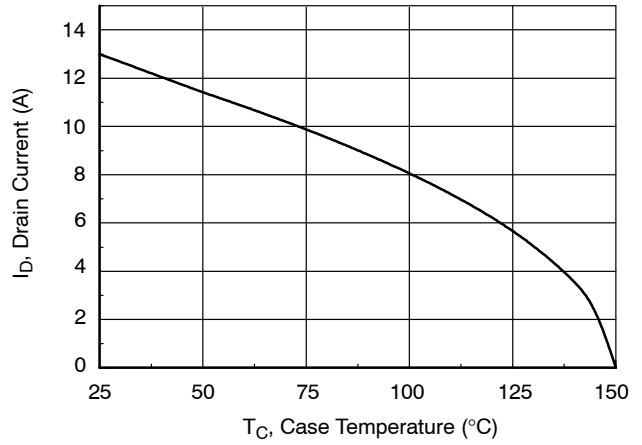


Figure 10. Maximum Drain Current vs Case Temperature

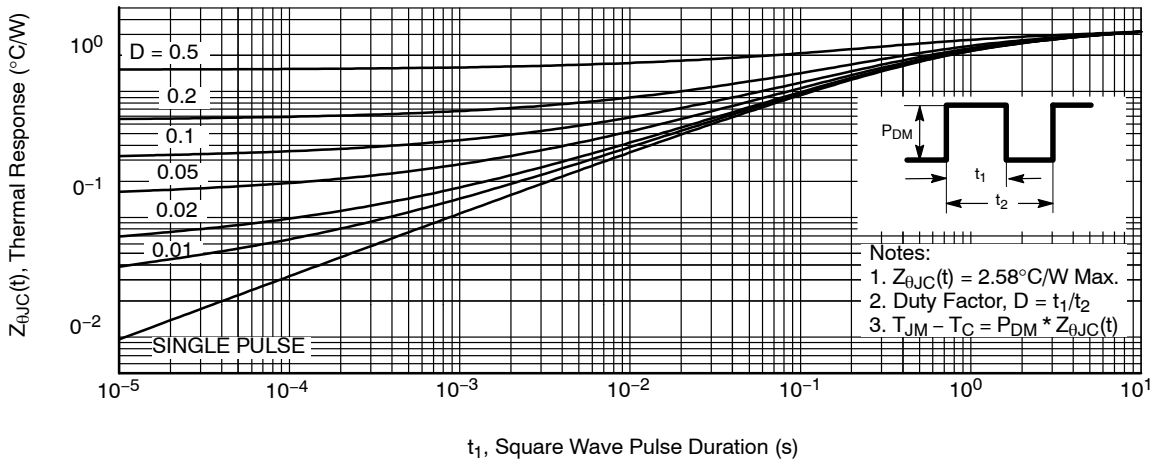


Figure 11. Transient Thermal Response Curve

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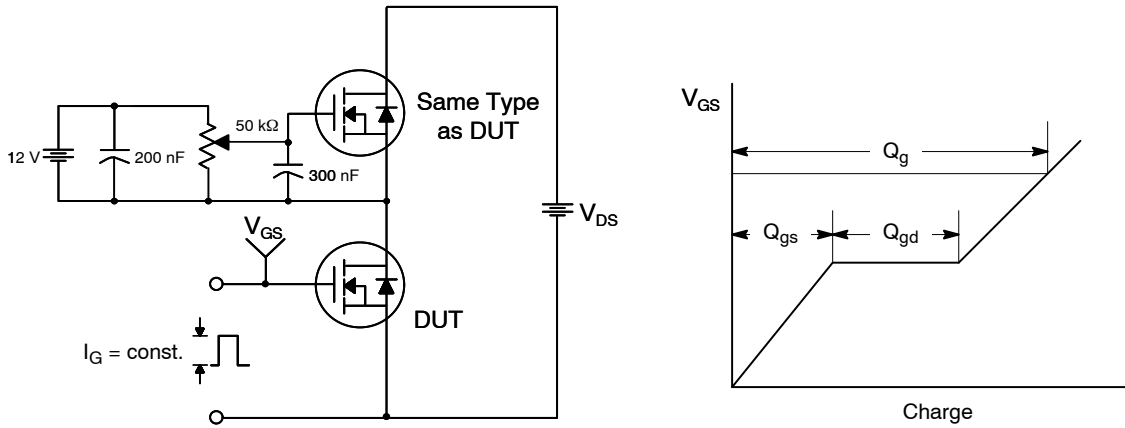


Figure 12. Gate Charge Test Circuit & Waveform

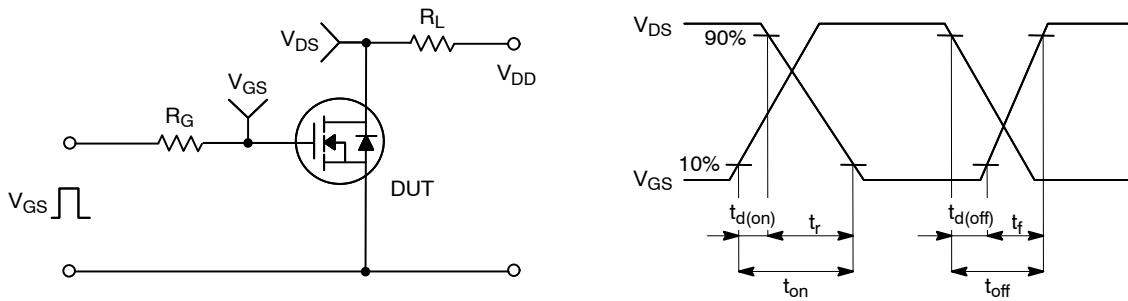


Figure 13. Resistive Switching Test Circuit & Waveforms

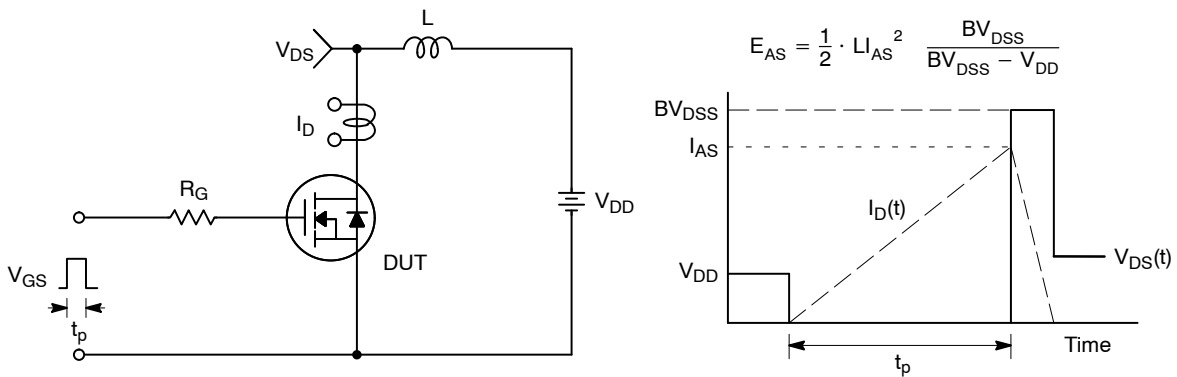


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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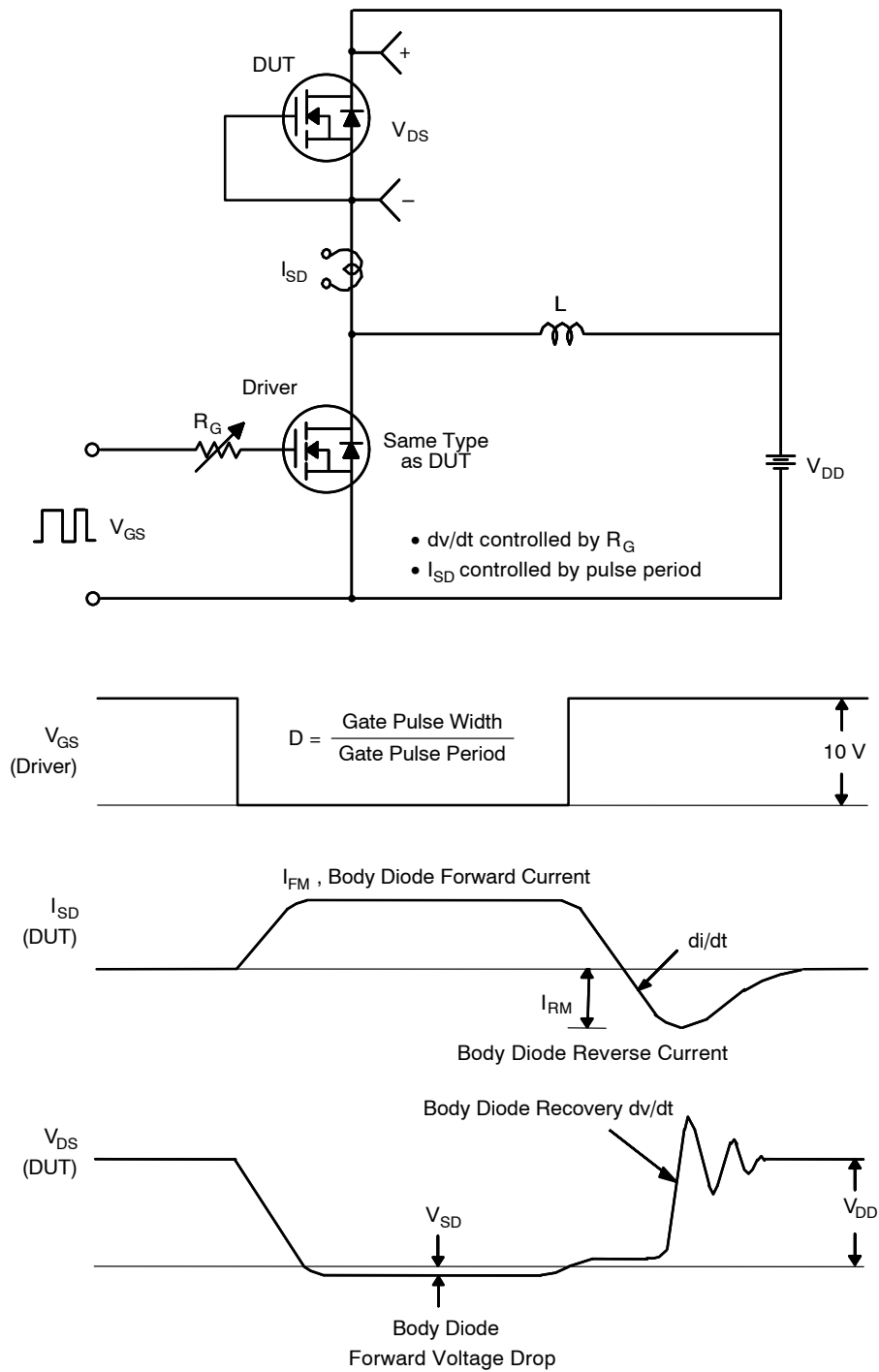


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

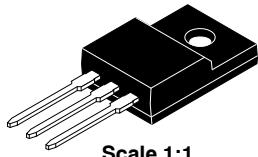
PACKAGE DIMENSIONS

ON Semiconductor®

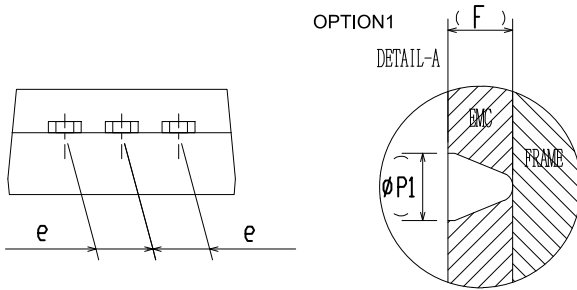
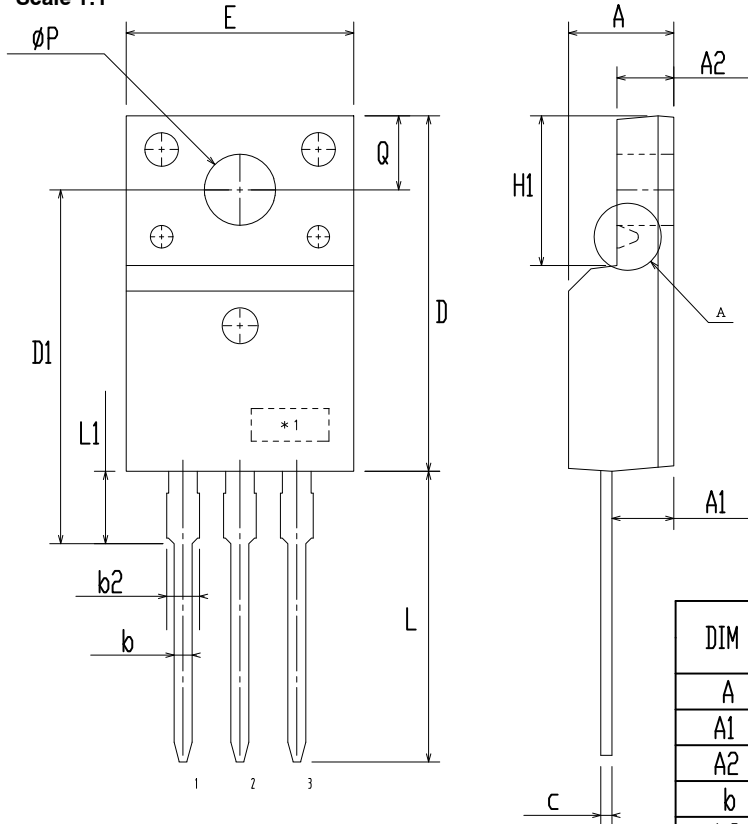


TO-220 Fullpack, 3-Lead / TO-220F-3SG
CASE 221AT
ISSUE B

DATE 19 JAN 2021



Scale 1:1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
phi P	2.98	3.18	3.38
phi P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.
- C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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DESCRIPTION:	TO-220 FULLPACK, 3-LEAD / TO-220F-3SG	PAGE 1 OF 1

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