

MOSFET – P-Channel, QFET®

-60 V, -47 A, 26 mΩ

FQP47P06

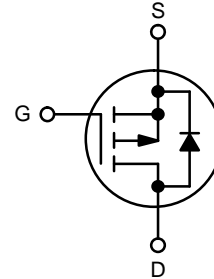
Description

This P-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

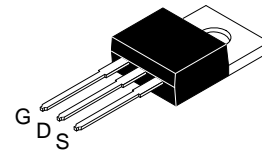
Features

- -47 A, -60 V, $R_{DS(on)} = 26 \text{ m}\Omega$ (Max.) @ $V_{GS} = -10 \text{ V}$, $I_D = -23.5 \text{ A}$
- Low Gate Charge (Typ. 84 nC)
- Low Crss (Typ. 320 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
-60 V	26 mΩ @ -10 V	-47 A

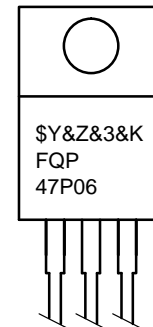


P-Channel MOSFET



TO-220-3LD
CASE 340AT

MARKING DIAGRAM



- \$Y = Logo
- &Z = Assembly Plant Code
- &3 = 3-Digit Plant Code
- &K = 2-Digits Lot Run Traceability Code
- FQP47P06 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FQP47P06	TO-220-3LD	1000 Units / Tube

FQP47P06

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	FQP47P06	Unit	
V_{DSS}	Drain–Source Voltage	–60	V	
I_D	Drain Current	– Continuous ($T_C = 25^\circ\text{C}$)	–47	A
		– Continuous ($T_C = 100^\circ\text{C}$)	–33.2	A
I_{DM}	Drain Current (Note 1)	– Pulsed	–188	A
V_{GSS}	Gate–Source Voltage	± 25	V	
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	820	mJ	
I_{AR}	Avalanche Current (Note 1)	–47	A	
E_{AR}	Repetitive Avalanche Energy (Note 1)	16	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)	–7.0	V/ns	
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)		160	W
		– Derate above 25°C	1.06	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to +175	$^\circ\text{C}$	
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 0.43\text{ mH}$, $I_{AS} = -47\text{ A}$, $V_{DD} = -25\text{ V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq -47\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Characteristic	FQP47P06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case, Max.	0.94	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case–to–Sink, Typ.	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

FQP47P06

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = –250 μA	–60	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C	–	–0.06	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = –60 V, V _{GS} = 0 V	–	–	–1	μA
		V _{DS} = –48 V, T _C = 150°C	–	–	–10	μA
I _{GSSF}	Gate–Body Leakage Current, Forward	V _{GS} = –25 V, V _{DS} = 0 V	–	–	–100	nA
I _{GSSR}	Gate–Body Leakage Current, Reverse	V _{GS} = 25 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = –250 μA	–2.0	–	–4.0	V
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = –10 V, I _D = –23.5 A	–	0.021	0.026	Ω
g _{FS}	Forward Transconductance	V _{DS} = –30 V, I _D = –23.5 A (Note 4)	–	21	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = –25 V, V _{GS} = 0 V, f = 1.0 MHz	–	2800	3600	pF
C _{oss}	Output Capacitance		–	1300	1700	pF
C _{rss}	Reverse Transfer Capacitance		–	320	420	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn–On Delay Time	V _{DD} = –30 V, I _D = –23.5 A, R _G = 25 Ω (Note 4, 5)	–	50	110	ns
t _r	Turn–On Rise Time		–	450	910	ns
t _{d(off)}	Turn–Off Delay Time		–	100	210	ns
t _f	Turn–Off Fall Time		–	195	400	ns
Q _g	Total Gate Charge	V _{DS} = –48 V, I _D = –47 A, V _{GS} = –10 V (Note 4, 5)	–	84	110	nC
Q _{gs}	Gate–Source Charge		–	18	–	nC
Q _{gd}	Gate–Drain Charge		–	44	–	nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATING

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–47	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current		–	–	–188	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –47 A	–	–	–4.0	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = –47 A, dI _F / dt = 100 A/μs (Note 4)	–	130	–	ns
Q _{rr}	Reverse Recovery Charge		–	0.55	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width ≤ 300 μs, Duty cycle ≤ 2%

5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

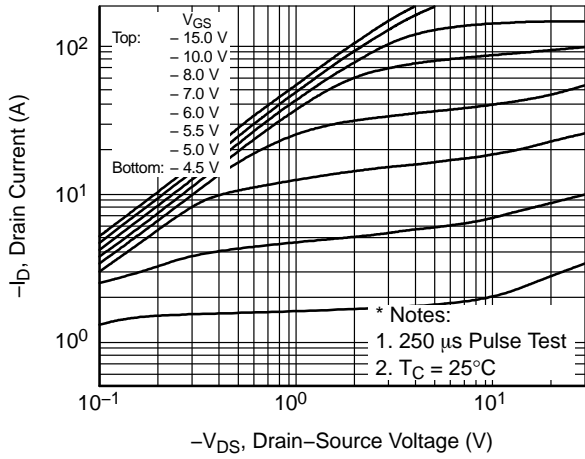


Figure 1. On-Region Characteristics

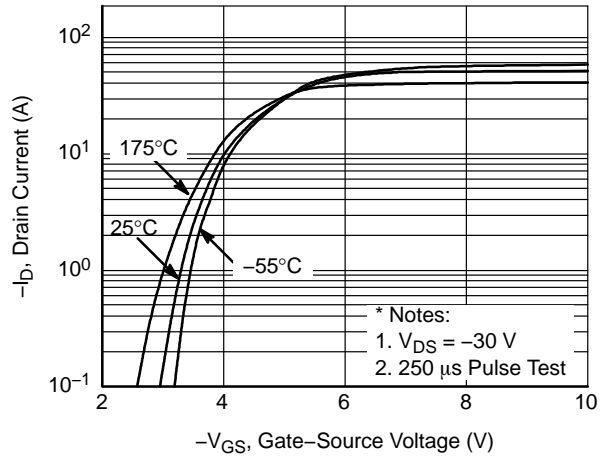


Figure 2. Transfer Characteristics

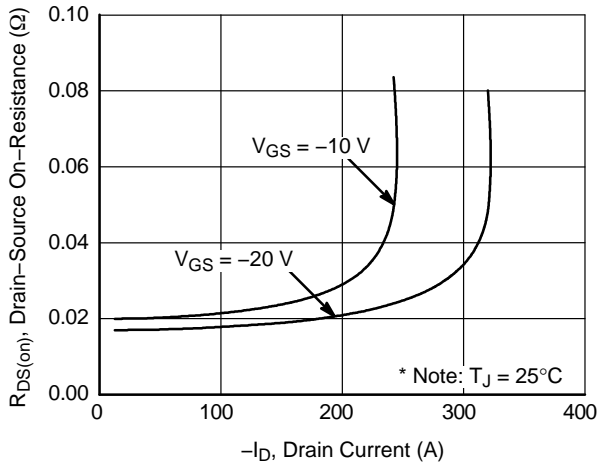


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

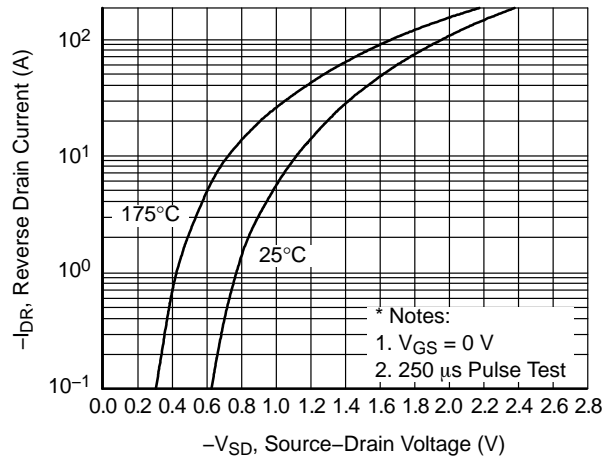


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

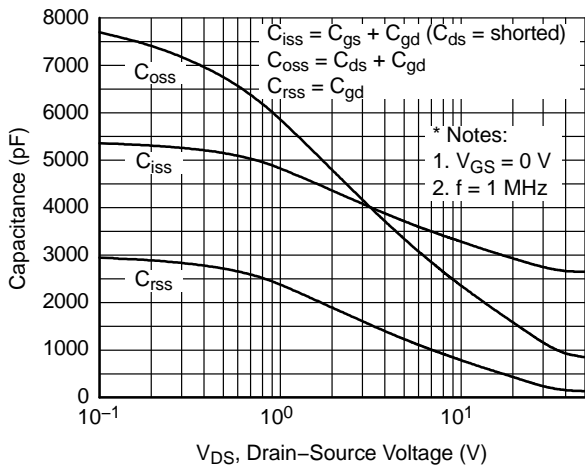


Figure 5. Capacitance Characteristics

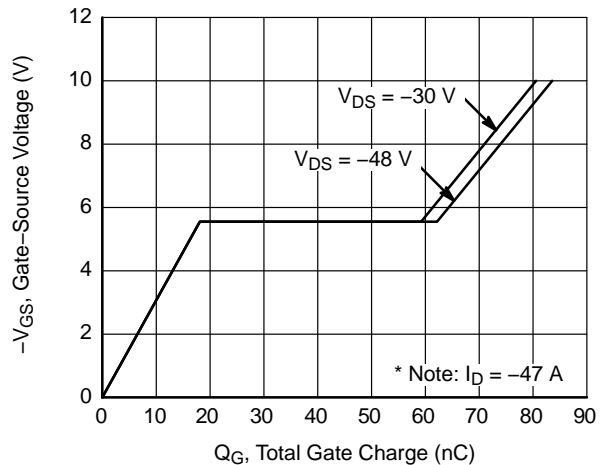


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (Continued)

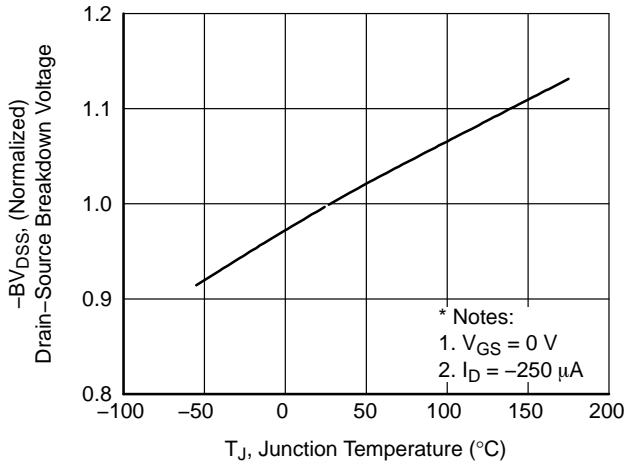


Figure 7. Breakdown Voltage Variation vs. Temperature

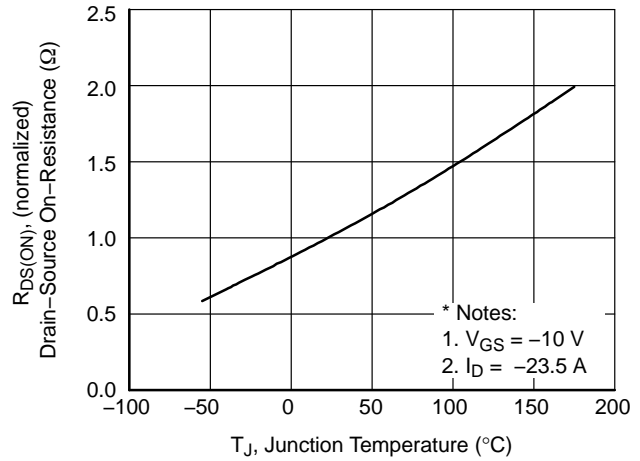


Figure 8. On-Resistance Variation vs. Temperature

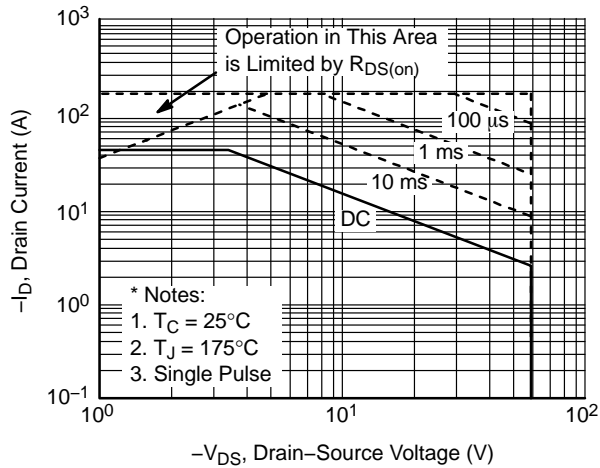


Figure 9. Maximum Safe Operating Area

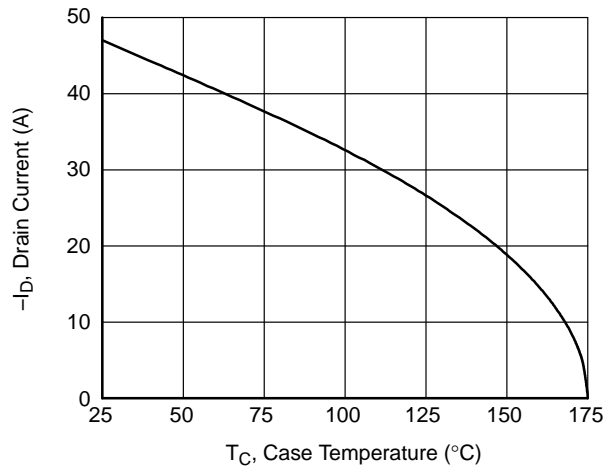


Figure 10. Maximum Drain Current vs. Case Temperature

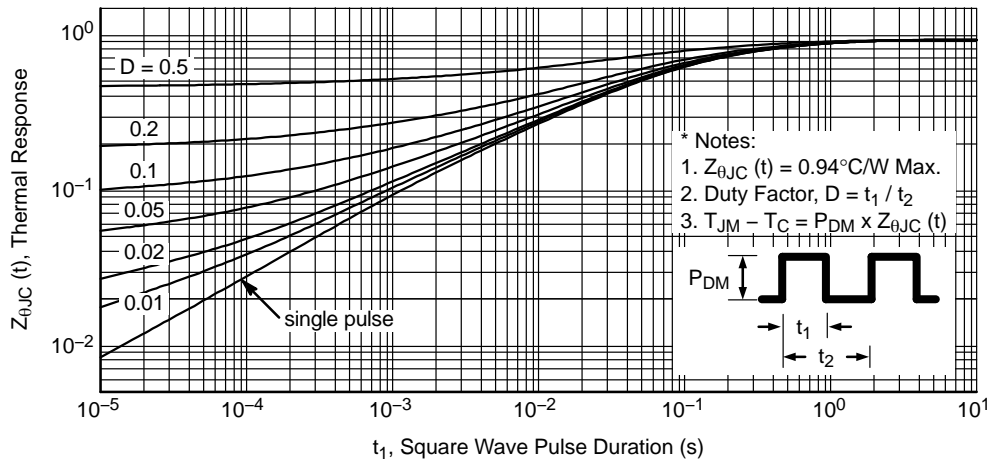


Figure 11. Transient Thermal Response Curve

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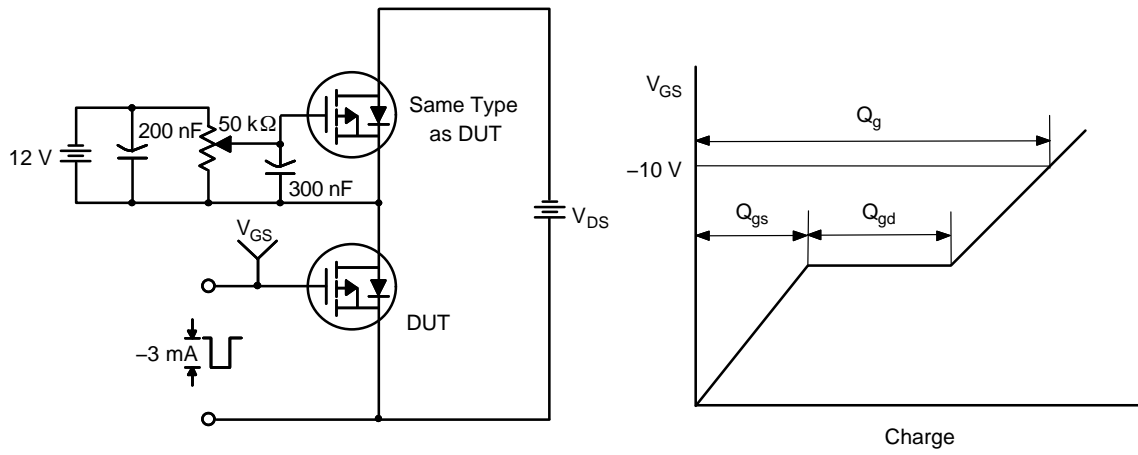


Figure 12. Gate Charge Test Circuit & Waveform

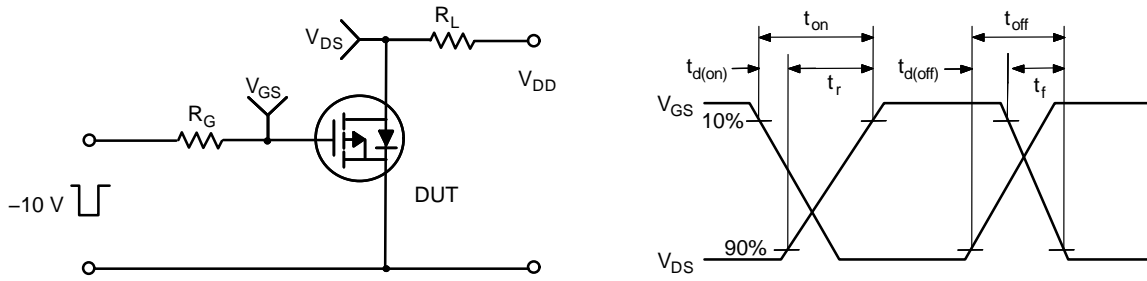


Figure 13. Resistive Switching Test Circuit & Waveforms

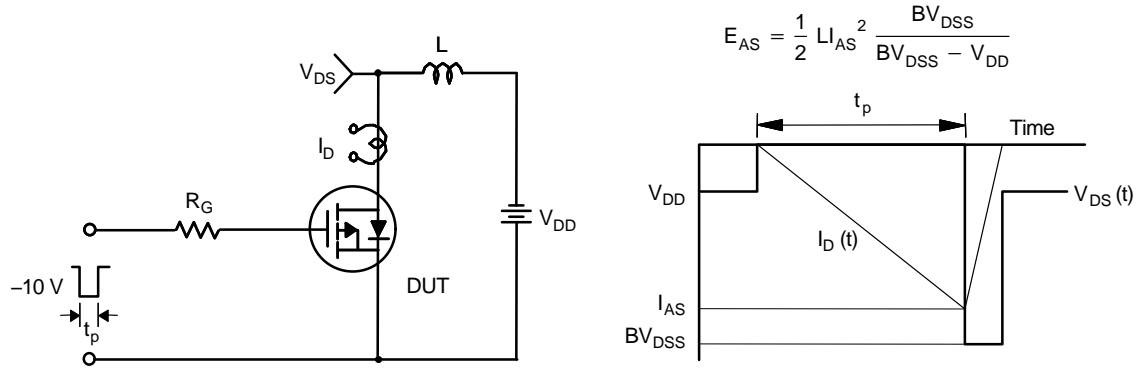


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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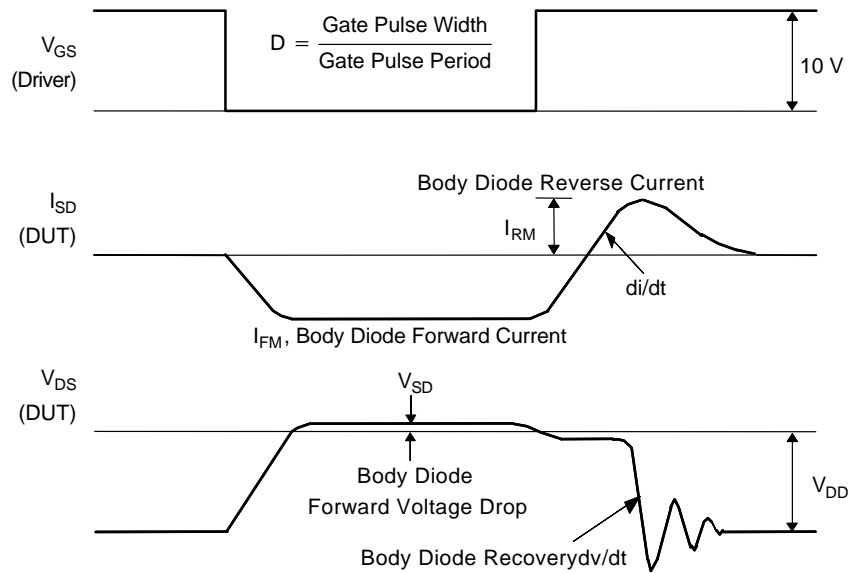
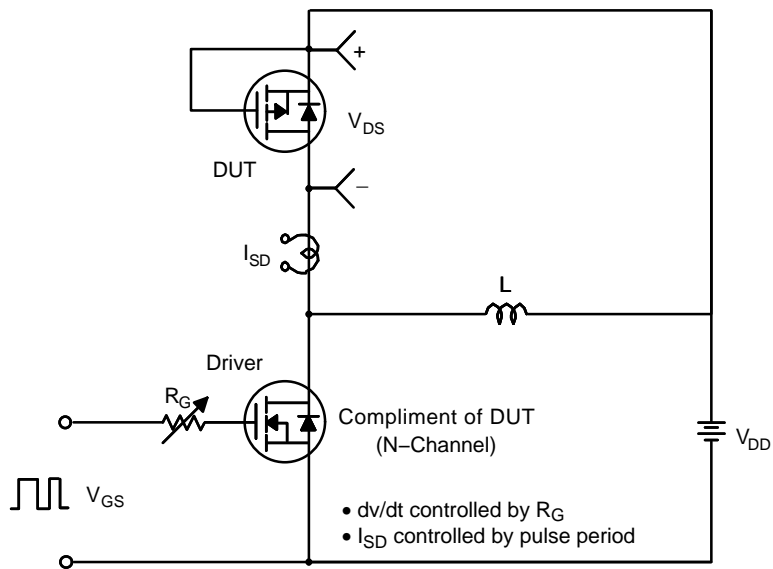
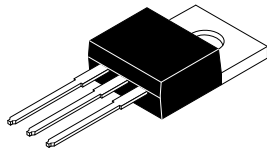


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



Scale 1:1

TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



- NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
 - D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
 - E) DOES NOT COMPLY JEDEC STANDARD VALUE.
 - F) "A1" DIMENSIONS AS BELOW:
 SINGLE GAUGE = 0.51 - 0.61
 DUAL GAUGE = 1.10 - 1.45
 - G) PRESENCE IS SUPPLIER DEPENDENT
 - H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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