

# MOSFET – N-Channel, QFET

200 V, 19.4 A, 150 mΩ

## FQP19N20

### Description

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 19.4 A, 200 V,  $R_{DS(on)}$  = 150 mΩ (Max.) @  $V_{GS} = 10$  V,  $I_D = 9.7$  A
- Low Gate Charge (Typ. 31 nC)
- Low  $C_{rss}$  (Typ. 30 pF)
- 100% Avalanche Tested

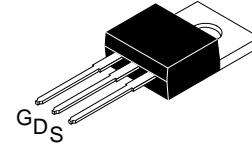
### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter		FQP19N20	Unit
$V_{DSS}$	Drain-Source Voltage		200	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	19.4	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	12.3	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	78	A
$V_{GSS}$	Gate-Source Voltage		$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)		250	mJ
$I_{AR}$	Avalanche Current (Note 1)		19.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)		14	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		5.5	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	140	W
		- Derate above $25^\circ\text{C}$	1.12	
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

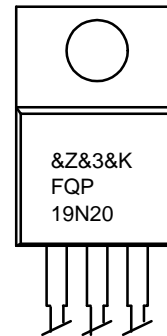
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $L = 1.0$  mH,  $I_{AS} = 19.4$  A,  $V_{DD} = 50$  V,  $R_G = 25$  Ω, starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 19.4$  A,  $di/dt \leq 300$  A/ $\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .

$V_{DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
200 V	150 mΩ @ 10 V	19.4 A



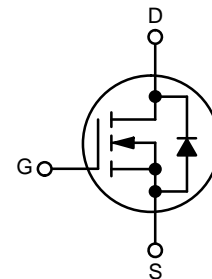
TO-220-3LD  
CASE 340AT

### MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code
- &K = 2-Digits Lot Run Traceability Code
- FQP19N20 = Specific Device Code

### N-CHANNEL MOSFET



### ORDERING INFORMATION

Part Number	Package	Shipping
FQP19N20	TO-220-3LD (Pb-Free, Halide Free)	1000 Units / Tube

# FQP19N20

## THERMAL CHARACTERISTICS

Symbol	Parameter	FQP19N20	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.89	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	200	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$	-	0.18	-	$\text{V}/^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, T_C = 125^{\circ}\text{C}$	-	-	10	
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 9.7\text{ A}$	-	0.12	0.15	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 9.7\text{ A}$	-	14.5	-	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	1220	1600	pF
$C_{oss}$	Output Capacitance		-	220	290	pF
$C_{rss}$	Reverse Transfer Capacitance		-	30	40	pF

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}, I_D = 19.4\text{ A}, R_G = 25\ \Omega$ (Note 4)	-	20	50	ns
$t_r$	Turn-On Rise Time		-	190	390	ns
$t_{d(off)}$	Turn-Off Delay Time		-	55	120	ns
$t_f$	Turn-Off Fall Time		-	80	170	ns
$Q_g$	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 19.4\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	31	40	nC
$Q_{gs}$	Gate-Source Charge		-	8.6	-	nC
$Q_{gd}$	Gate-Drain Charge		-	13.5	-	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

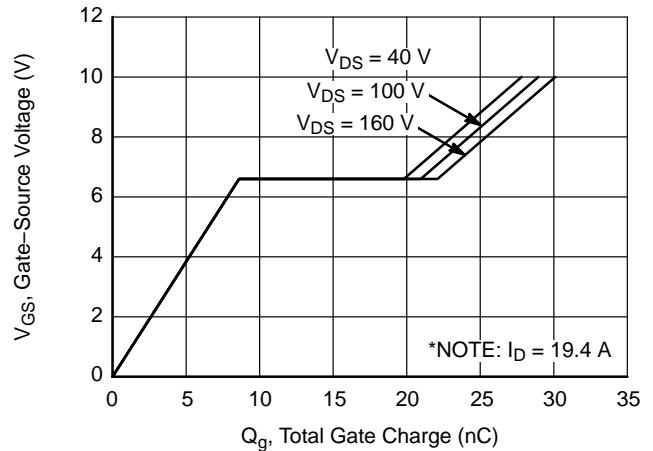
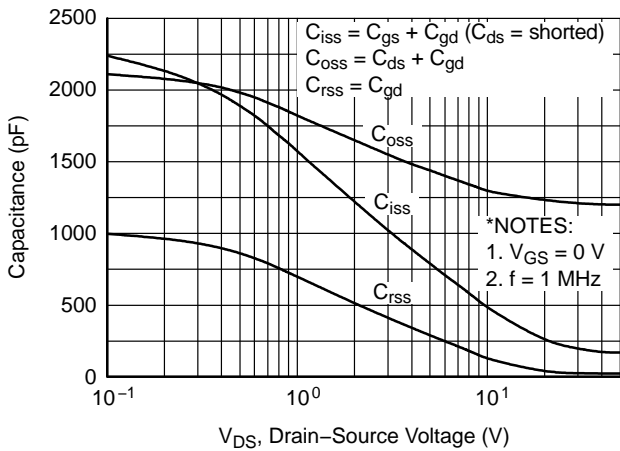
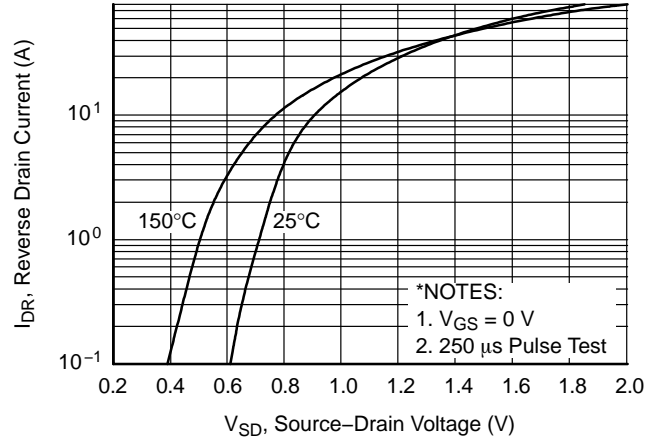
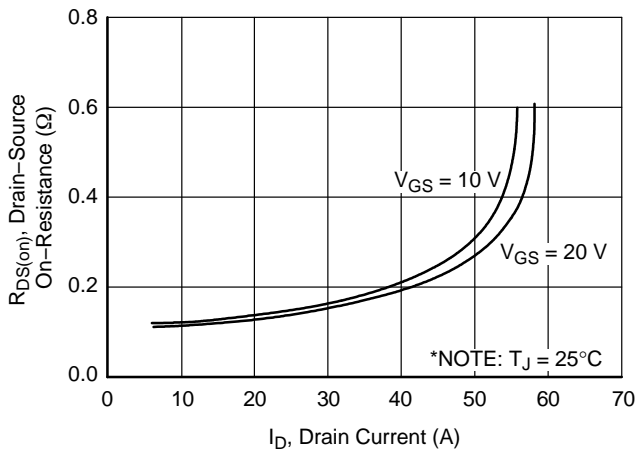
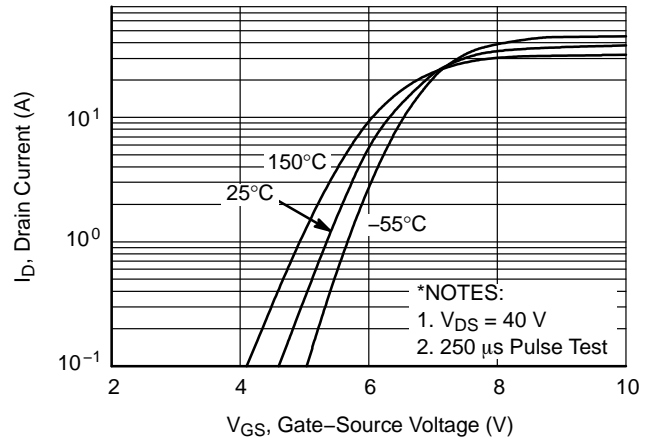
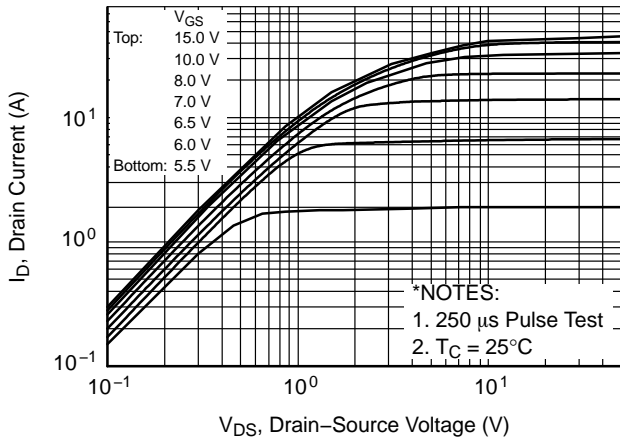
$I_S$	Maximum Continuous Drain-Source Diode Forward Current	-	-	19.4	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	-	-	78	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 19.4\text{ A}$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 19.4\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	140	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	0.69	-	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature

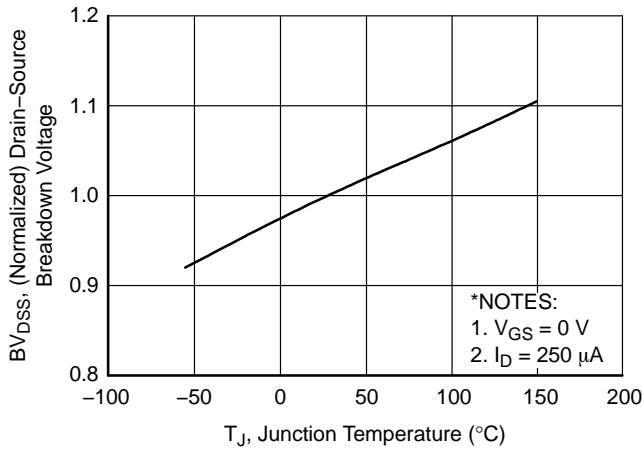
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## TYPICAL CHARACTERISTICS

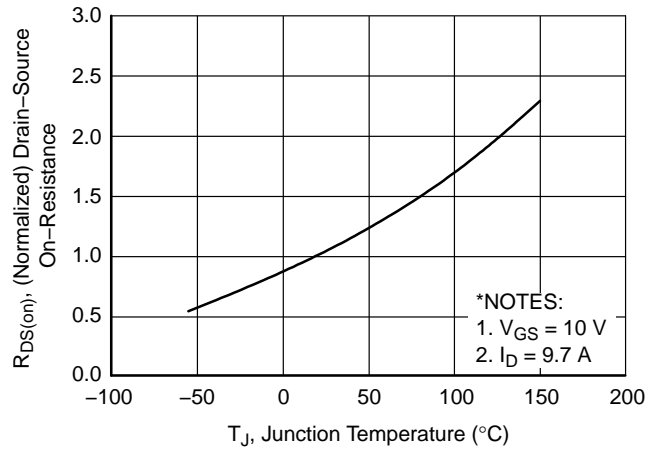


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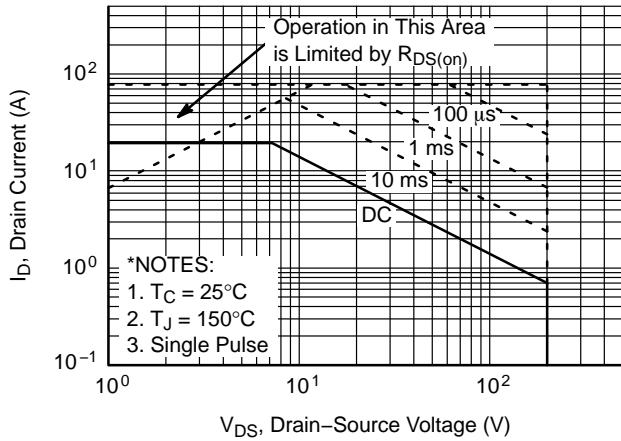
## TYPICAL CHARACTERISTICS (CONTINUED)



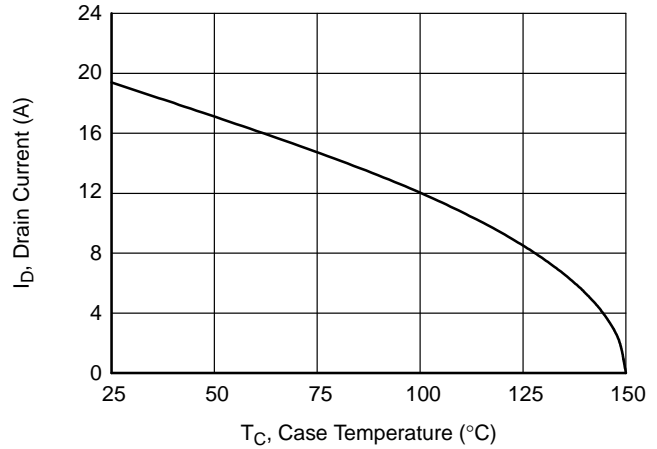
**Figure 7. Breakdown Voltage Variation vs. Temperature**



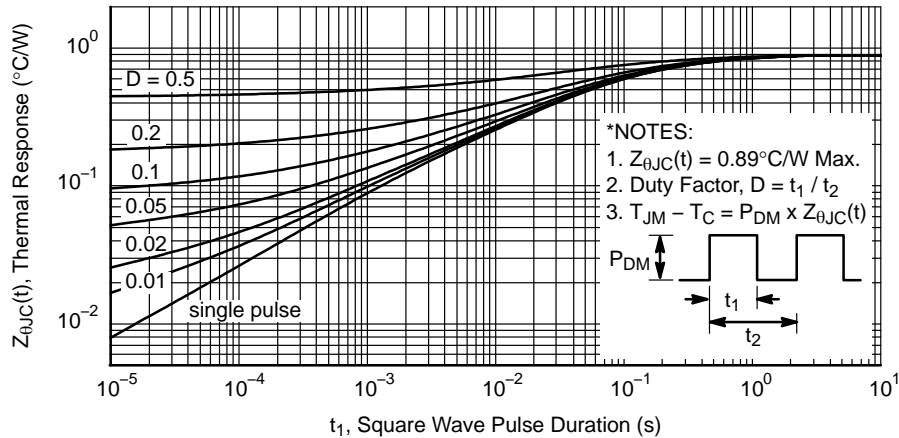
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

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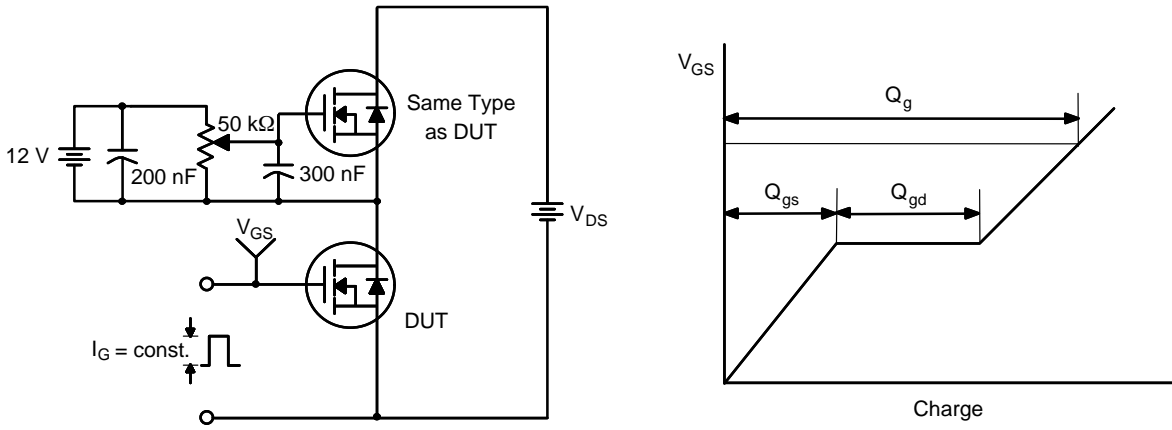


Figure 12. Gate Charge Test Circuit & Waveform

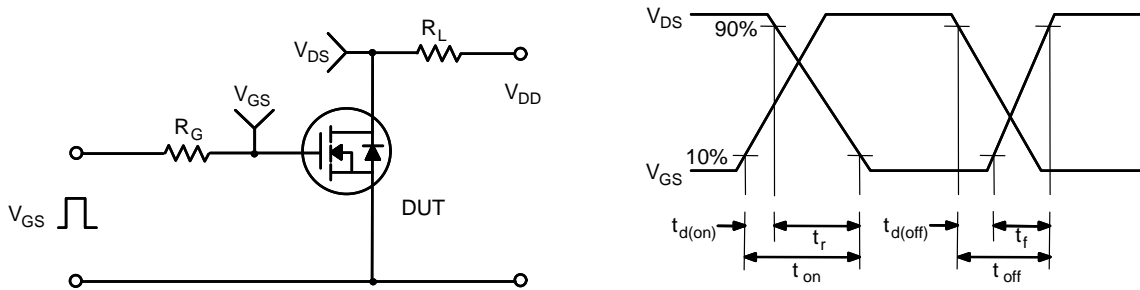


Figure 13. Resistive Switching Test Circuit & Waveforms

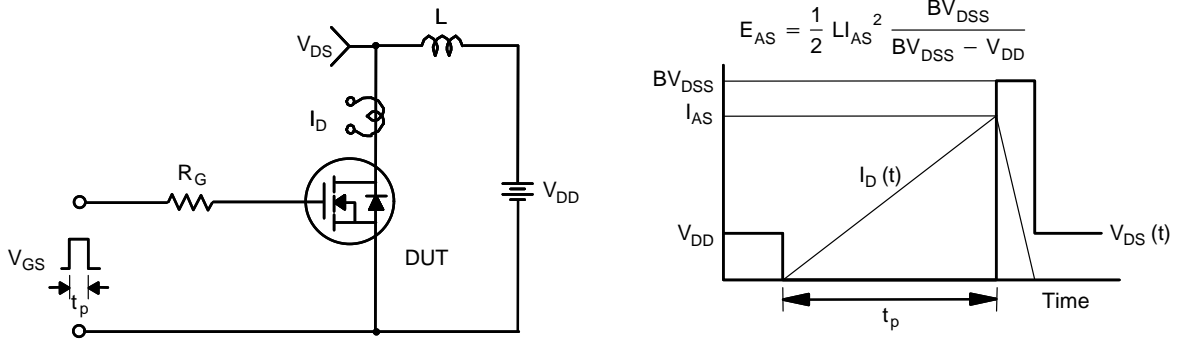
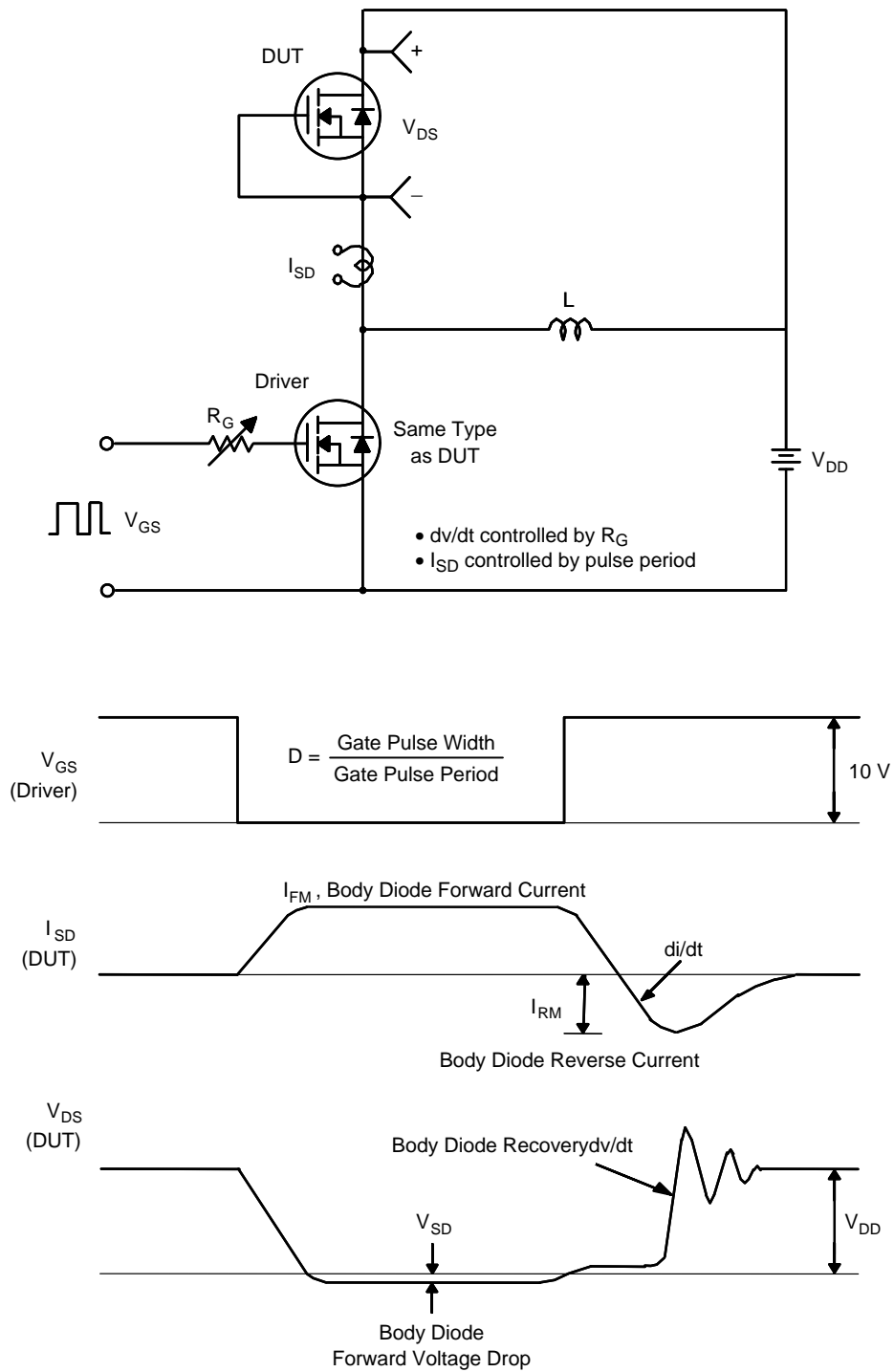
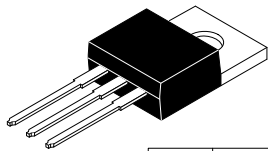


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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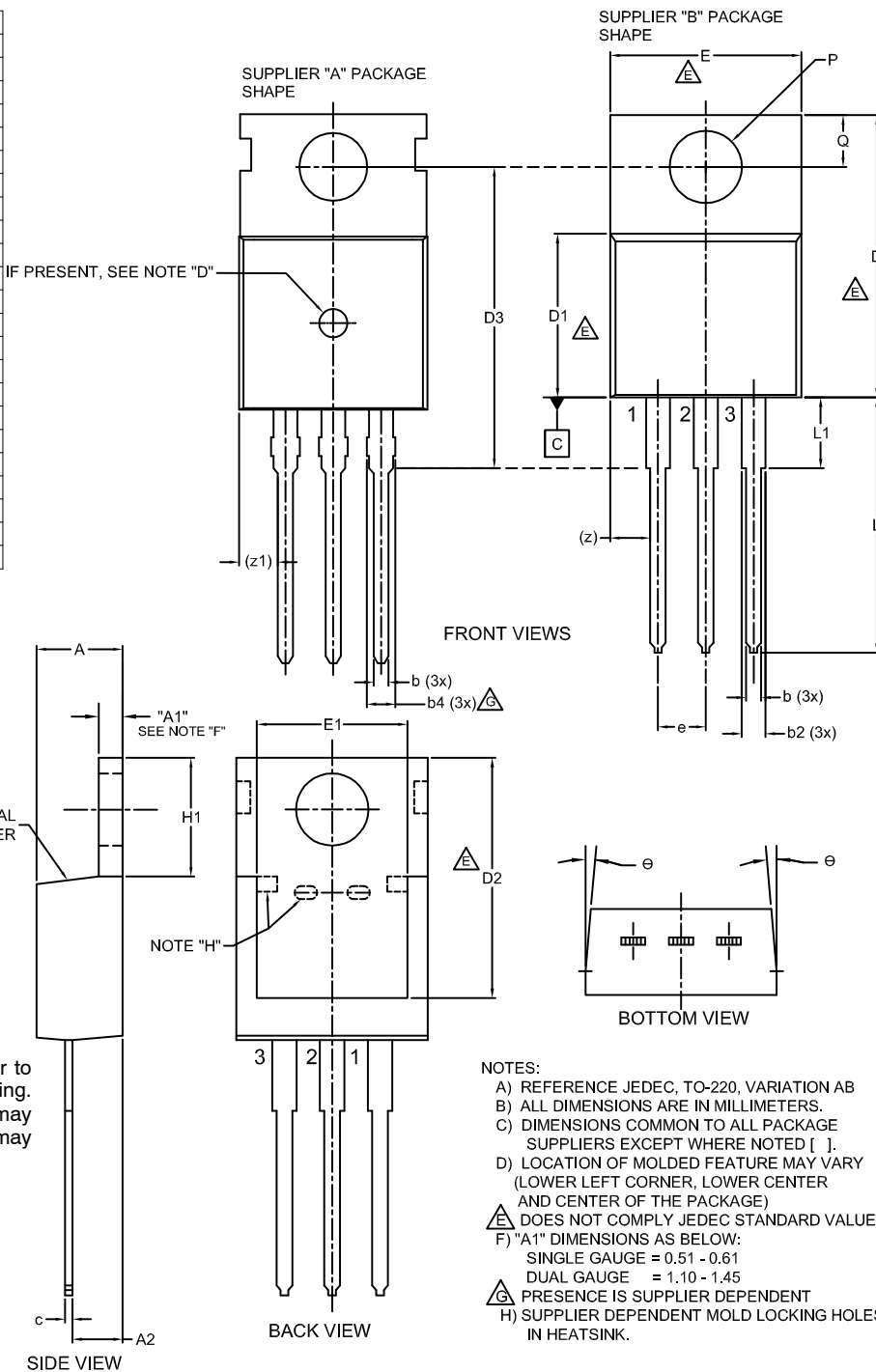
**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**



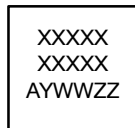
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CASE 340AT  
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°



GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- ⚠ DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:  
 SINGLE GAUGE = 0.51 - 0.61  
 DUAL GAUGE = 1.10 - 1.45
- ⚠ PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	TO-220-3LD	PAGE 1 OF 1

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