

MOSFET – N-Channel, QFET®

100 V, 48 A, 39 mΩ

FQH44N10

Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

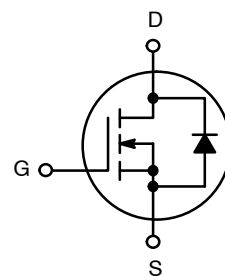
- 48 A, 100 V, $R_{DS(on)} = 39 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 24 \text{ A}$
- Low Gate Charge (Typ. 48 nC)
- Low C_{rss} (Typ. 85 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



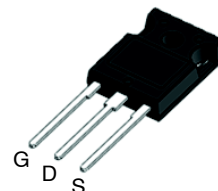
ON Semiconductor®

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V_{DS}	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	39 mΩ @ 10 V	48 A

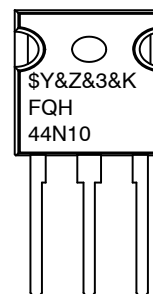


POWER MOSFET



**TO-247-3LD
CASE 340CK**

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FQH44N10	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FQH44N10

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		FQH44N10-133	Unit
V _{DSS}	Drain-Source Voltage		100	V
I _D	Drain Current	Continuous (T _C = 25°C)	48	A
		Continuous (T _C = 100°C)	34	
I _{DM}	Drain Current	Pulsed (Note 1)	192	A
V _{GSS}	Gate-Source Voltage		±25	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		530	mJ
I _{AR}	Avalanche Current (Note 1)		48	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		18	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P _D	Power Dissipation	(T _C = 25°C)	180	W
		Derate Above 25°C	1.2	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T _L	Maximum Lead Temperature for Soldering Purpose 1/8" from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. L = 0.345 mH, I_{AS} = 48 A, V_{DD} = 25 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 43.5 A, di/dt ≤ 300 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FQH44N10-133	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.83	°C/W
R _{θCS}	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQH44N10-133	FQH44N10	TO-247	Tube	N/A	N/A	30 Units

FQH44N10

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		0.1		V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 80\text{ V}, T_C = 150^\circ\text{C}$			10	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0		4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}$		0.03	0.039	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 24\text{ A}$		31		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		1400	1800	pF
C_{oss}	Output Capacitance			425	550	pF
C_{rss}	Reverse Transfer Capacitance			85	110	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 43.5\text{ A}, R_g = 25\text{ }\Omega$ (Note 4)		19	45	ns
t_r	Turn-On Rise Time			190	390	ns
$t_{d(off)}$	Turn-Off Delay Time			90	190	ns
t_f	Turn-Off Fall Time			100	210	ns
Q_g	Total Gate Charge	$V_{DS} = 80\text{ V}, I_D = 43.5\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)		48	62	nC
Q_{gs}	Gate-Source Charge			9.0		nC
Q_{gd}	Gate-Drain Charge			24		nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current				48	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current				192	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 48A			1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 43.5 A, dI _F /dt = 100 A/μs		98		ns
Q _{rr}	Reverse Recovery Charge			360		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

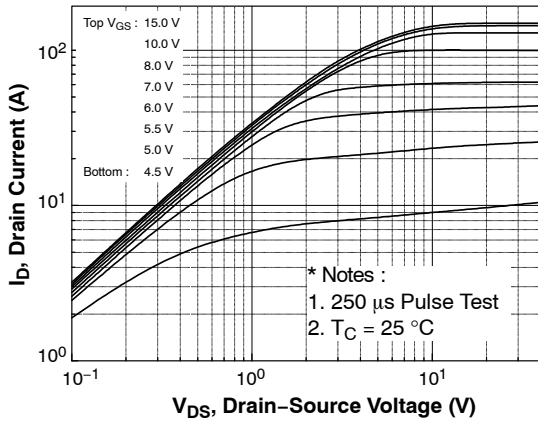


Figure 1. On-Region Characteristics

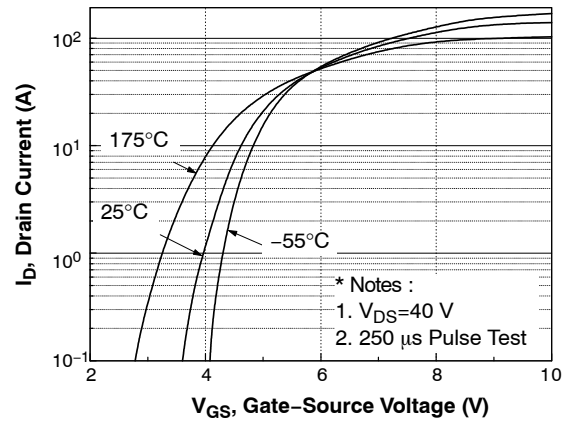


Figure 2. Transfer Characteristics

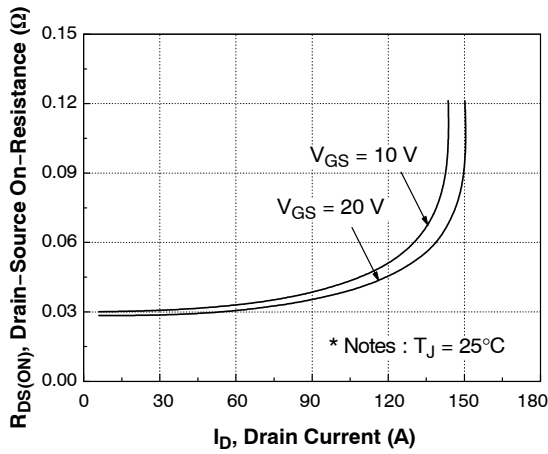


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

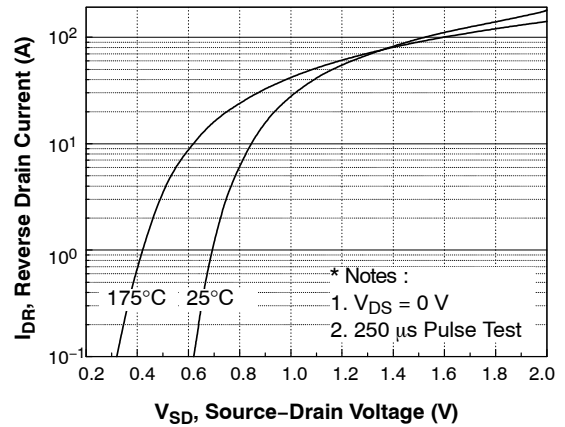


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

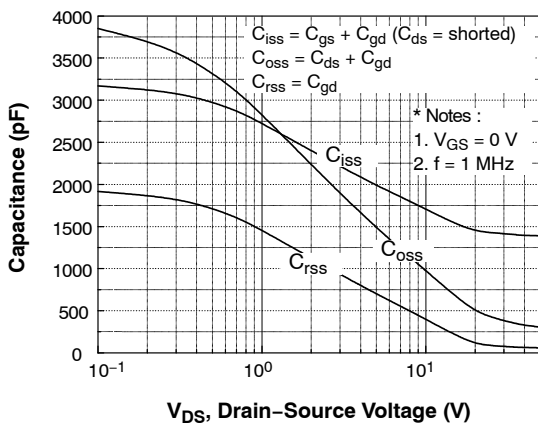


Figure 5. Capacitance Characteristics

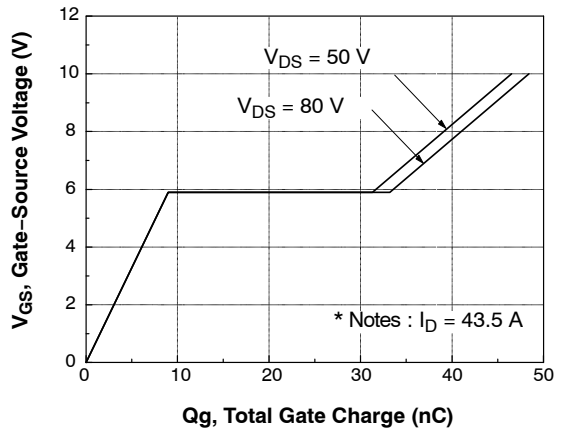
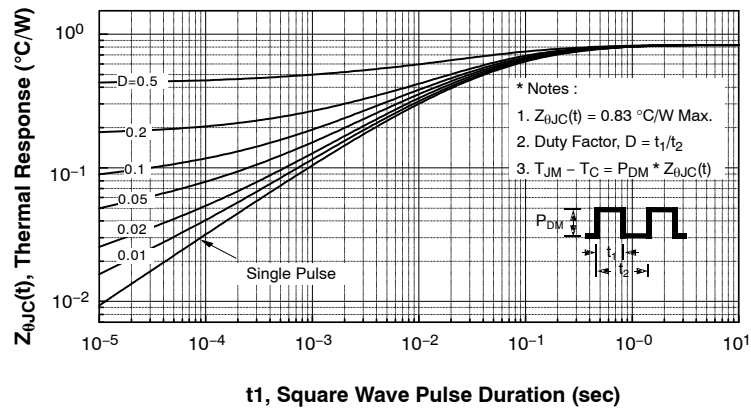
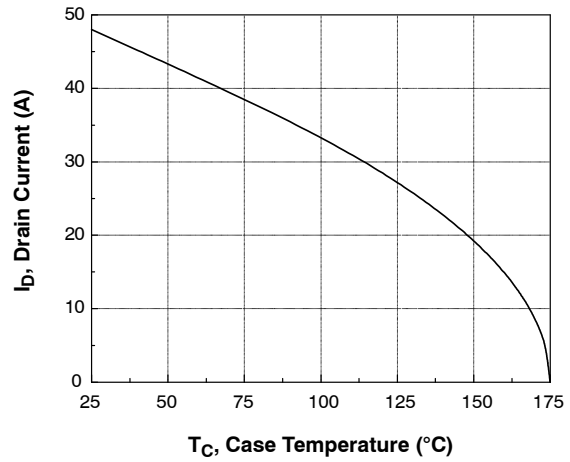
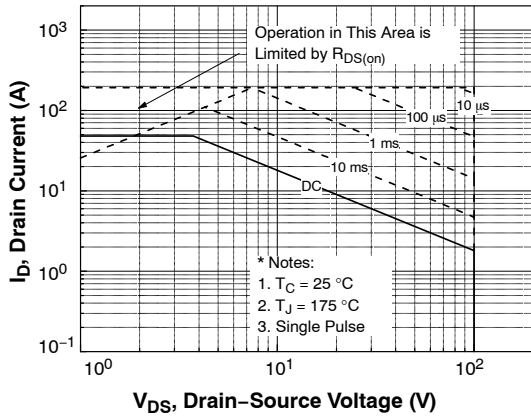
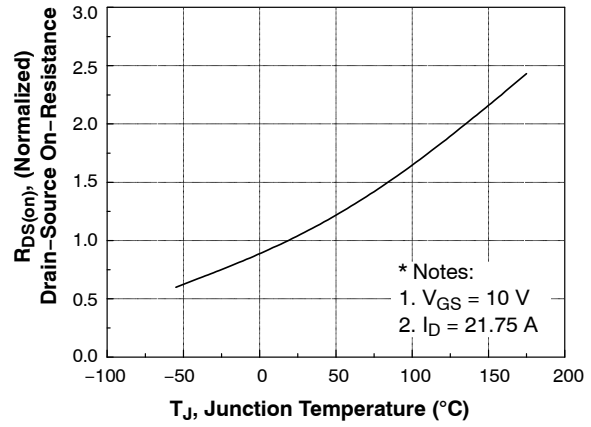
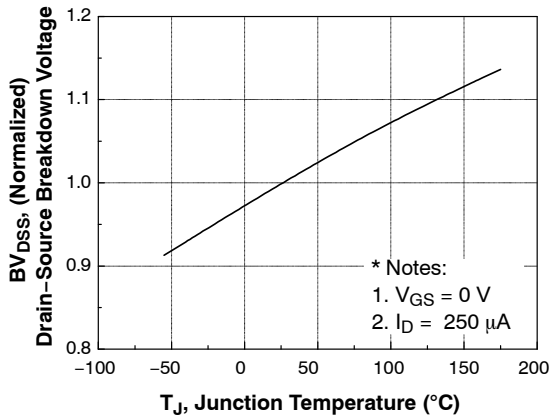


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



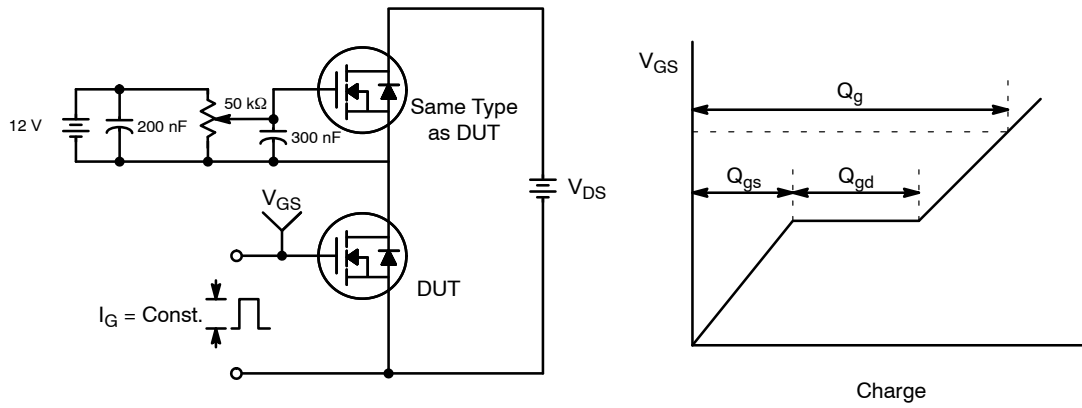


Figure 12. Gate Charge Test Circuit & Waveform

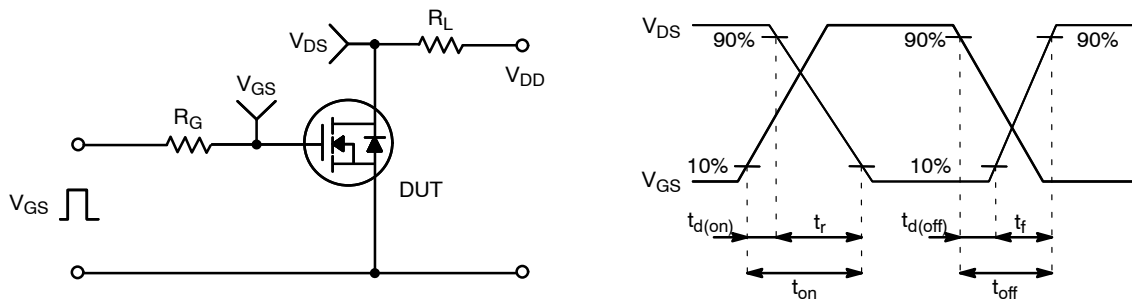


Figure 13. Resistive Switching Test Circuit & Waveforms

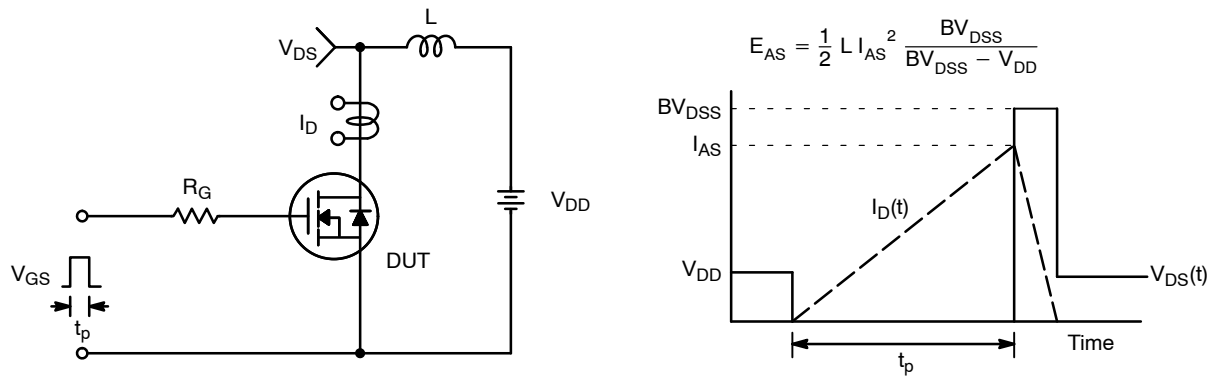


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

The top diagram shows a circuit for testing the body diode of a MOSFET. A MOSFET (DUT) is connected with its drain to a positive terminal and its source to a negative terminal. A current source I_{SD} is connected between the drain and source. A gate driver is connected to the gate of the MOSFET through a gate resistor R_G . The driver is a MOSFET of the same type as the DUT, with its gate driven by a square wave V_{GS} . The drain of the driver is connected to the source of the DUT. The drain of the DUT is connected to a load inductor L and a DC supply V_{DD} . The drain-source voltage of the DUT is V_{DS} . The current through the DUT is I_{SD} . The gate voltage V_{GS} is a square wave. The current I_{SD} is controlled by the pulse period of V_{GS} . The dv/dt is controlled by R_G .

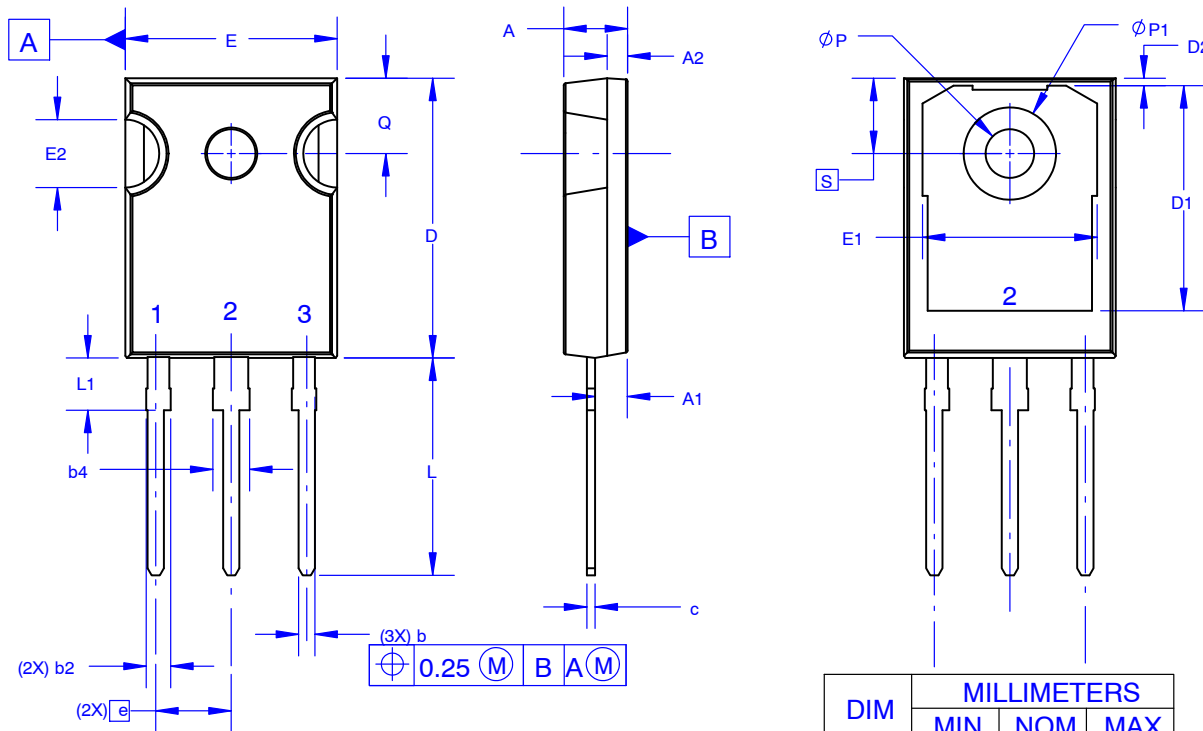
The bottom part of the figure shows three waveforms:

- V_{GS} (Driver):** A square wave pulse. The duty cycle is defined as $D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$. The pulse height is 10 V.
- I_{SD} (DUT):** The body diode forward current I_{FM} during the pulse. The reverse current I_{RM} is shown during the recovery phase. The di/dt is indicated by the slope of the current transition.
- V_{DS} (DUT):** The drain-source voltage. It shows the forward voltage drop V_{SD} and the recovery dv/dt during the reverse current phase. The peak voltage is V_{DD} .

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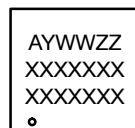
TO-247-3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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