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May 2014

FQA65N20

N-Channel QFET[®] MOSFET

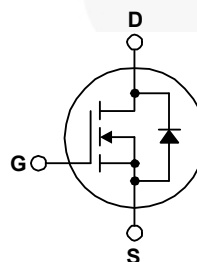
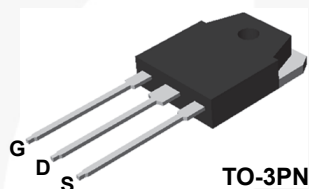
200 V, 65 A, 32 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 65 A, 200 V, $R_{DS(on)} = 32 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 32.5 \text{ A}$
- Low Gate Charge (Typ. 170 nC)
- Low C_{rss} (Typ. 90 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQA65N20	Unit
V_{DSS}	Drain-Source Voltage	200	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	65	A
	- Continuous ($T_C = 100^\circ\text{C}$)	41	A
I_{DM}	Drain Current - Pulsed (Note 1)	260	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1010	mJ
I_{AR}	Avalanche Current (Note 1)	65	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	31	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	310	W
	- Derate above 25°C	2.5	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQA65N20	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.4	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ	0.24	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA65N20	FQA65N20	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.15	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 160\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 32.5\text{ A}$	--	0.025	0.032	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 32.5\text{ A}$	--	58	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	6600	7900	pF
C_{oss}	Output Capacitance		--	1000	1200	pF
C_{rss}	Reverse Transfer Capacitance		--	90	120	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}, I_D = 65\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4)	--	120	250	ns
t_r	Turn-On Rise Time		--	640	770	ns
$t_{d(off)}$	Turn-Off Delay Time		--	340	690	ns
t_f	Turn-Off Fall Time		--	275	560	ns
Q_g	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 65\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	--	170	200	nC
Q_{gs}	Gate-Source Charge		--	45	--	nC
Q_{gd}	Gate-Drain Charge		--	75	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	65	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	260	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 65 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 65 A,	--	195	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	--	1.4	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. $L = 0.36\text{ mH}$, $I_{AS} = 65\text{ A}$, $V_{DD} = 50\text{ V}$, $R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 65\text{ A}$, $dI/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Characteristics

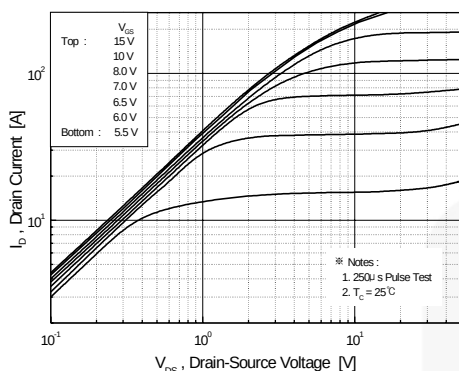


Figure 1. On-Region Characteristics

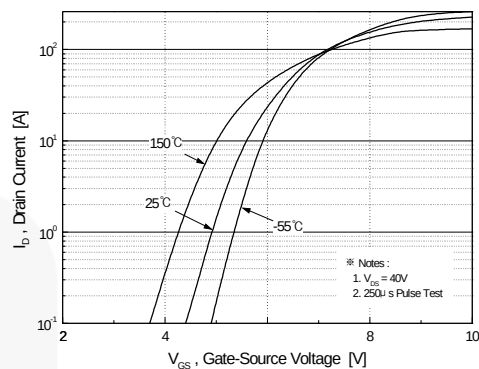


Figure 2. Transfer Characteristics

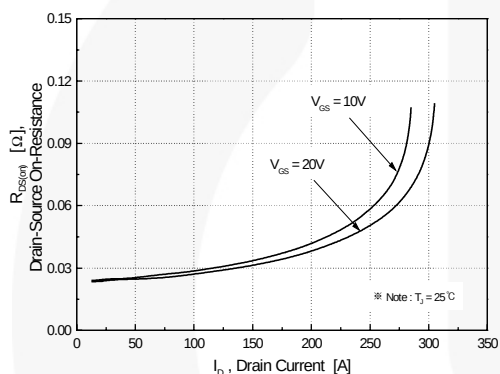


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

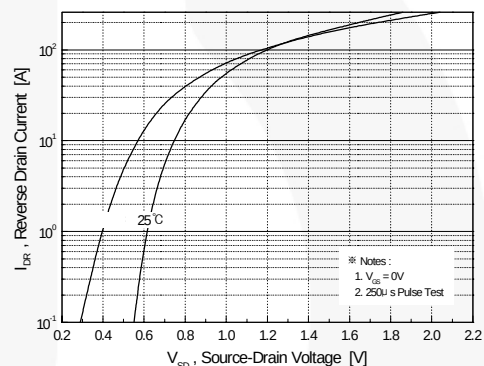


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

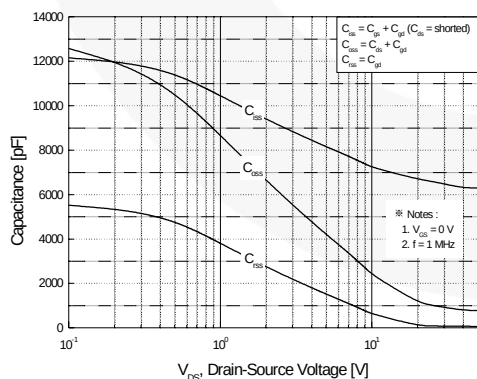


Figure 5. Capacitance Characteristics

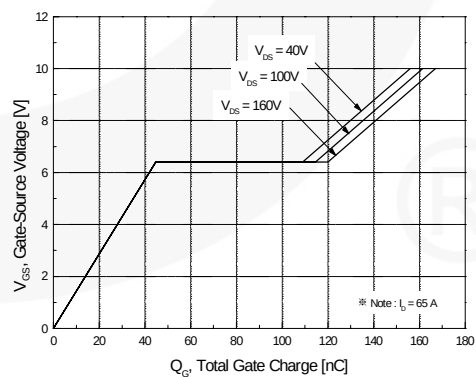


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

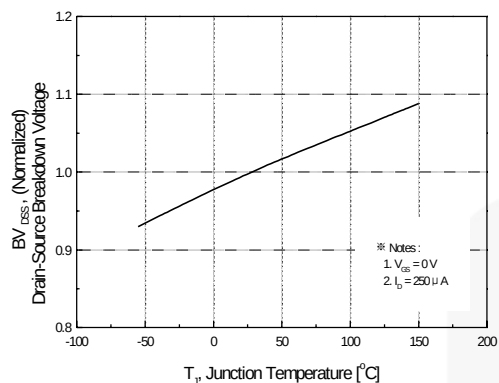


Figure 7. Breakdown Voltage Variation vs. Temperature

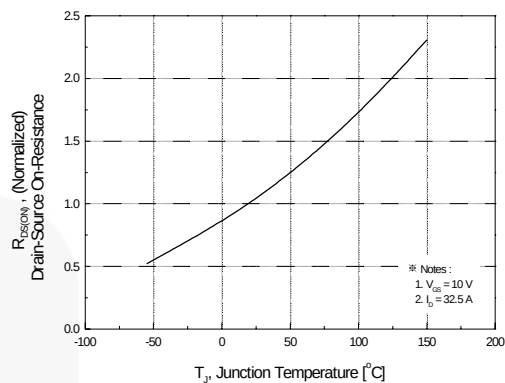


Figure 8. On-Resistance Variation vs. Temperature

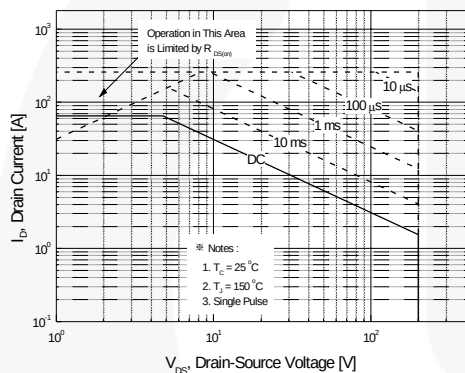


Figure 9. Maximum Safe Operating Area

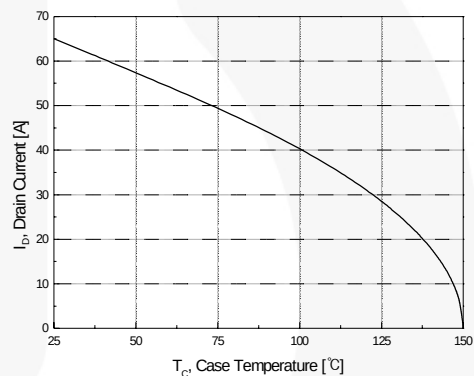


Figure 10. Maximum Drain Current vs. Case Temperature

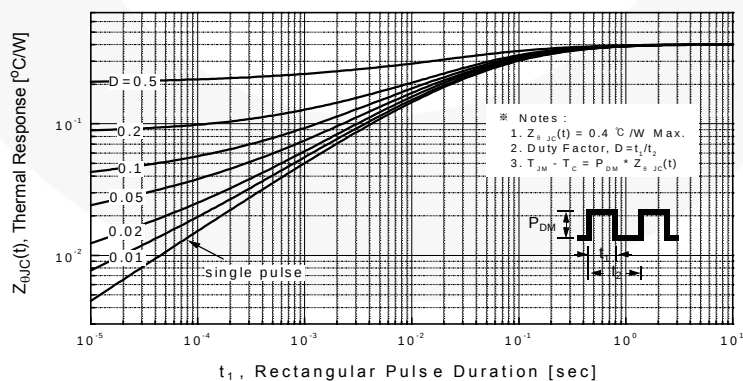


Figure 11. Transient Thermal Response Curve

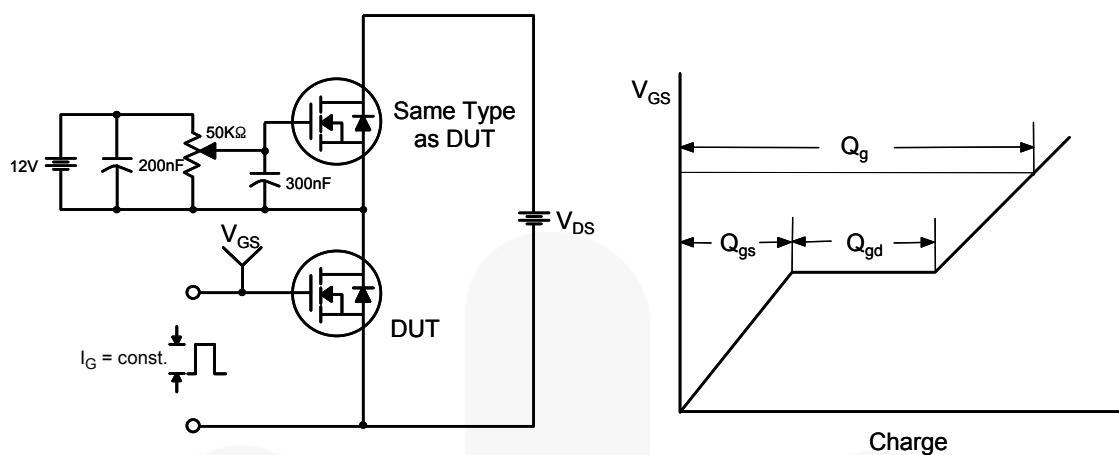


Figure 12. Gate Charge Test Circuit & Waveform

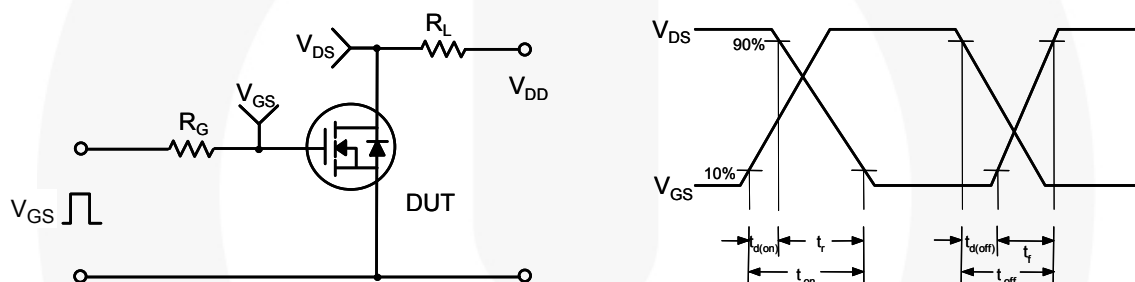


Figure 13. Resistive Switching Test Circuit & Waveforms

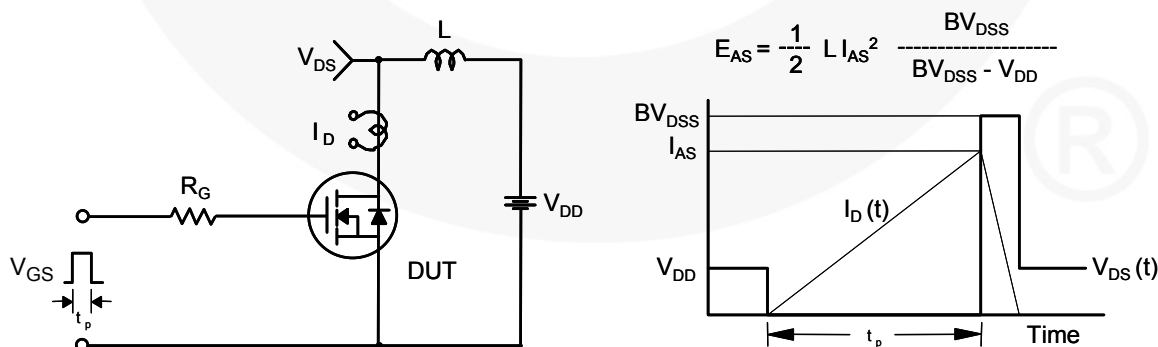


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

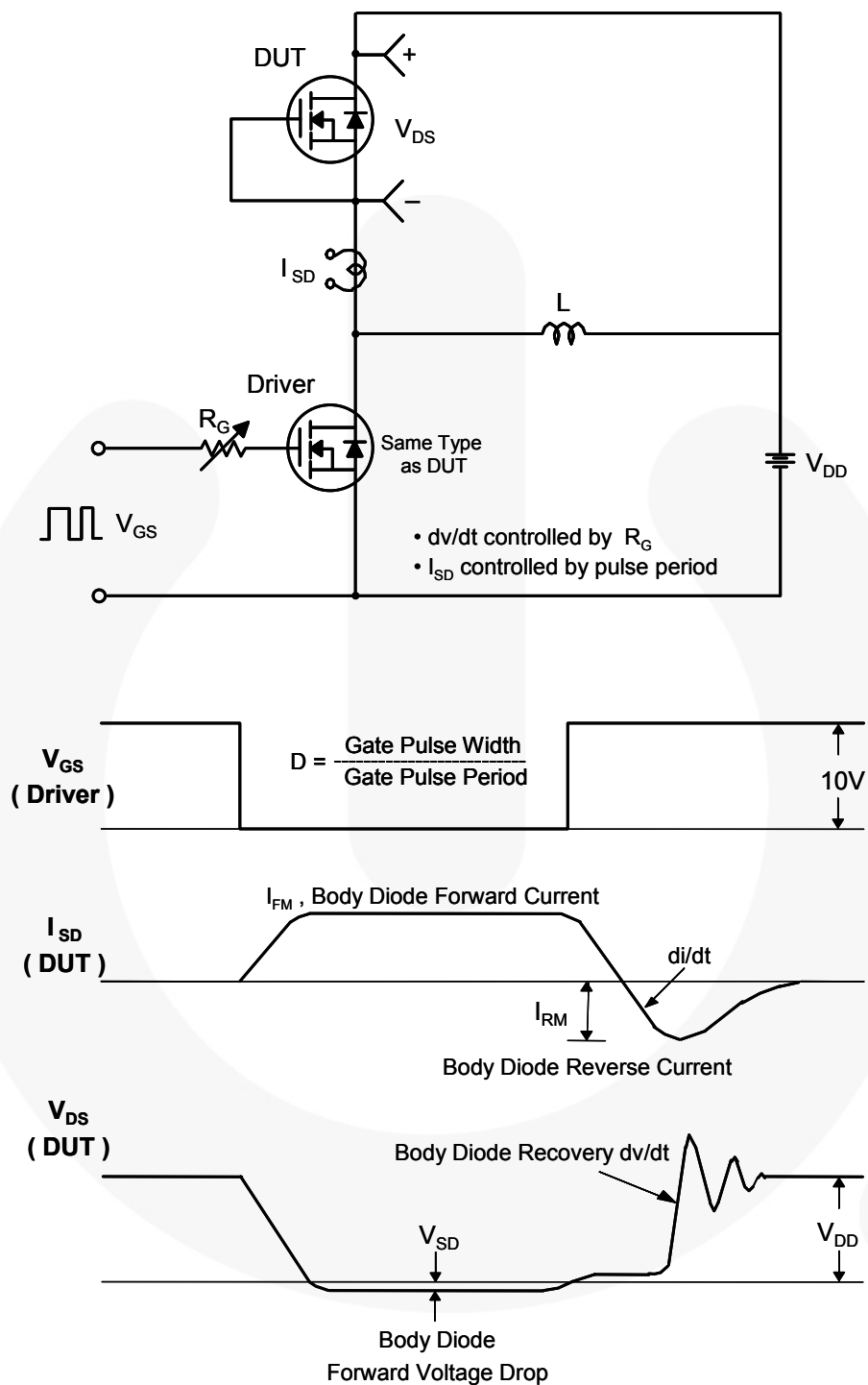
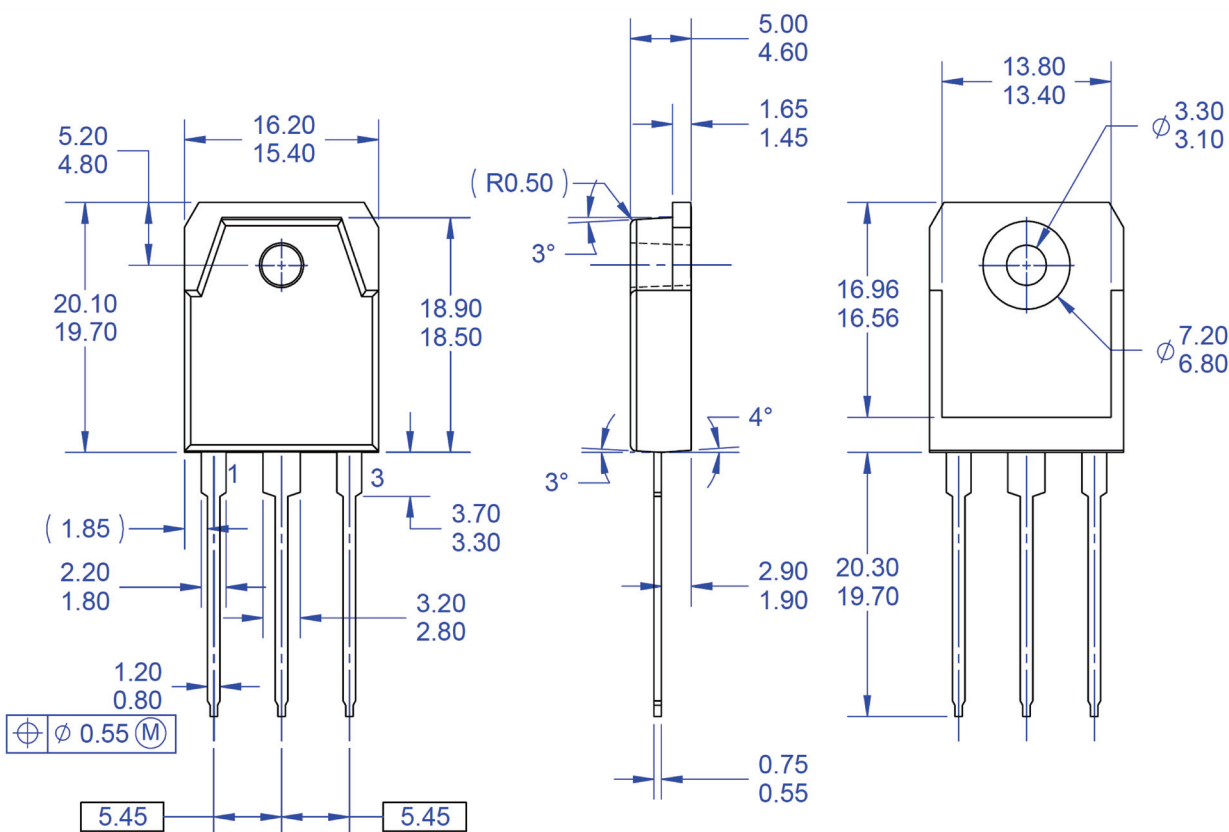


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
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- E) DRAWING FILE NAME: TO3PN03AREV1.
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Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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