

# MOSFET – N-Channel QFET

250 V, 40 A, 70 mΩ

## FQA40N25

### Description

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

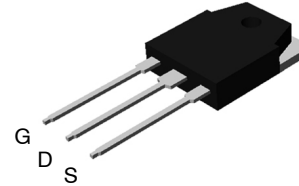
- 40 A, 250 V,  $R_{DS(on)} = 70 \text{ m}\Omega$  (Max) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 20 \text{ A}$
- Low Gate Charge (Typ. 85 nC)
- Low  $C_{rss}$  (Typ. 70 pF)
- 100% Avalanche Tested
- This is a Pb-Free Device

### ABSOLUTE MAXIMUM RATINGS

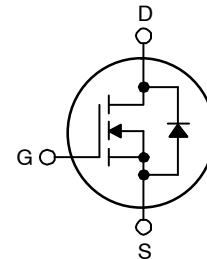
( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	250	V
$I_D$	Drain Current Continuous ( $T_C = 25^\circ\text{C}$ ) Continuous ( $T_C = 100^\circ\text{C}$ )	40 25	A
$I_{DM}$	Drain Current – Pulsed (Note 1)	160	A
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	800	mJ
$I_{AR}$	Avalanche Current (Note 1)	40	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	28	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) – Derate above $25^\circ\text{C}$	280 2.22	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

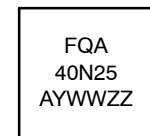
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



TO-3P-3LD / EIAJ SC-65, ISOLATED CASE 340BZ



### MARKING DIAGRAM



FQA40N25 = Specific Device Code  
A = Assembly Location  
YWW = Date Code (Year & Week)  
ZZ = Assembly Lot

### ORDERING INFORMATION

Device	Package	Shipping
FQA40N25	TO-3P (Pb-Free)	450 Unit / Tube

# FQA40N25

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max	0.45	°C/W
$R_{\theta CS}$	Thermal Resistance, Junction-to-Sink, Typ	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max	40	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTIC

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	250	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.24	-	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 200\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	0.051	0.07	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 20\text{ A}$	-	29	-	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	3100	4000	pF
$C_{oss}$	Output Capacitance		-	620	800	
$C_{rss}$	Reverse Transfer Capacitance		-	70	90	

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125\text{ V}, I_D = 40\text{ A}, R_G = 25\ \Omega$	-	70	150	ns	
$t_r$	Turn-On Rise Time		(Note 4)	-	580		1150
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	-	120		250
$t_f$	Turn-Off Fall Time		(Note 4)	-	165		340
$Q_g$	Total Gate Charge	$V_{DS} = 200\text{ V}, I_D = 40\text{ A}, V_{GS} = 10\text{ V}$	-	85	110	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4)	-	25		-
$Q_{gd}$	Gate-Drain Charge		(Note 4)	-	46		-

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	-	-	40	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	-	-	160	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 40\text{ A}$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 40\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	220	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	2.0	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $L = 0.8\text{ mH}, I_{AS} = 40\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 40\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

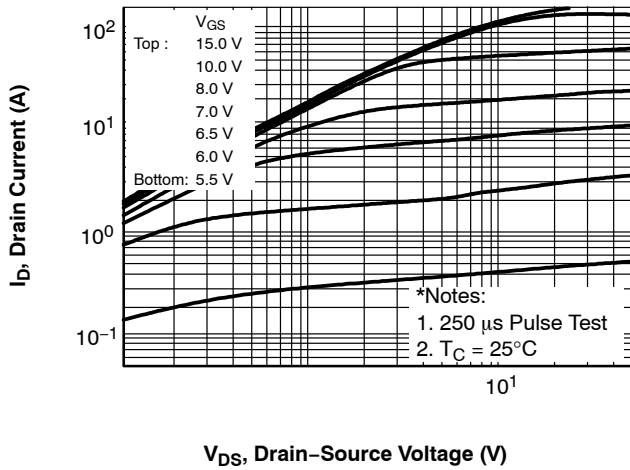


Figure 1. On-Region Characteristics

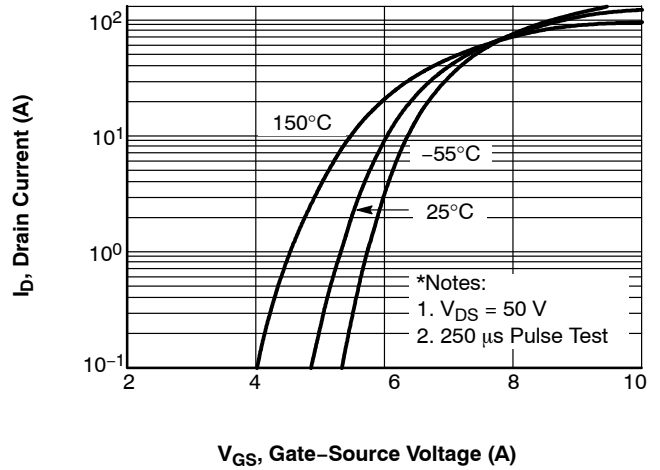


Figure 2. Transfer Characteristics

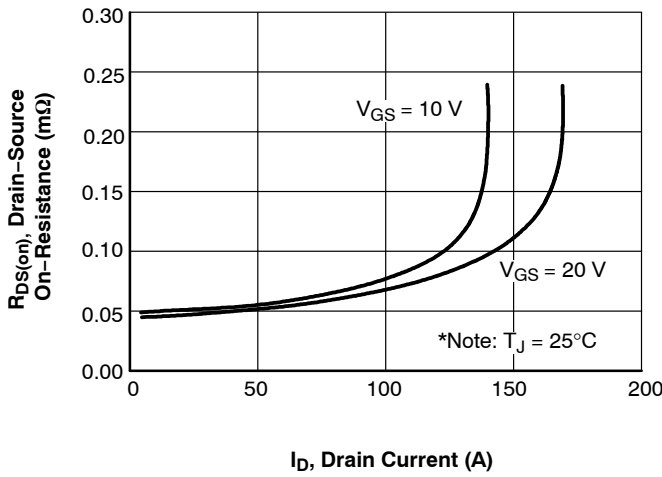


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

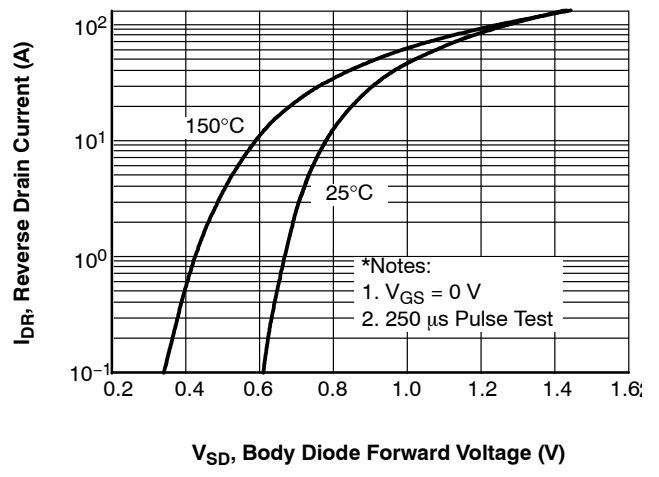


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

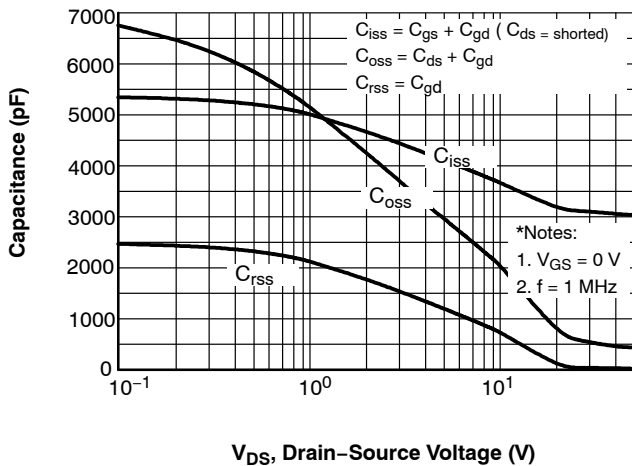


Figure 5. Capacitance Characteristics

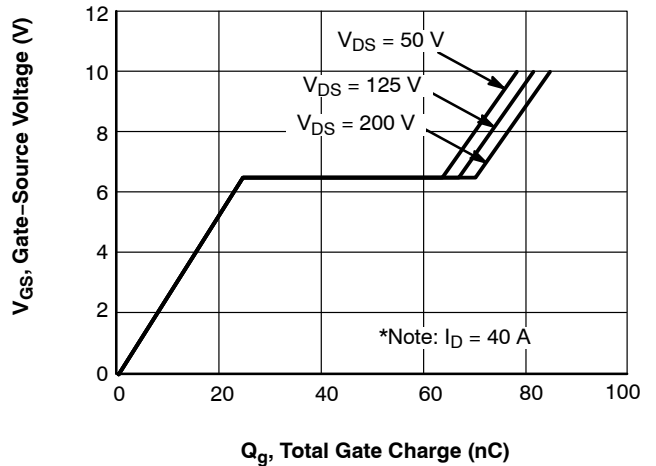
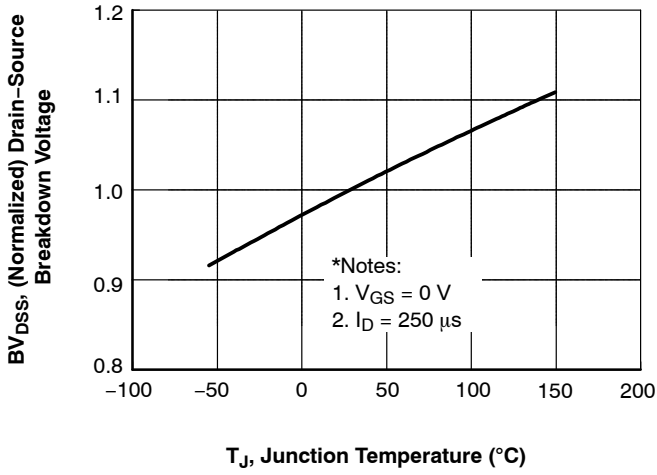


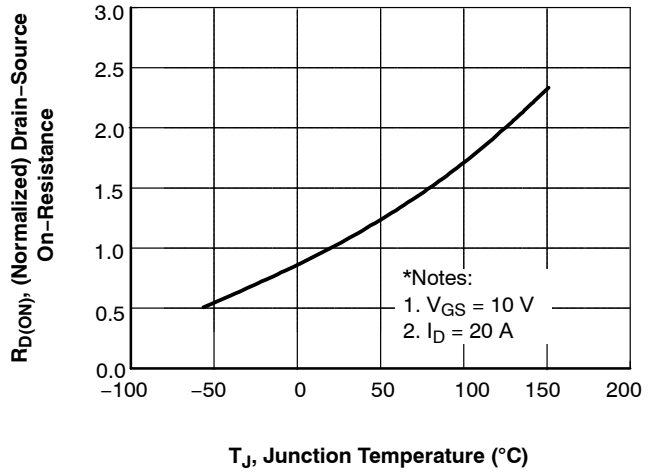
Figure 6. Gate Charge Characteristics

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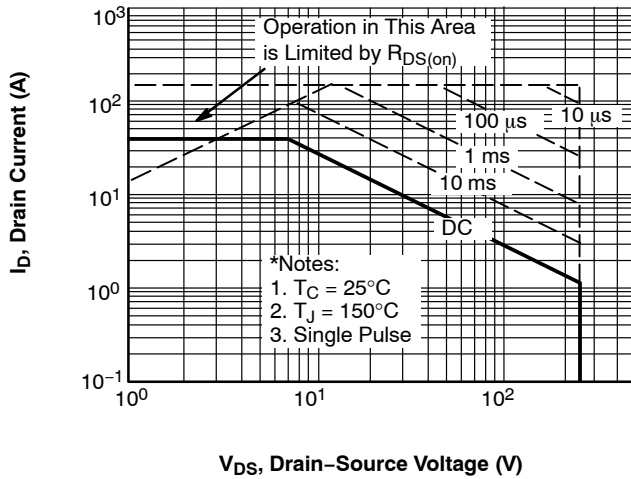
## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)



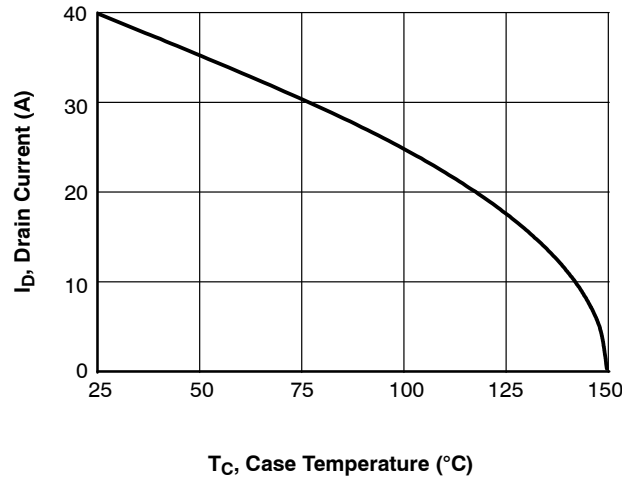
**Figure 7. Breakdown Voltage Variation vs. Temperature**



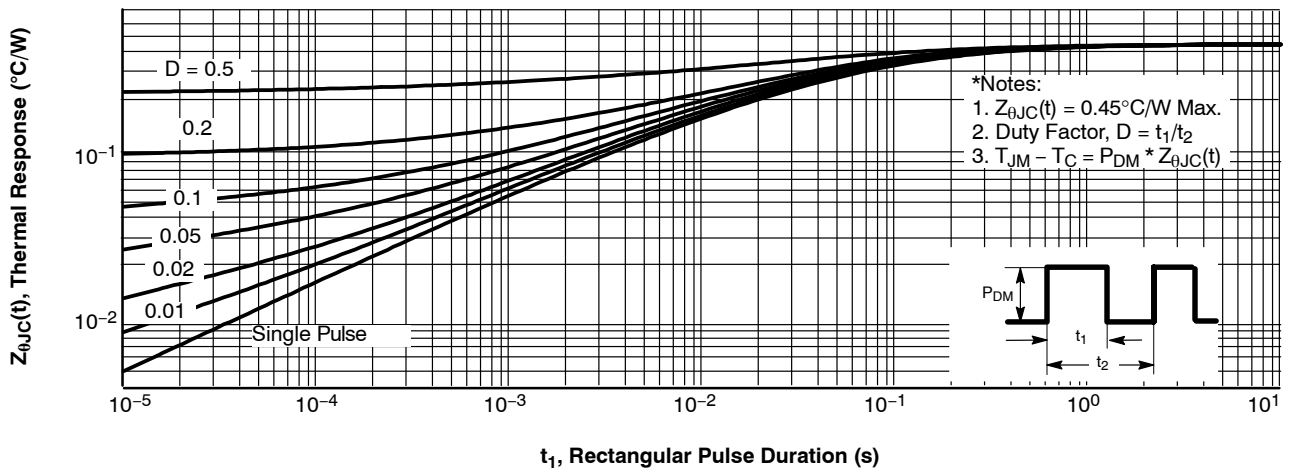
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

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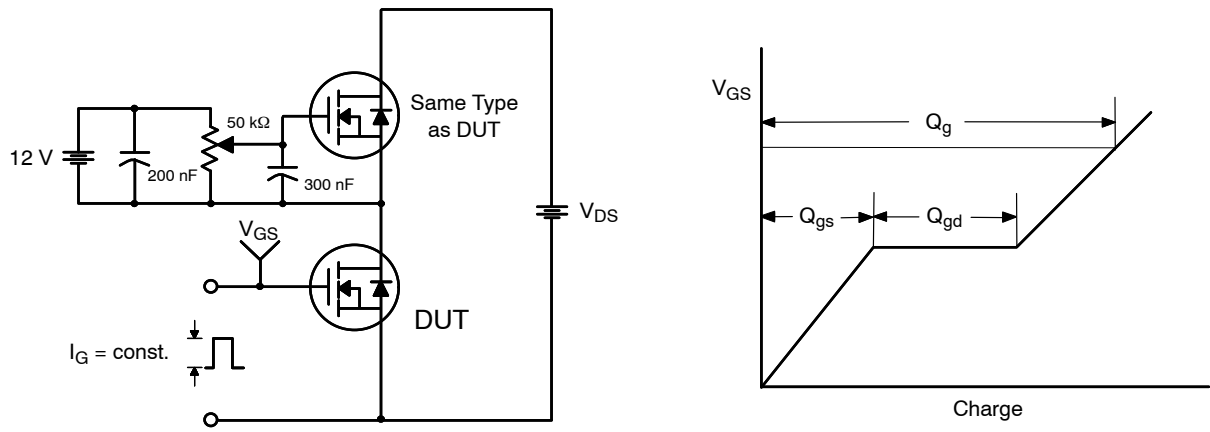


Figure 12. Gate Charge Test Circuit & Waveform

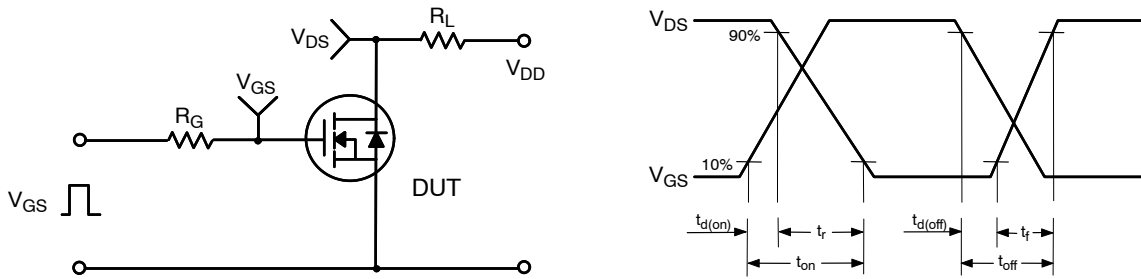


Figure 13. Resistive Switching Test Circuit & Waveforms

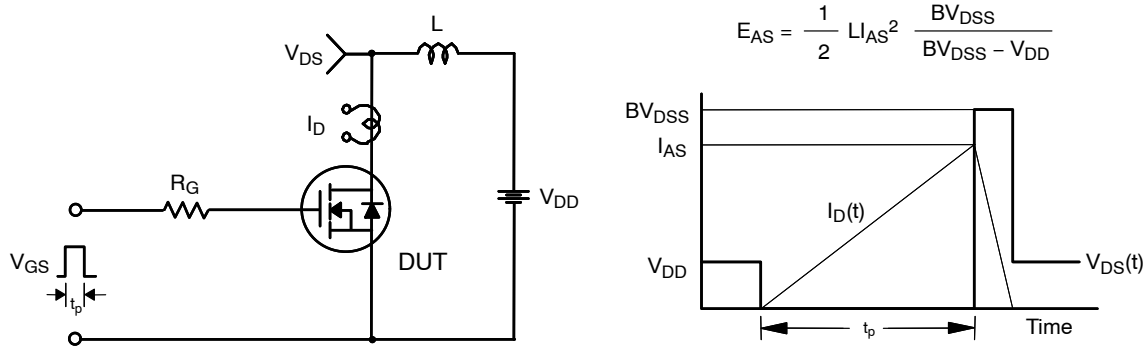


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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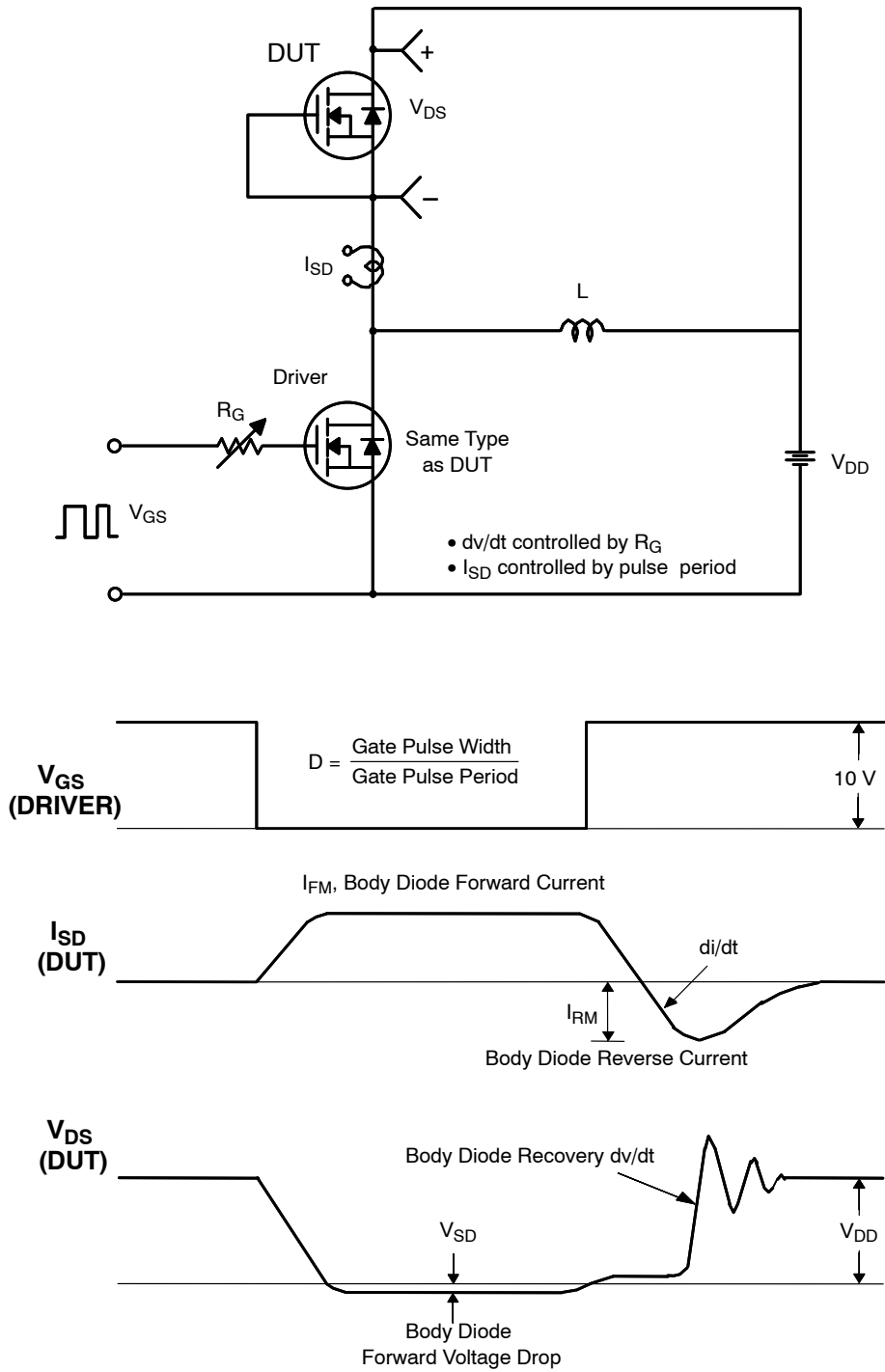


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

# MECHANICAL CASE OUTLINE

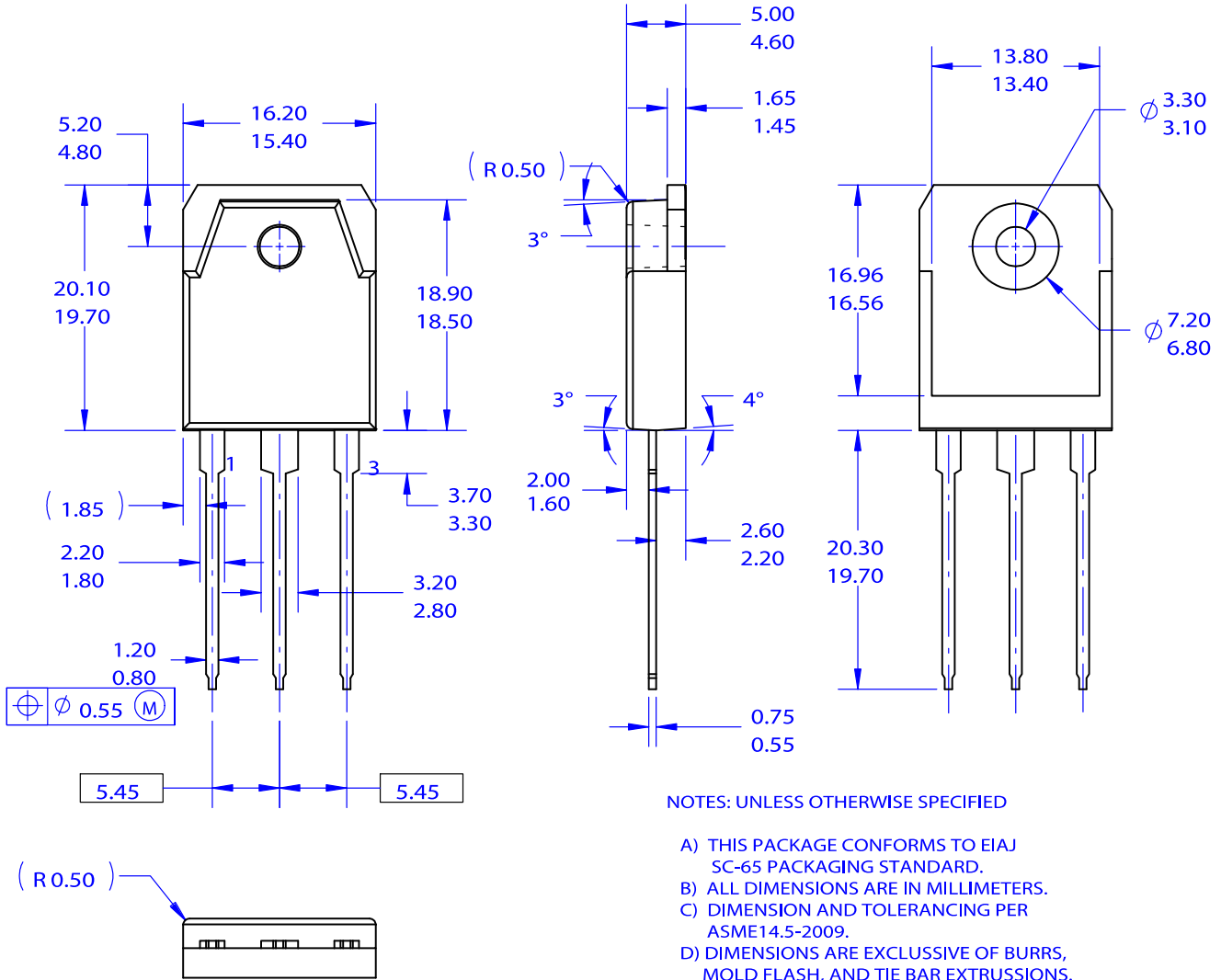
## PACKAGE DIMENSIONS

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### TO-3P-3LD / EIAJ SC-65, ISOLATED CASE 340BZ ISSUE O

DATE 31 OCT 2016



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