

FPF2260ATMX

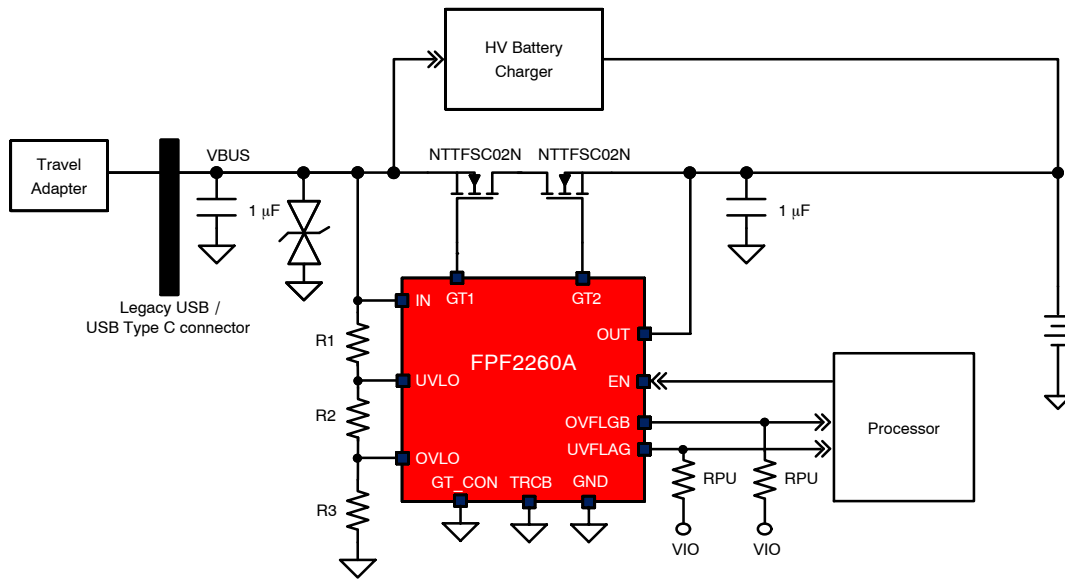


Figure 1. Schematic – Adjustable Option

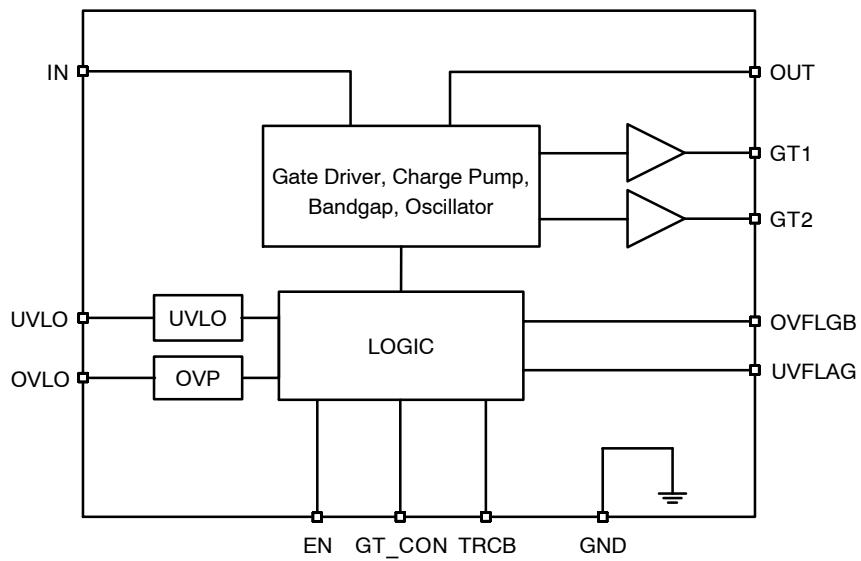


Figure 2. Simplified Block Diagram

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PIN FUNCTION DESCRIPTION

Pin No.	Name	Description
1	GND	Ground
2	OVLO	OVLO Input: Over Voltage Lockout Adjustment Input
3	IN	Power Input: External FET Input and Device Supply
4	GT1	Gate 1 Output:
5	GT2	Gate 2 Output:
6	OUT	Power Output: External FET Output and Device Supply(More Description)
7	UVFLAG	UVLO Flag Output: Open-drain output, turn ON the internal MOS to pull down this pin to indicate no Under-Voltage condition on IN
8	OVFLGB	OVP Flag Output: Open-drain output, turn ON the internal MOS to pull down this pin to indicate Over-Voltage condition on IN
9	EN	Enable Input: Active HIGH with internal 500 kΩ pull down resistor
10	GT_CON	Gate Voltage Control Input: VGS select Pin 0: Vgs = 12 V; 1/floating: Vgs = 6V with internal 500 kΩ pull up resistor
11	UVLO	UVLO Input: Under Voltage Lockout Adjustment Input
12	TRCB	True RCB Enable Input: 0: no TRCB; 1/floating: Block Reverse Current Entirely with internal 500 kΩ pull up resistor

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{IN}	Input Voltage Range (Note 1)	-28 to +28	V
V _{OUT}	Output Voltage Range	-0.3 to +28	V
V _{I/O}	Standard I/O Range (UVFLAG, OVFLGB, TRCB, GT_CON)	-0.3 to +6	V
V _{HVIO}	HV I/O Range (OVLO, UVLO, EN)	-0.3 to +28	V
T _{J(max)}	Maximum Junction Temperature	150	°C
TSTG	Storage Temperature Range	-65 to 150	°C
ESDHBM	ESD Capability, Human Body Model (Note 2)	±2	kV
ESDCDM	ESD Capability, Charged Device Model (Note 2)	±1	kV
T _{SLD}	Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
ESD Charged Device Model tested per AEC-Q100-011 (EIA/JESD22-C101)
Latch-up Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
R _{θJA}	Thermal Characteristics, X2QFN12 (Note 4) Thermal Resistance, Junction-to-Air (Note 5)	139.3	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. Values based on 2S2P JEDEC std. PCB.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{in}	Supply Voltage on VIN (GT_CON floating)	4.0	22	V
	Supply Voltage on VIN (GT_CON grounded)		16	
V_{OVLO} , $UVLO$, EN , $TRCB$, GT_CON , $OVFLAG$, $UVFLAG$	I/O pins	0	5.5	V
C_{in}	IN Capacitor	1	–	μF
C_{out}	OUT Capacitor	1	–	μF
T_A	Ambient Temperature	–40	85	$^{\circ}C$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V_{IN} = 2.9$ to 23 V, $C_{IN} = 0.1$ μF , $C_{OUT} = 0.1$ μF , $T_A = -40$ to $85^{\circ}C$; For typical values $V_{IN} = 5.0$ V, $I_{IN} \leq 3$ A, $C_{IN} = 0.1$ μF , $T_A = 25^{\circ}C$, for min/max values $T_A = -40^{\circ}C$ to $85^{\circ}C$; unless otherwise noted. (Note 6)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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LEAKAGE AND QUIESCENT CURRENTS

I_Q	Input Quiescent Current on VIN	$V_{IN} = 5$ V, $V_{OVLO} = 1$ V, $TRCB = 0$, V_{OUT} floating	–	160	–	μA
		$V_{IN} = 20$ V, $V_{OVLO} = 1$ V, $TRCB = 0$, V_{OUT} floating	–	400	–	
I_{OFF}	Device turned off current	$V_{IN} = 5$ V, $V_{EN} = 0$ V, $V_{OUT} = 0$ V	–	120	–	μA
I_{IN_Q}	Supply Current during Over Voltage	$V_{IN} = 20$ V, $V_{OVLO} = 1.8$ V, $V_{OUT} = 0$ V	–	180	–	μA
I_{OVLO}	OVLO Input Leakage Current	$V_{OVLO} = V_{OVLO_TH}$	–100	–	100	nA

OVER VOLTAGE AND UNDER VOLTAGE LOCKOUT

V_{DEF_OVLO}	Default Over-Voltage Trip Level	V_{IN} rising, $T_A = -40$ to $85^{\circ}C$	5.9	6.1	6.3	V
V_{DEF_UVLO}	Default Under-Voltage Trip Level	V_{IN} falling, $T_A = -40$ to $85^{\circ}C$	1.8	2.0	2.2	V
V_{OVLO_TH}	OVLO set threshold	V_{OVLO} rising from 1.1 V to 1.3 V, the OVLO voltage to switch off power FET	1.15	1.19	1.23	V
V_{HYS_OVLO}	OVLO threshold hysteresis		–	2	–	%
V_{UVLO_TH}	UVLO set threshold	V_{UVLO} falling from 1.3 V to 1.1 V, the UVLO voltage to switch off power FET	1.15	1.17	1.23	V
V_{HYS_UVLO}	UVLO threshold hysteresis		–	2	–	%
V_{OV_RNG}	Adjustable OVLO range	$V_{OVLO} > 0.5$ V	4	–	22	V

TRCB (IN TRCB MODE ONLY, I.E. VTRCB = HIGH/FLOAT)

V_{DROP}	TRCB trigger level	$V_{IN} = 5$ V, $I_{LOAD} = 100$ mA	–	35	–	mV
t_{REL}	TRCB release time	$V_{IN} = 5$ V	–	1	–	ms

I/O THRESHOLDS

V_{IH_OVLO} V_{IL_OVLO}	OVLO Input Threshold Voltage	High Low	0.3 –	– –	0.15	V V
	Voltage Increasing, Logic High Voltage Decreasing, Logic Low					

GATE DRIVER

V_{GS}	Turn on status gate positive voltage over OUT (Note 8)	$V_{IN} = V_{OUT} = 5$ V, $V_{GT_CON} = 0$ V	–	12	–	V
		$V_{IN} = V_{OUT} = 5$ V, $V_{GT_CON} = 1.8$ V	–	6	–	
I_{GS}	Turn on status gate positive current	$V_{TRCB} = 0$ V, $V_{IN} = V_{OUT} = 5$ V, $V_{GT_CON} = 1.8$ V, $I_{LOAD} = 10$ mA	–	–	10	μA
	OVP turn off gate current (Note 9)	$V_{IN} = 5$ V, $V_{GT_CON} = 1.8$ V, V_{OVLO} from 1.1 V to 1.3 V	–	–	3	A

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ELECTRICAL CHARACTERISTICS ($V_{IN} = 2.9$ to 23 V, $C_{IN} = 0.1$ μ F, $C_{OUT} = 0.1$ μ F, $T_A = -40$ to 85° C; For typical values $V_{IN} = 5.0$ V, $I_{IN} \leq 3$ A, $C_{IN} = 0.1$ μ F, $T_A = 25^\circ$ C, for min/max values $T_A = -40^\circ$ C to 85° C; unless otherwise noted. (Note 6) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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I/O AND LOGIC CONTROL

V_{IH}	I/O Logic High Voltage	Pins: EN, TRCB, GT_CON	1.2	–	–	V
V_{IL}	I/O Logic Low Voltage		–	–	0.5	V
V_{OL}	Output Low Voltage of Open-Drain pins	$V_{I/O} = 3.3$ V, $I_{SINK} = 1$ mA, Pins: UVFLAG, OVFLGB	–	–	0.4	V
I_{LKG}	Leakage Current of I/O pins	$V_{I/O} = 3.3$ V, Logic de-asserted, Pins: UVFLAG, OVFLGB, GT_CON	–0.5	–	0.5	μ A

TIMING

t_{SW_DEB}	De-bounce Time of Power FET turned on	Time from 2.5 V $< V_{IN} < V_{IN_OVLO}$ to $V_{OUT} = 0.1 \times V_{IN}$	–	15	–	ms
t_{OTG_DEB}	De-bounce Time of OTG turned on	Time from $V_{OUT} > 2.8$ V to $V_{IN} = 0.1 \times V_{OUT}$	–	15	–	ms
t_{UV_DEB}	De-bounce Time of UVFLAG flag	Time from $V_{IN} > V_{IN_UVLO}$ to UVFLAG < 0.4 V	–	130	–	μ s
t_{OV_DEB}	De-bounce Time of OVFLGB flag	Time from $V_{IN} < V_{IN_OVLO}$ to OVFLGB > 1.8 V	–	1	–	ms
t_R	Switch Turn-On rising Time (Note 9)	$V_{IN} = 5$ V, $R_L = 100$ Ω , $C_L = 22$ μ F, V_{OUT} from $0.1 \times V_{IN}$ to $0.9 \times V_{IN}$	–	2	–	ms
t_{OFF}	Switch Turn-Off Time (Note 8, 9)	$R_L = 10$ Ω , $C_L = 0$ μ F, time from $V_{IN} > V_{OVLO}$ to $V_{OUT} = 0.9 \times V_{IN}$ Internal OVP level External OVP level (Note 10)	– –	50 100	– –	ns ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25^\circ$ C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

7. Refer to the APPLICATION INFORMATION section.

8. Based on the recommended MOSFET devices.

9. Values based on design and/or characterization

10. Depends on the capacitance on OVLO pin.

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TYPICAL CHARACTERISTICS

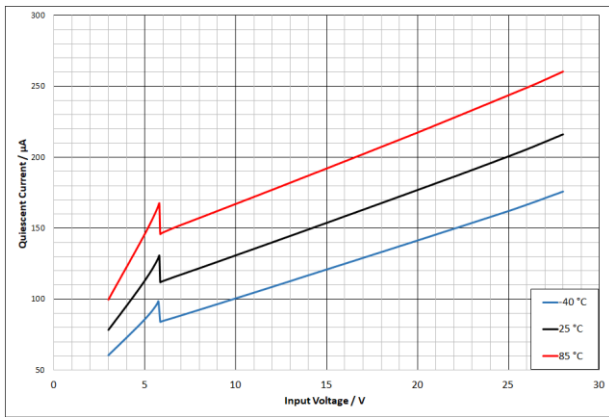


Figure 3. Quiescent Current over Temperature

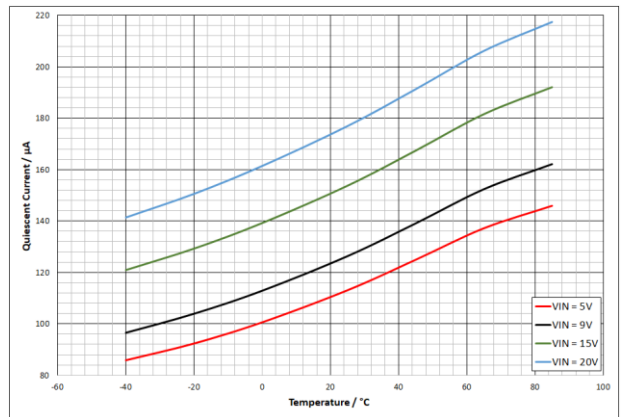


Figure 4. Quiescent Current over V_{IN}

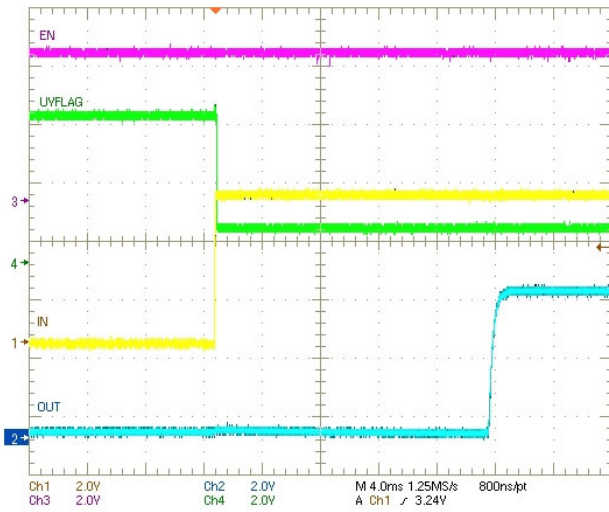


Figure 5. Power-Up Transient
($V_{IN} = 5\text{ V}$, $C_{OUT} = 0.1\ \mu\text{F}$)

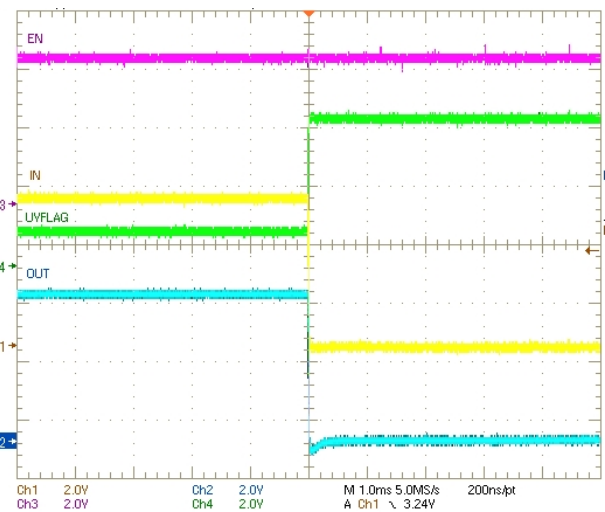


Figure 6. Power-Down Transient
($V_{IN} = 5\text{ V}$, $C_{OUT} = 0.1\ \mu\text{F}$)

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FUNCTION DESCRIPTION

General

FPF2260A is an OVP controller to drive external N-type MOSFETs. The device can protect next stage system which is optimized to lower voltage working condition, especially with ultra-high charging current. The device includes multi-functions including OVP, Advanced TRCB, and Negative Stress protection.

Power MOSFET Driver

The FPF2260A integrates charge pump driver to control external N-type MOSFET pair. The drive voltage can be configured by GPIO for different MOSFET.

The drive voltage for MOSFET can be configured by GPIO pin GT_CON. V_{GS} could be set to 6 V by pull GT_CON to high or floating. Or, V_{GS} will be set to 12 V by pulling GT_CON to ground.

True Reverse Current Blocking and USB OTG

The FPF2260A support advanced TRCB mode by pulling TRCB pin to high or floating it. In the advanced TRCB mode, no reverse current will be seen from OUT to IN through the external MOSFETs if $V_{OUT} - V_{IN} > 30$ mV.

When advanced TRCB mode is active, OTG operation is not supported. If OTG is needed, TRCB pin needs to be pulled down to ground.

Enable Control

The GPIO EN is an active high control pin. When the voltage is pulled low, FPF2260A will disable the external MOSFETs by connecting GT1 to IN and GT2 to OUT.

When EN is logic high, FPF2260A will close external MOSFET if there are no over stressed condition.

Under Voltage Lockout

FPF2260A will turn the FETs off when the voltage on IN is lower than the UVLO threshold V_{IN_UVLO} .

Whenever IN voltage ramps up to higher than the threshold, the power FET will be turned on automatically after t_{DEB} de-bounce time if there is no other over stressed condition.

The external resistor ladder can be decided according to the following equation:

$$V_{IN_UVLO} = V_{UVLO_TH} \times [1 + R1 / (R2 + R3)] \quad (\text{eq. 1})$$

where R1, R2 and R3 are the resistors in figure 1.

Over Voltage Lockout

The power FET will be turned off whenever IN voltage higher than V_{IN_OVLO} . The value of V_{IN_OVLO} can be set by external resistor ladder or just be default value V_{IN_OVLO} .

When $V_{OVLO} \leq 0.3$ V, V_{OVLO} is decided by default value. When $V_{OVLO} > 0.3$ V, the power switch will be turned off once $V_{OVLO} > V_{OVLO_TH}$. The external resistor ladder can be decided according to the following equation:

$$V_{IN_OVLO} = V_{OVLO_TH} \times [1 + (R1 + R2) / R3] \quad (\text{eq. 2})$$

where R1, R2 and R3 are the resistors in figure 1.

Negative Voltage Protection

FPF2260 support negative voltage protection to help system avoid unexpected negative stress. The gate of first external power FET, GT1, will be pulled down with the voltage on IN when it is negative. This behavior can keep the external FET at off status till -28 V.

APPLICATIONS INFORMATION

Input Decoupling (C_{in})

A ceramic or tantalum at least 0.1 μ F capacitor is recommended and should be put before and close the connection point of MOSFET and FPF2260A IN. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (C_{out})

The FPF2260A is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling value is 0.1 μ F and can be augmented to fulfill stringent load transient requirements.

Hints for PCB Layout

The external MOSFET is an important part to FPF2260A. The connection of gate should be as short as possible to avoid parasitic resistance and inductance for better OVP performance.

ORDERING INFORMATION

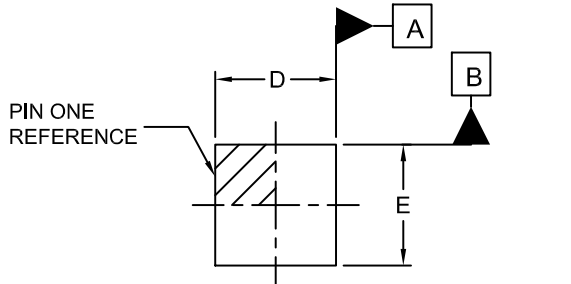
Part Number	Marking	Package	Shipping [†]
FPF2260ATMX	6B	X2QFN12	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

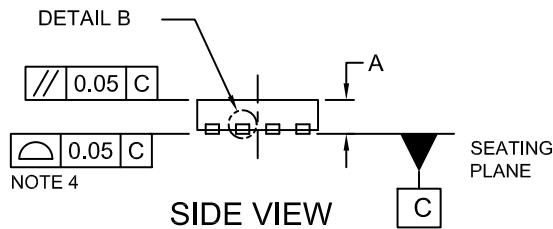


X2QFN12 1.6x1.6, 0.4P
CASE 722AG
ISSUE A

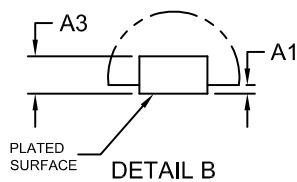
DATE 26 SEP 2017



TOP VIEW



SIDE VIEW

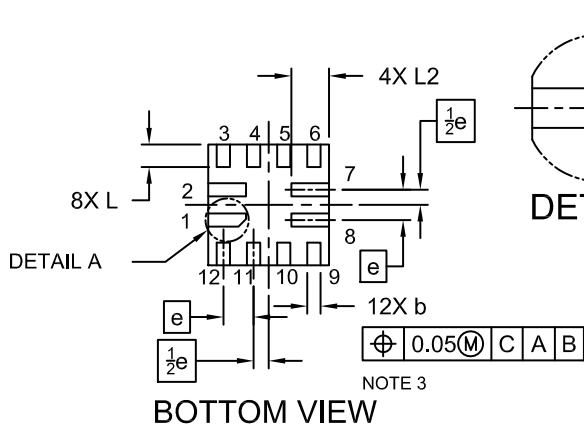


DETAIL B

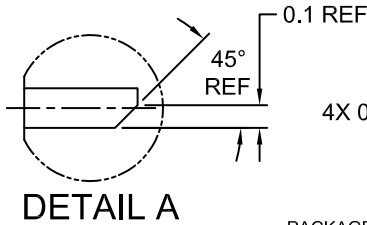
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM THE TERMINAL TIP.
4. PROFILE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

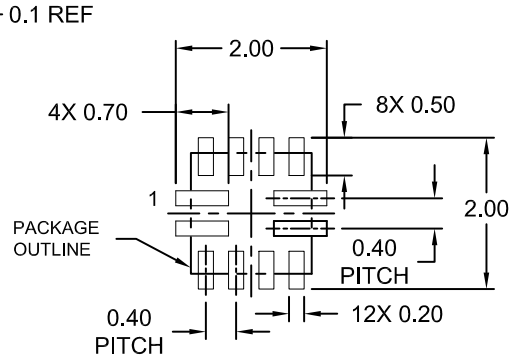
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	--	--	0.05
A3	0.127 REF		
b	0.15	0.175	0.20
D	1.55	1.60	1.65
E	1.55	1.60	1.65
e	0.40 BSC		
L	0.25	0.30	0.35
L2	0.45	0.50	0.55



BOTTOM VIEW



DETAIL A



RECOMMENDED MOUNTING FOOTPRINT

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DESCRIPTION:	X2QFN12 1.6x1.6, 0.4P	PAGE 1 OF 1

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