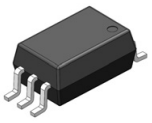
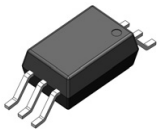
4.0 A Output Current, High Speed Gate Drive Optocoupler in Stretched Body SOP 6-Pin

FOD8343, FOD8343T



SOIC6
CASE 751EL



SOIC6 W
CASE 751EM

Description

The FOD8343 series is a 4.0 A maximum peak output current gate drive optocoupler, capable of driving medium−power IGBT / MOSFETs. It is ideally suited for fast−switching driving of power IGBT and MOSFET used in motor−control inverter applications, and high−performance power systems.

The FOD8343 series utilizes stretched body package to achieve 8 mm creepage and clearance distances (FOD8343T), and optimized IC design to achieve reliably high−insulation voltage and high−noise immunity.

The FOD8343 series consists of an Aluminum Gallium Arsenide (AlGaAs) Light−Emitting Diode (LED) optically coupled to an integrated circuit with a high−speed driver for push−pull MOSFET output stage. The device is housed in a stretched body, 6−pin, small outline, plastic package.

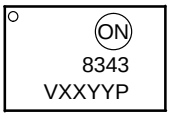
Features

- FOD8343T − 8 mm Creepage and Clearance Distance, and 0.4 mm Insulation Distance to Achieve Reliable and High−Voltage Insulation
- 4.0 A Maximum Peak Output Current Driving Capability for Medium−Power IGBT/MOSFET
  - Use of P−Channel MOSFETs at Output Stage Enables Output Voltage Swing Close to Supply Rail
- 50 kV/μs Minimum Common Mode Rejection Wide Supply Voltage Range: 10 V to 30 V
- Fast Switching Speed Over Full Operating Temperature Range
  - 210 ns Maximum Propagation Delay
  - 65 ns Maximum Pulse Width Distortion Under−Voltage Lockout (UVLO) with Hysteresis
- Extended Industrial Temperate Range: −40°C to 100°C
- Safety and Regulatory Approvals:
  - UL1577, 5,000 V_{RMS} for 1 Minute
  - DIN EN/IEC60747−5−5, 1,140 V Peak Working Insulation Voltage

Application

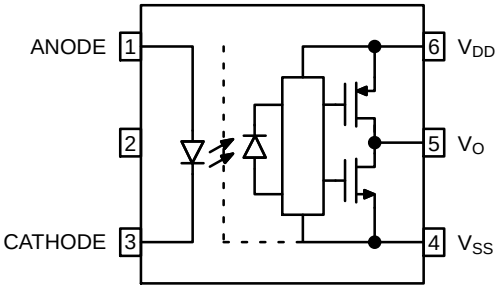
- AC and Brushless DC Motor Drives
- Industrial Inverter
- Uninterruptible Power Supply Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

MARKING DIAGRAM



8343 = Device Number
V = DIN EN/IEC60747−5−5 Option (Only Appears on Component Ordered with this Option)
XX = Two Digit Year Code, e.g. ‘15’
YY = Two Digit Work Week Ranging from ‘01’ to ‘53’
P = Assembly Package Code

FUNCTIONAL SCHEMATIC



ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

Related Resources

- FOD3182, 3 A Output Current, High Speed MOSFET Gate Drive Optocoupler
- FOD8314, FOD8314T, 1.0 A Output Current, Gate Drive Optocoupler in Stretched Body SOP 6−Pin

TRUTH TABLE

LED	V_{DD} − V_{SS} "Positive Going" (Turn−on)	V_{DD} − V_{SS} "Negative Going" (Turn−off)	V_O
Off	0 V to 30 V	0 V to 30 V	LOW
On	0 V to 7 V	0 V to 6.5 V	LOW
On	7 V to 9.5 V	6.5 V to 9 V	Transition
On	9.5 V to 30 V	9 V to 30 V	HIGH

PIN DEFINITIONS

Pin No.	Symbol	Description
1	ANODE	LED Anode
2	N.C	Not Connection
3	CATHODE	LED Cathode
4	V_{SS}	Negative Supply Voltage
5	V_O	Output Voltage
6	V_{DD}	Positive Supply Voltage

PIN CONFIGURATION

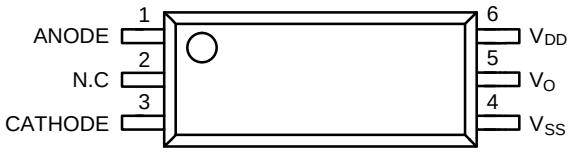


Figure 1. Pin Configuration

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC60747−5−5 , this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter		Characteristics	
		FOD8343	FOD8343T
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	<150 V_{RMS}	I−IV	I−IV
	<300 V_{RMS}	I−IV	I−IV
	<450 V_{RMS}	I−III	I−IV
	<600 V_{RMS}	I−III	I−III
Climatic Classification		40/100/21	40/100/21
Pollution Degree (DIN VDE 0110/1.89)		2	2
Comparative Tracking Index		175	175

Symbol	Parameter	Value		Unit
		FOD8343	FOD8343T	
V_{PR}	Input−to−Output Test Voltage, Method B, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	1,671	2,137	V_{peak}
	Input−to−Output Test Voltage, Method A, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	1,426	1,824	V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	891	1,140	V_{peak}
V_{IOTM}	Highest Allowable Over−Voltage	6,000	8,000	V_{peak}
	External Creepage	≥8.0	≥8.0	mm
	External Clearance	≥7.0	≥8.0	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥0.4	≥0.4	mm
	Safety Limit Values − Maximum Values Allowed in the Event of a Failure,			
T_S	Case Temperature	150	150	°C
$I_{S,INPUT}$	Input Current	200	200	mA
$P_{S,OUTPUT}$	Output Power	600	600	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9	10^9	Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +100	°C
T_J	Junction Temperature	−40 to +125	°C
T_{SOL}	Lead Solder Temperature *(Refer to Reflow Temperature Profile)*	260 for 10 s	°C
$I_{F(AVG)}$	Average Input Current	25	mA
V_R	Reverse Input Voltage	5.0	V
$I_{O(PEAK)}$	Peak Output Current (Note 1)	4	A
V_{DD}	Supply Voltage	−0.5 to 35	V
$V_{O(PEAK)}$	Peak Output Voltage	0 to V_{DD}	V
$t_{R(IN)}$, $t_{F(IN)}$	Input Signal Rise and Fall Time	250	ns
PD_I	Input Power Dissipation (Note 2) (Note 4)	45	mW
PD_O	Output Power Dissipation (Note 3) (Note 4)	500	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum pulse width = 10 μs
2. No derating required across operating temperature range.
3. Derate linearly from 25°C at a rate of 5.2 mW/°C.
4. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	−40	+100	°C
$V_{DD} - V_{SS}$	Supply Voltage	10	30	V
$I_{F(ON)}$	Input Current (ON)	10	16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	−3.0	0.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ISOLATION CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at T_A = 25°C.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ISO}	Input−Output Isolation Voltage	T_A = 25°C, R.H. < 50%, t = 1.0 minute, $I_{I-O} \le$ 20 μA (Note 5) (Note 6)	5000	–	–	VAC_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 5)	–	10^{11}	–	Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, Frequency = 1.0 MHz (Note 5)	–	1	–	pF

5. Device is considered a two terminal device: pins 1, 2 and 3 are shorted together and pins 4, 5 and 6 are shorted together.
6. 5,000 VAC_{RMS} for 1 minute duration is equivalent to 6,000 VAC_{RMS} for 1 second duration.

ELECTRICAL CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_F	Input Forward Voltage	I_F = 10 mA	1.1	1.5	1.8	V
$\Delta(V_F/T_A)$	Temperature Coefficient of Forward Voltage		–	−1.8	–	mV/°C
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA	5.0	–	–	V
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V	–	20	–	pF
I_{OH}	High Level Output Current (Note 1)	$V_{OH} = V_{DD} - 3$ V	1.0	–	–	A
		$V_{OH} = V_{DD} - 10$ V	3.0	–	–	A
I_{OL}	Low Level Output Current (Note 1)	$V_{OL} = V_{SS} + 3$ V	1.0	–	–	A
		$V_{OL} = V_{SS} + 10$ V	3.0	–	–	A
V_{OH}	High Level Output Voltage (Note 7) (Note 8)	I_F = 10 mA, I_O = −100 mA	$V_{DD} - 0.5$	$V_{DD} - 0.1$	–	V
V_{OL}	Low Level Output Voltage (Note 7) (Note 8)	I_F = 0 mA, I_O = 100 mA	–	$V_{SS} + 0.1$	$V_{SS} + 0.5$	V
I_{DDH}	High Level Supply Current	V_O = Open, I_F = 10 to 16 mA	–	2.9	4.0	mA
I_{DDL}	Low Level Supply Current	V_O = Open, V_F = −3.0 to 0.8 V	–	2.8	4.0	mA
I_{FLH}	Threshold Input Current Low to High	I_O = 0 mA, V_O > 5 V	–	2.0	7.5	mA
V_{FHL}	Threshold Input Voltage High to Low	I_O = 0 mA, V_O < 5 V	0.8	–	–	V
V_{UVLO+}	UnderVoltage Lockout Threshold	I_F = 10 mA, V_O > 5 V	7.0	8.3	9.5	V
V_{UVLO-}		I_F = 10 mA, V_O < 5 V	6.5	7.7	9.0	V
$UVLO_{HYS}$	UnderVoltage Lockout Threshold Hysteresis		–	0.6	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
7. In this test, V_{OH} is measured with a dc load current of 100 mA. When driving capacitive load V_{OH} will approach V_{DD} as I_{OH} approaches 0 A.
8. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

SWITCHING CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}	Propagation Delay Time to Logic Low Output (Note 9)	I_F =10 mA, R_g = 10 Ω, C_g = 10 nF, f = 250 kHz, Duty Cycle = 50%	50	145	210	ns
t_{PLH}	Propagation Delay Time to Logic High Output (Note 10)		50	120	210	ns
PWD	Pulse Width Distortion (Note 11) $\lvert t_{PHL} - t_{PLH} \rvert$		–	35	65	ns
PDD (Skew)	Propagation Delay Difference Between Any Two Parts (Note 12)		−90	–	90	
t_R	Output Rise Time (10% to 90%)		–	38	–	ns
t_F	Output Fall Time (90% to 10%)		–	24	–	ns
$t_{ULVO\ ON}$	ULVO Turn On Delay	I_F = 10 mA, V_O > 5 V	–	2.0	–	μs
$t_{ULVO\ OFF}$	ULVO Turn Off Delay	I_F = 10 mA, V_O < 5 V	–	0.3	–	μs
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	V_{DD} = 30 V, I_F = 10 mA to 16 mA, V_{CM} = 2000 V, T_A = 25°C (Note 13)	50	–	–	kV/μs
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	V_{DD} = 30 V, V_F = 0 V, V_{CM} = 2000 V, T_A = 25°C (Note 14)	50	–	–	kV/μs

9. Propagation delay t_{PHL} is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal.
10. Propagation delay t_{PLH} is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
11. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
12. The difference between t_{PHL} and t_{PLH} between any two FOD8343 parts under the same operating conditions, with equal loads.
13. Common mode transient immunity at output high is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, V_{CM}, to ensure that the output remains high (i.e., V_O > 15.0 V).
14. Common mode transient immunity at output low is the maximum tolerable positive dVcm/dt on the leading edge of the common pulse signal, V_{CM}, to ensure that the output remains low (i.e., V_O < 1.0 V).

TYPICAL PERFORMANCE CHARACTERISTICS

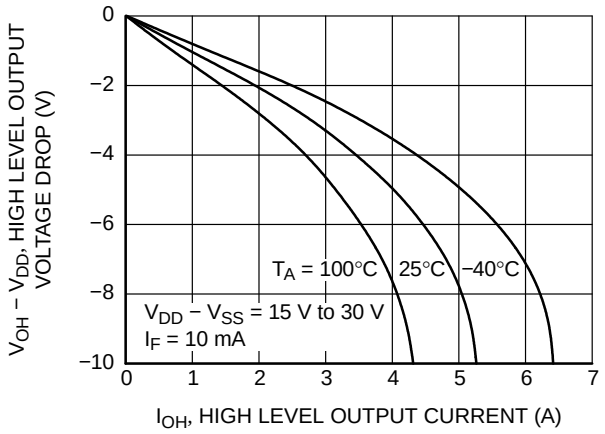


Figure 2. High Level Output Voltage Drop vs. High Level Output Current

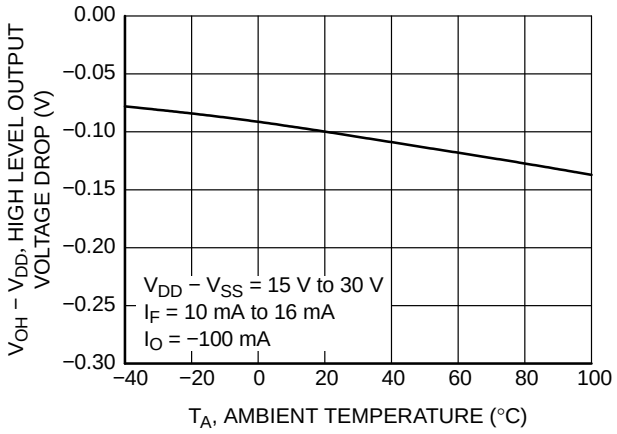


Figure 3. High Level Output Voltage Drop vs. Ambient Temperature

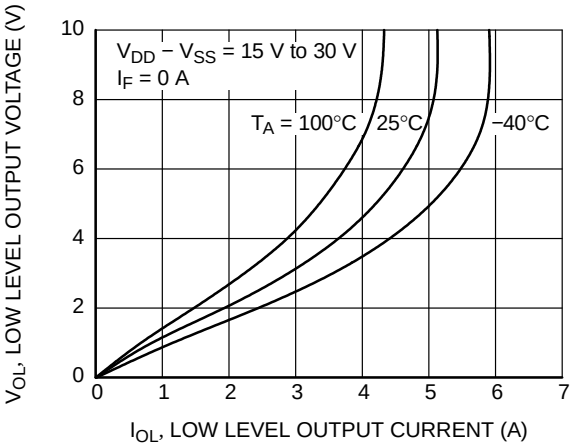


Figure 4. Low Level Output Voltage Drop vs. Low Level Output Current

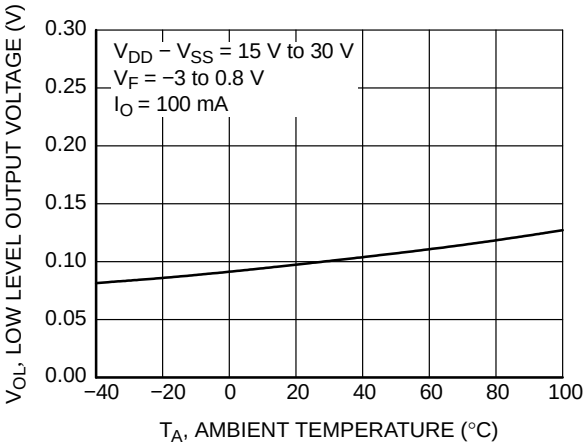


Figure 5. Low Level Output Voltage Drop vs. Ambient Temperature

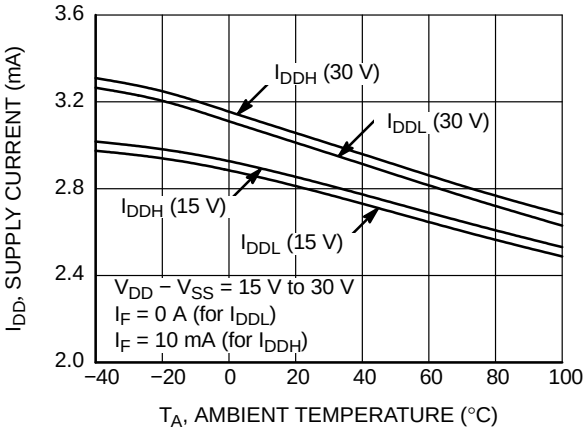


Figure 6. Supply Current vs. Ambient Temperature

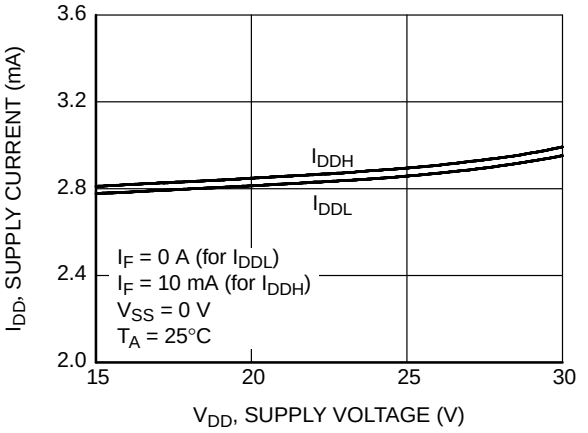


Figure 7. Supply Current vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

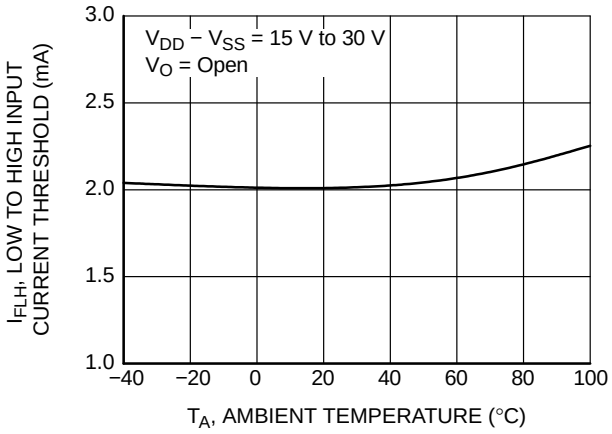


Figure 8. Low to High Input Current Threshold vs. Ambient Temperature

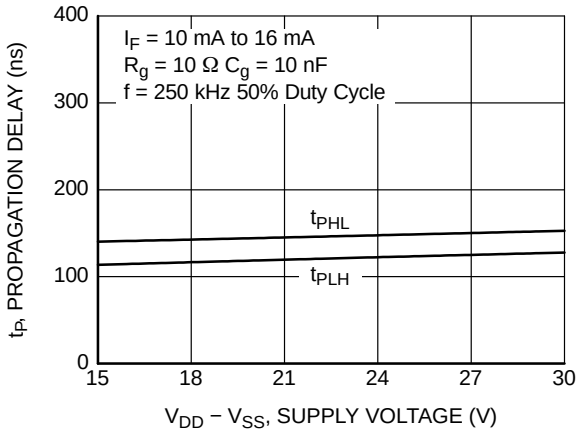


Figure 9. Propagation Delay vs. Supply Voltage

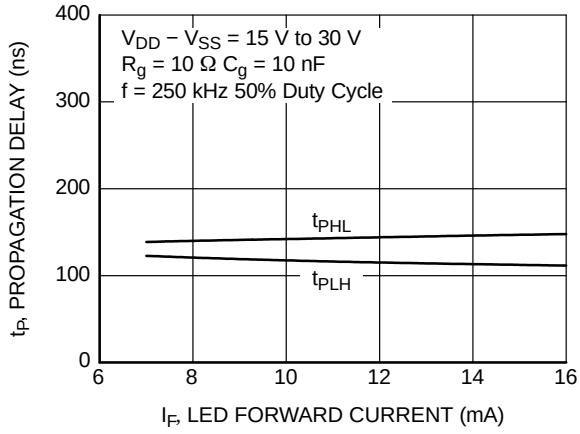


Figure 10. Propagation Delay vs. LED Forward Current

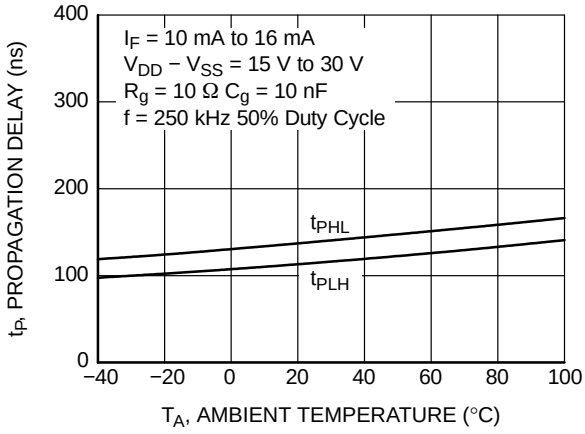


Figure 11. Propagation Delay vs. Ambient Temperature

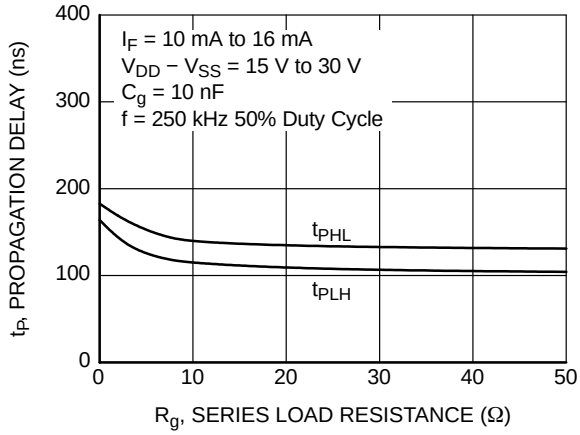


Figure 12. Propagation Delay vs. Series Load Resistance

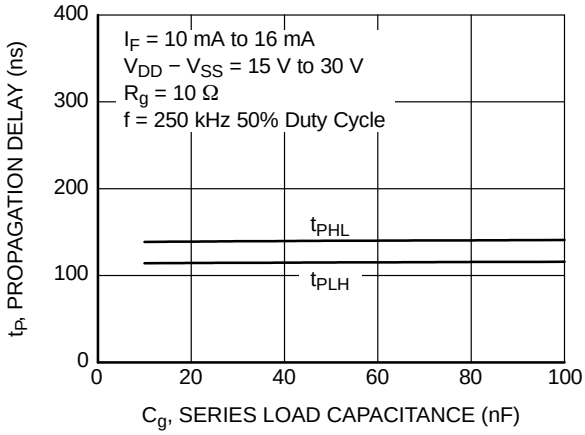


Figure 13. Propagation Delay vs. Series Load Capacitance

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

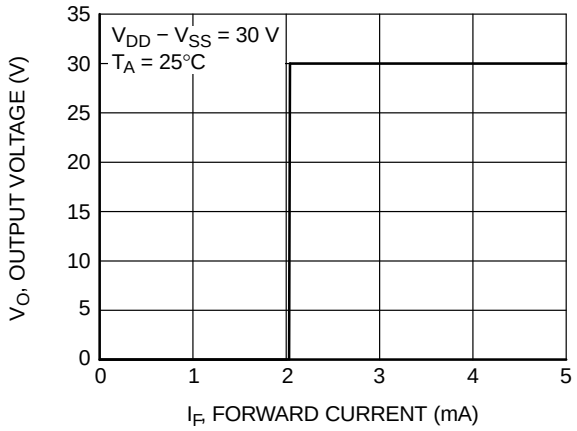


Figure 14. Transfer Characteristics

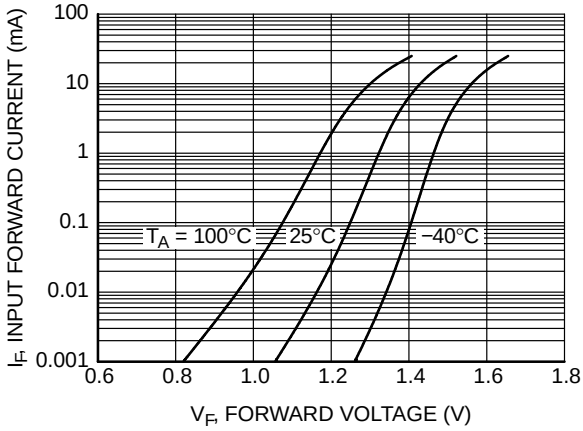


Figure 15. Input Forward Current vs. Forward Voltage

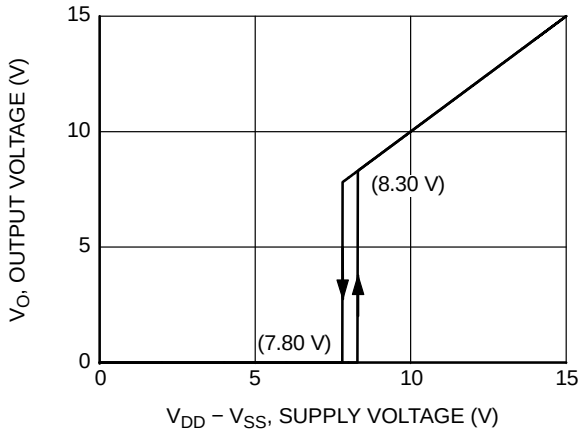


Figure 16. Under Voltage Lockout

TEST CIRCUITS

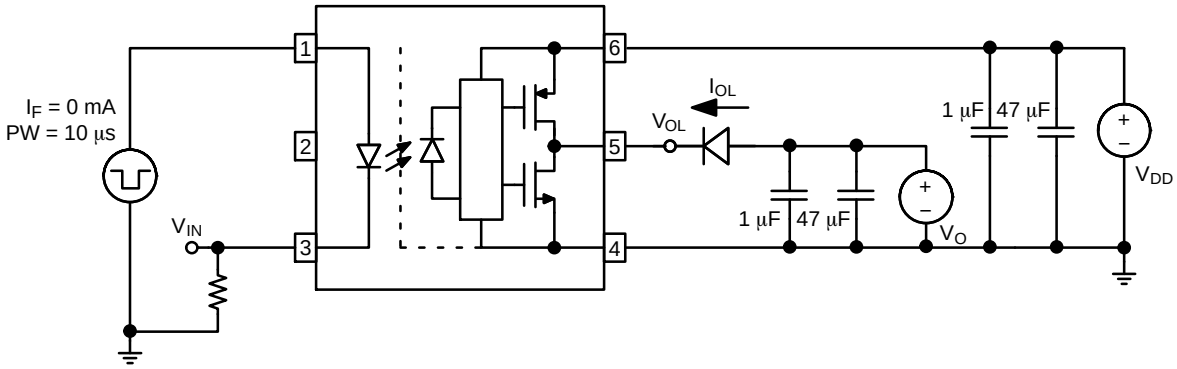


Figure 17. I_{OL} Test Circuit

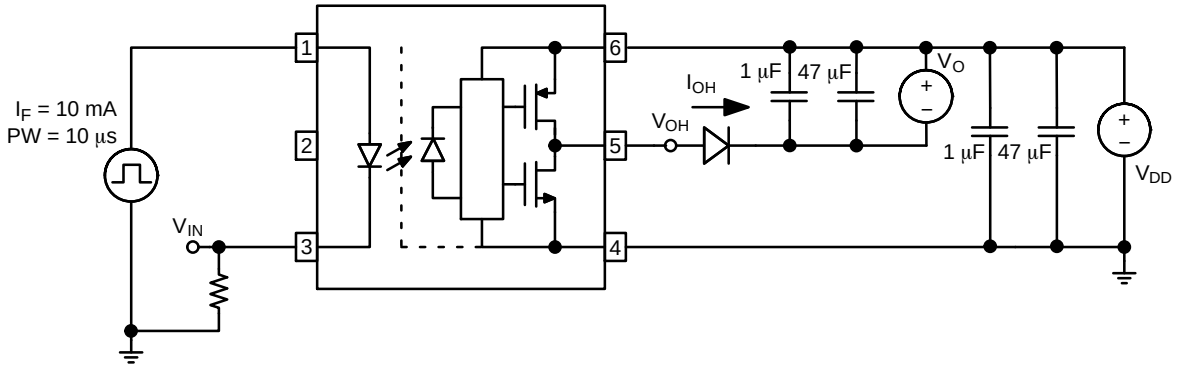


Figure 18. I_{OH} Test Circuit

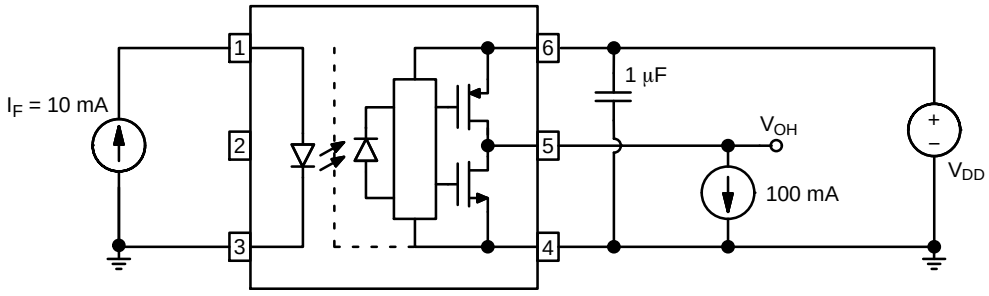


Figure 19. V_{OH} Test Circuit

TEST CIRCUITS (Continued)

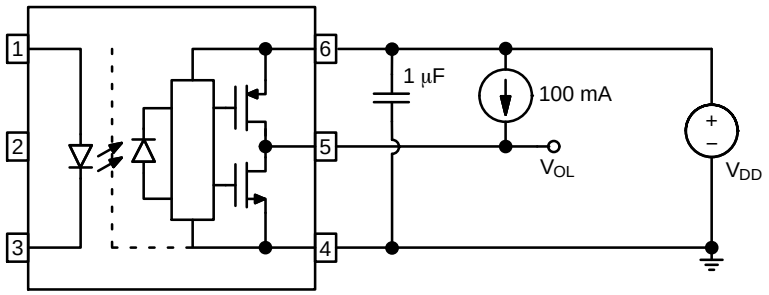


Figure 20. V_{OL} Test Circuit

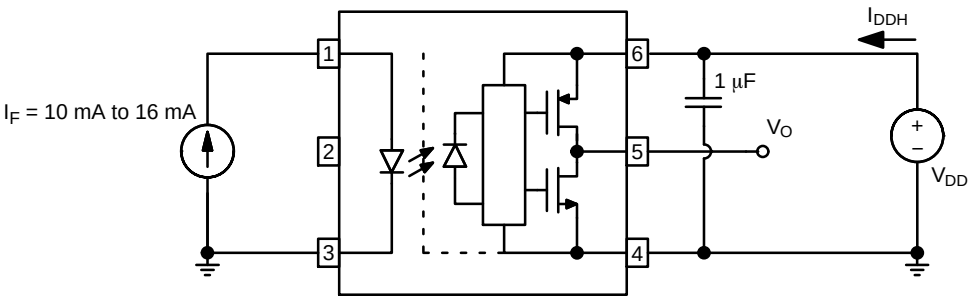


Figure 21. I_{DDH} Test Circuit

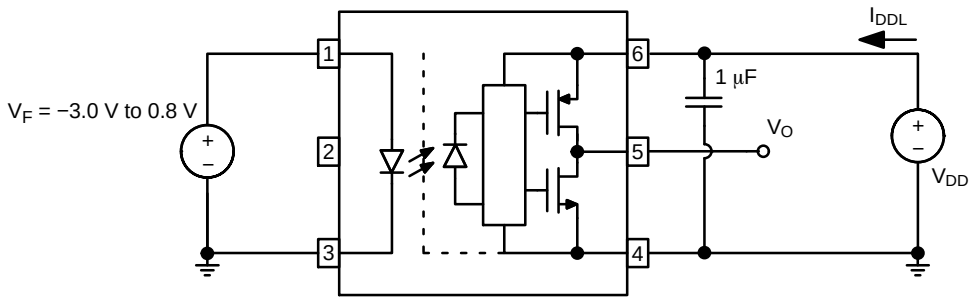


Figure 22. I_{DDL} Test Circuit

TEST CIRCUITS (Continued)

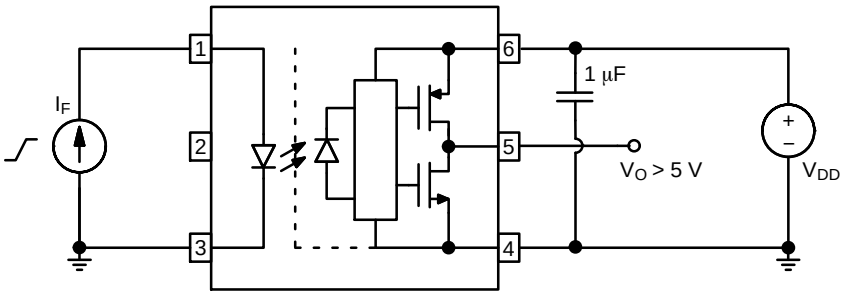


Figure 23. I_{FLH} Test Circuit

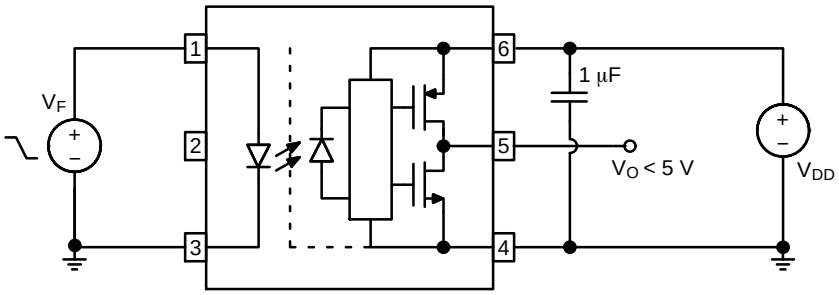


Figure 24. V_{FHL} Test Circuit

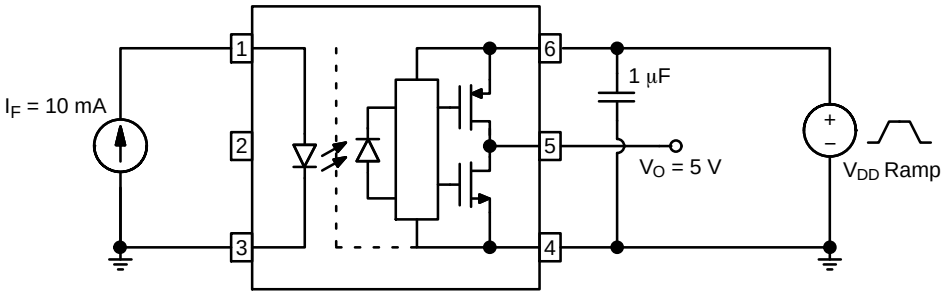


Figure 25. I_{DDH} Test Circuit

TEST CIRCUITS (Continued)

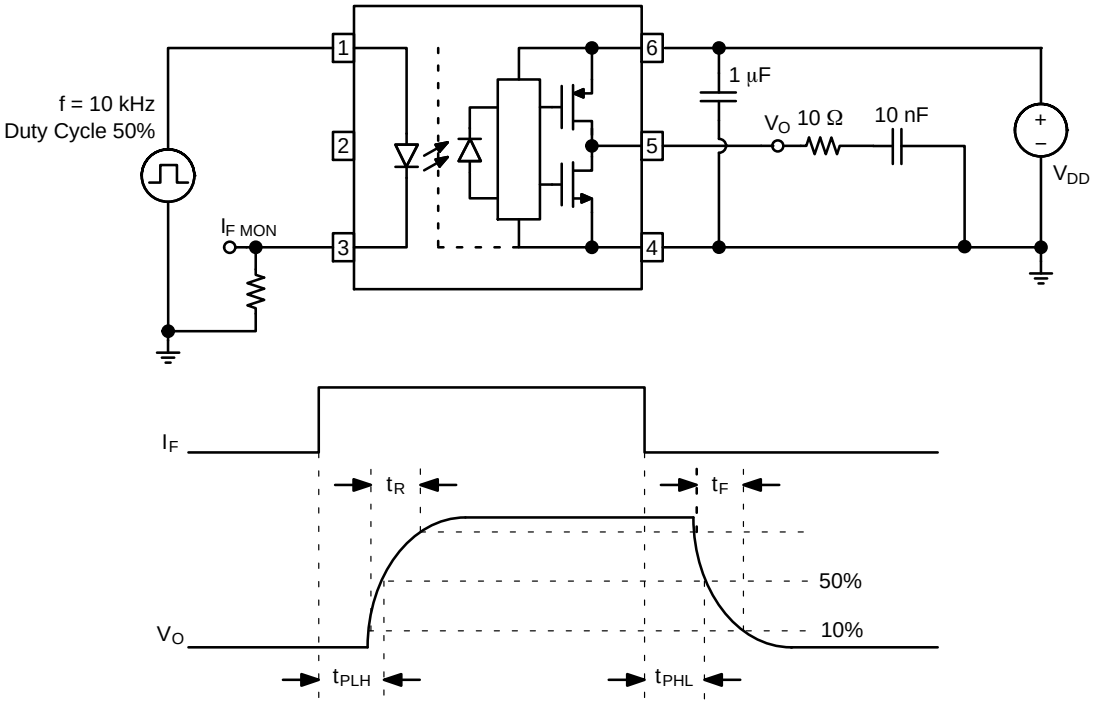


Figure 26. t_{PLH}, t_{PHL}, t_R and t_F Test Circuit and Waveforms

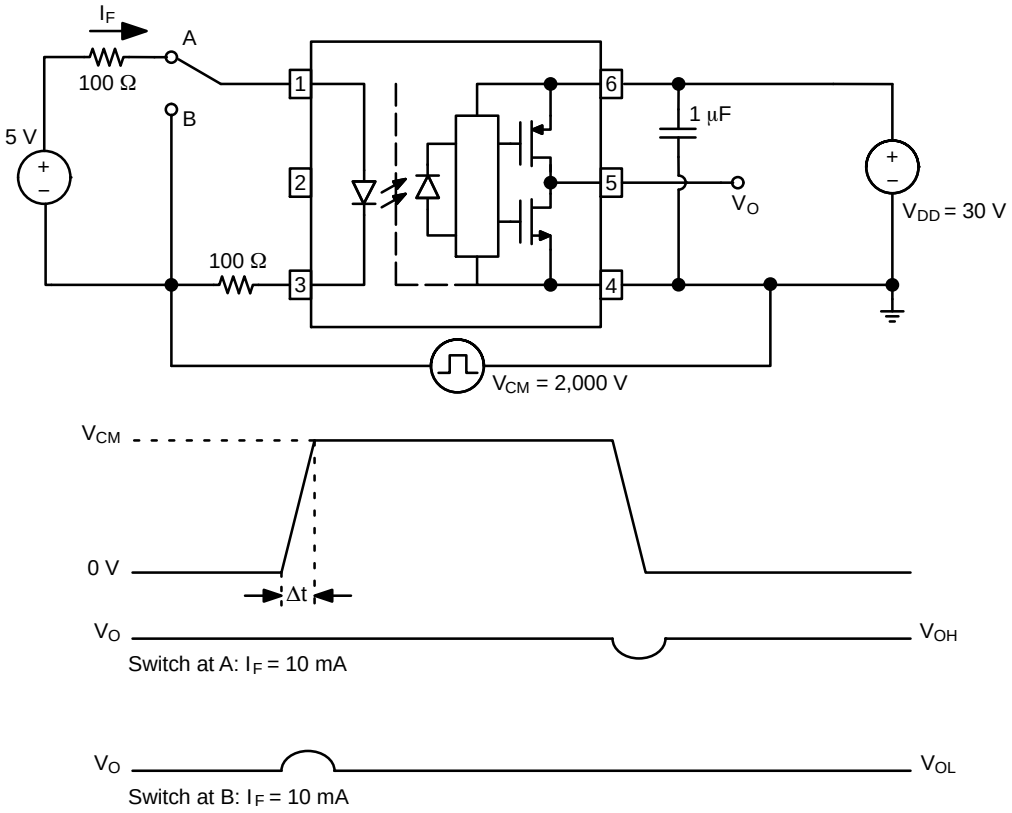
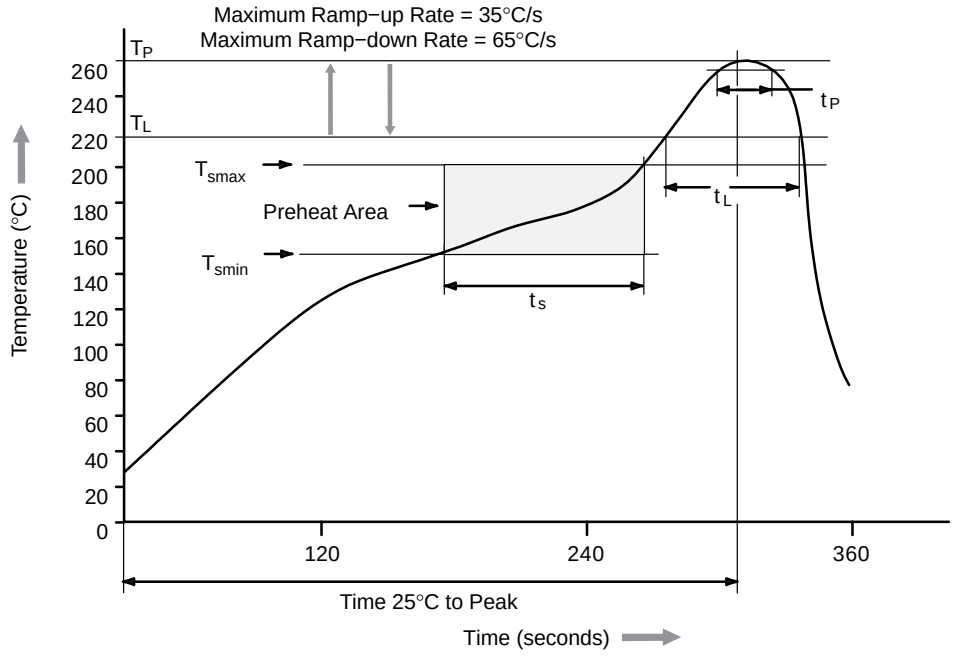


Figure 27. CMR Test Circuit and Waveforms

REFLOW PROFILE



Profile Feature	Pb−Free Assembly Profile
Temperature Minimum (T_{smin})	150°C
Temperature Maximum (T_{smax})	200°C
Time (t_S) from (T_{smin} to T_{smax})	60 s to 120 s
Ramp−up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 s to 150 s
Peak Body Package Temperature	260°C +0°C / −5°C
Time (t_P) within 5°C of 260°C	30 s
Ramp−Down Rate (T_P to T_L)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 28. Reflow Profile

ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
FOD8343	Stretched Body SOP 6−Pin	100 Units / Tube
FOD8343R2	Stretched Body SOP 6−Pin	1,000 / Tape & Reel
FOD8343V	Stretched Body SOP 6−Pin, DIN EN/IEC60747−5−5 Option	100 Units / Tube
FOD8343R2V	Stretched Body SOP 6−Pin, DIN EN/IEC60747−5−5 Option	1,000 / Tape & Reel
FOD8343T	Stretched Body SOP 6−Pin, Wide Lead	100 Units / Tube
FOD8343TR2	Stretched Body SOP 6−Pin, Wide Lead	1,000 / Tape & Reel
FOD8343TV	Stretched Body SOP 6−Pin, Wide Lead, DIN EN/IEC60747−5−5 Option	100 Units / Tube
FOD8343TR2V	Stretched Body SOP 6−Pin, Wide Lead, DIN EN/IEC60747−5−5 Option	1,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: All packages are lead free per JEDEC: J−STD−020B standard.

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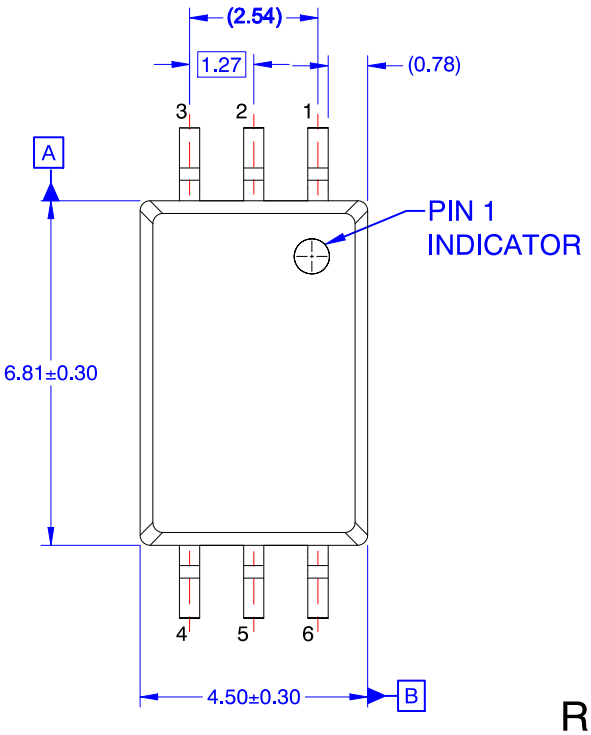
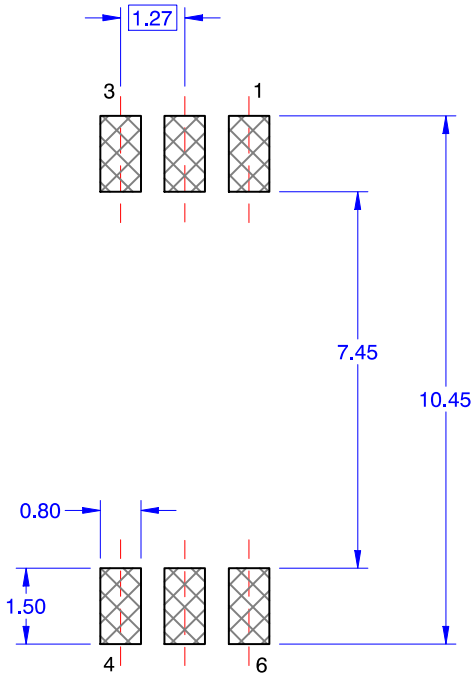
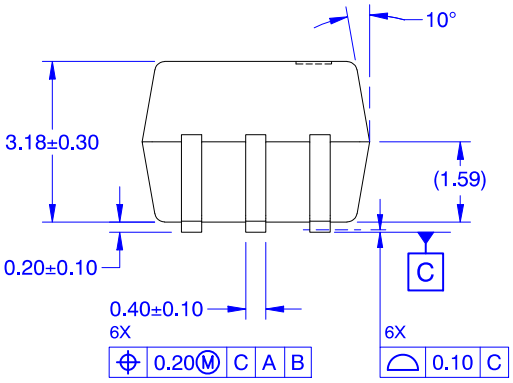
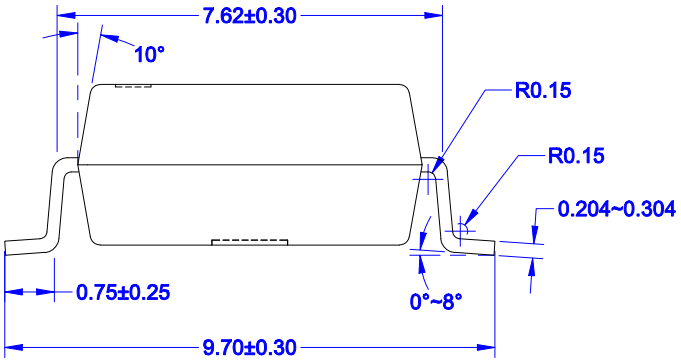




RECOMMENDED LAND PATTERN





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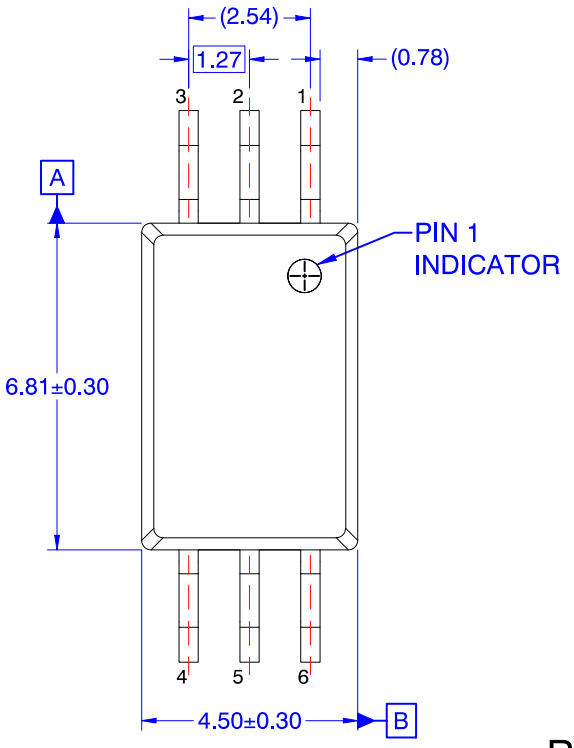

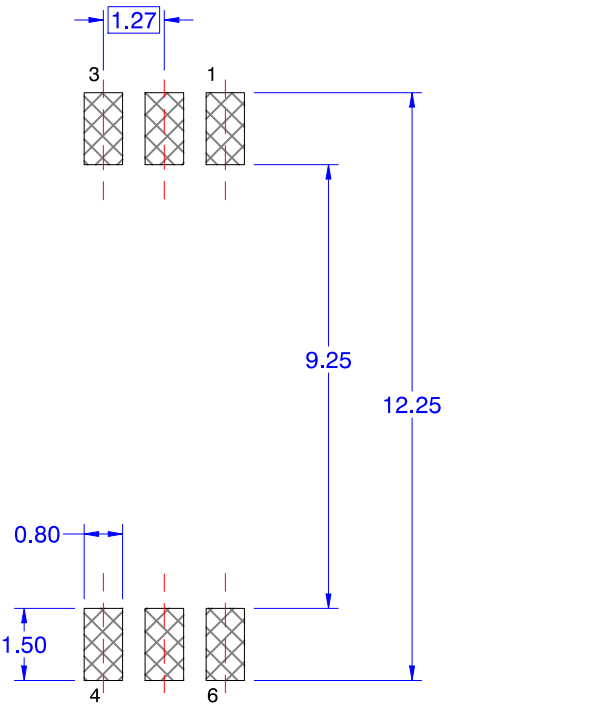

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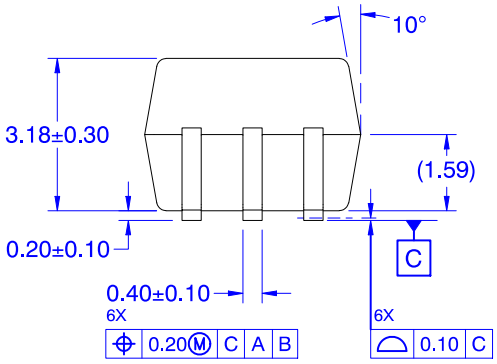

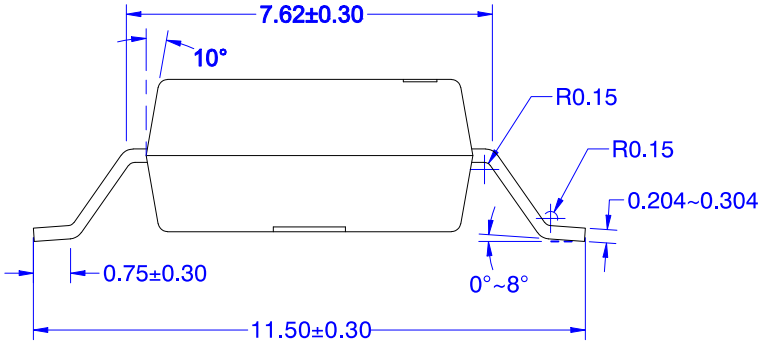

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