IGBT - SMPS II Series N-Channel with Anti-Parallel Stealth Diode 600 V

FGH50N6S2D

ON Semiconductor®

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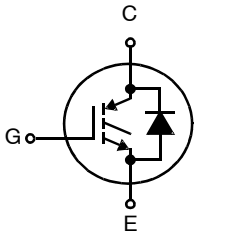
Description

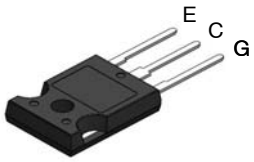
The FGH50N6S2D is a Low Gate Charge, Low Plateau Voltage SMPS II IGBT combining the fast switching speed of the SMPS IGBTs along with lower gate charge, plateau voltage and avalanche capability (UIS). These LGC devices shorten delay times, and reduce the power requirement of the gate drive. These devices are ideally suited for high voltage switched mode power supply applications where low conduction loss, fast switching times and UIS capability are essential. SMPS II LGC devices have been specially designed for:

- Power Factor Correction (PFC) Circuits
- Full Bridge Topologies
- Half Bridge Topologies
- Push−Pull Circuits
- Uninterruptible Power Supplies
- Zero Voltage and Zero Current Switching Circuits

Features

- 100 kHz Operation at 390 V, 40 A
- 200 kHz Operation at 390 V, 25 A
- 600 V Switching SOA Capability
- Typical Fall Time 90 ns at T_J = 125°C
- Low Gate Charge 70 nC at V_{GE} = 15 V
- Low Plateau Voltage 6.5 V Typical
- UIS Rated 480 mJ
- Low Conduction Loss
- This is a Pb−Free Device





TO−247−3LD
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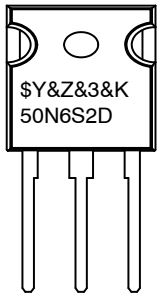
MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
50N6S2D	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Parameter		Symbol	Ratings	Unit
Collector to Emitter Breakdown Voltage		BV_{CES}	600	V
Collector Current Continuous	T_C = 25°C	I_C	75	A
	T_C = 110°C		60	A
Collector Current Pulsed (Note 1)		I_{CM}	240	A
Gate to Emitter Voltage Continuous		V_{GES}	±20	V
Gate to Emitter Voltage Pulsed		V_{GEM}	±30	V
Switching Safe Operating Area at T_J = 150°C, Figure 2		SSOA	150 A at 600 V	
Pulsed Avalanche Energy, I_{CE} = 30 A, L = 1 mH, V_{DD} = 50 V		E_{AS}	480	mJ
Power Dissipation Total	T_C = 25°C	P_D	463	W
Power Dissipation Derating	T_C > 25°C		3.7	W/°C
Operating Junction Temperature Range		T_J	−55 to +150	°C
Storage Junction Temperature Range		T_{STG}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse width limited by maximum junction temperature.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Tape Width	Quantity
50N6S2D	FGH50N6S2D	TO−247	N/A	30

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction−Case, IGBT	$R_{\theta JC}$	0.27	°C/W
Thermal Resistance Junction−Case, Diode	$R_{\theta JC}$	1.1	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
OFF STATE CHARACTERISTICS							
Collector to Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0 V,		600	–	–	V
Collector to Emitter Leakage Current	I_{CES}	V_{CE} = 600 V	T_J = 25°C	–	–	250	μA
			T_J = 125°C	–	–	2.8	mA
Gate to Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V		–	–	±250	nA
ON STATE CHARACTERISTICs							
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 A, V_{GE} = 15 V	T_J = 25°C	–	1.9	2.7	V
			T_J = 125°C	–	1.7	2.2	V
Diode Forward Voltage	V_{EC}	I_{EC} = 30 A		–	2.2	2.6	V
DYNAMIC CHARACTERISTICS							
Gate Charge	$Q_{G(ON)}$	I_C = 30 A, V_{CE} = 300 V	V_{GE} = 15 V	–	70	85	nC
			V_{GE} = 20 V	–	90	110	nC
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250 μA, V_{CE}= V_{GE}		3.5	4.3	5.0	V
Gate to Emitter Plateau Voltage	V_{GEP}	I_C = 30 A, V_{CE} = 300 V		–	6.5	8.0	V

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
Switching SOA	SSOA	T_J = 150°C, R_G = 3 Ω, V_{GE} = 15 V, L = 100 μH, V_{CE} = 600 V	150	–	–	A
Current Turn−On Delay Time	$t_{d(ON)I}$	IGBT and Diode at T_J = 25°C, I_{CE} = 30 A, V_{CE} = 390 V, V_{GE} = 15 V, R_G = 3 Ω, , L = 200 μH, Test Circuit − Figure 26	–	13	–	ns
Current Rise Time	t_{rI}		–	15	–	ns
Current Turn−Off Delay Time	$t_{d(OFF)I}$		–	55	–	ns
Current Fall Time	t_{fI}		–	50	–	ns
Turn−On Energy (Note 2)	E_{ON1}		–	260	–	μJ
Turn−On Energy (Note 2)	E_{ON2}		–	330	–	μJ
Turn−Off Energy Loss (Note 3)	E_{OFF}		–	250	350	μJ
Current Turn−On Delay Time	$t_{d(ON)I}$	IGBT and Diode at T_J = 125°C, I_{CE} = 30 A, V_{CE} = 390 V, V_{GE} = 15 V, R_G = 3 Ω, , L = 200 μH, Test Circuit − Figure 26	–	13	–	ns
Current Rise Time	t_{rI}		–	15	–	ns
Current Turn−Off Delay Time	$t_{d(OFF)I}$		–	92	150	ns
Current Fall Time	t_{fI}		–	88	100	ns
Turn−On Energy (Note 2)	E_{ON1}		–	260	–	μJ
Turn−On Energy (Note 2)	E_{ON2}		–	490	600	μJ
Turn−Off Energy (Note 3)	E_{OFF}		–	575	850	μJ
Diode Reverse Recovery Time	t_{rr}	I_{EC} = 30 A, dI_{EC}/dt = 200 A/μs	–	50	55	ns
		I_{EC} = 1 A, dI_{EC}/dt = 200 A/μs	–	30	42	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Values for two Turn−On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn−on loss of the IGBT only. E_{ON2} is the turn−on loss when a typical diode is used in the test circuit and the diode is at the same TJ as the IGBT. The diode type is specified in Figure 26.
3. Turn−Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). All devices were tested per JEDEC Standard No. 24−1 Method for Measurement of Power Device Turn−Off Switching Loss. This test method produces the true total Turn−Off Energy Loss.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

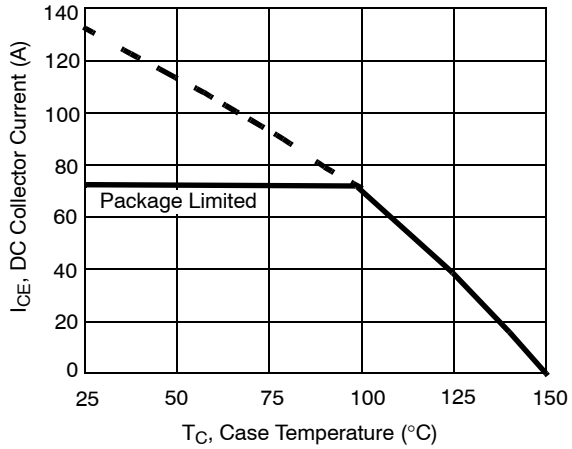


Figure 1. DC Collector Current vs. Case Temperature

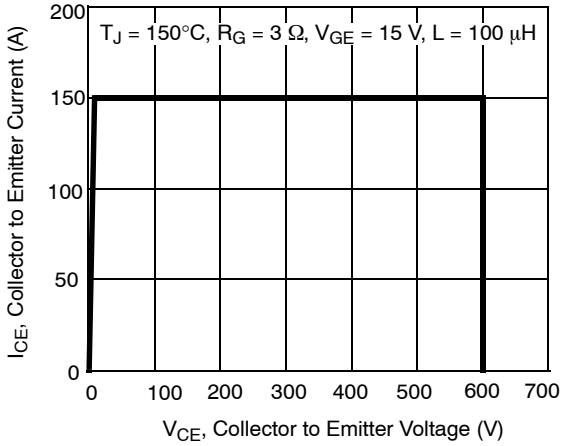


Figure 2. Minimum Switching Safe Operating Area

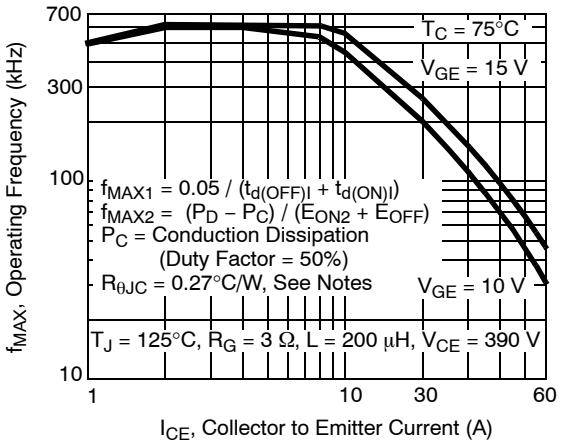


Figure 3. Operating Frequency vs. Collector to Emitter Current

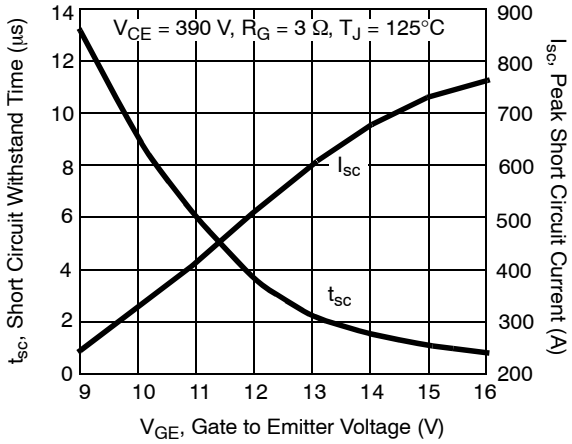


Figure 4. Short Circuit Withstand Time

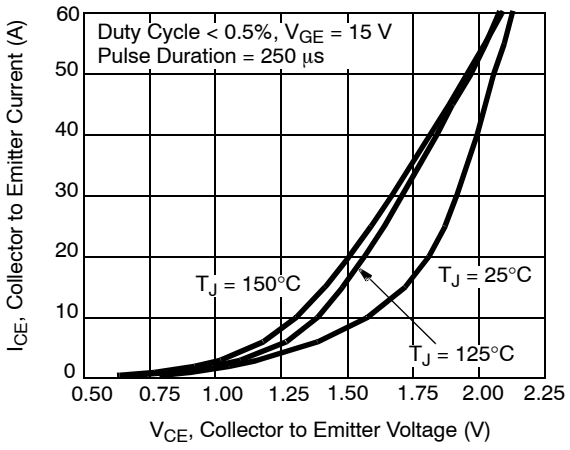


Figure 5. Collector to Emitter On−State Voltage

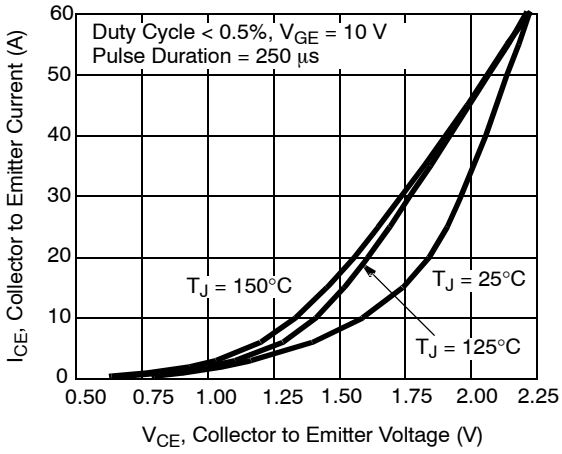


Figure 6. Collector to Emitter On−State Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted) (continued)

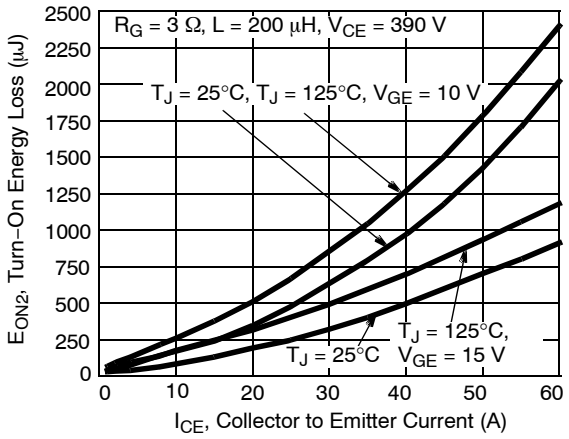


Figure 7. Turn−On Energy Loss vs. Collector to Emitter Current

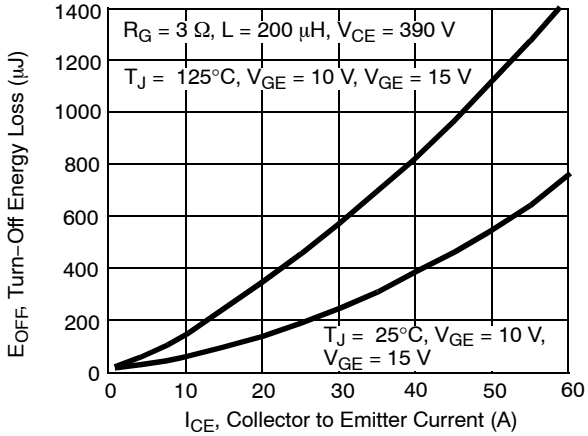


Figure 8. Turn−Off Energy Loss vs. Collector to Emitter Current

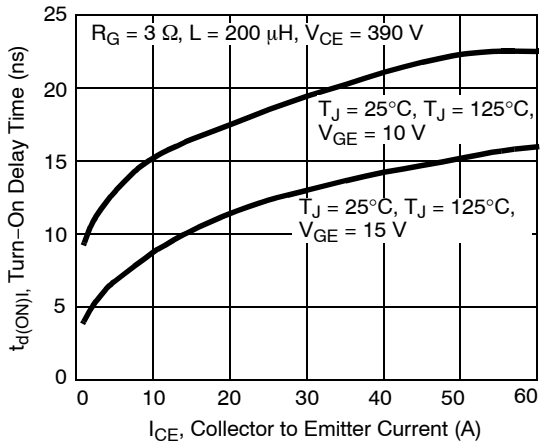


Figure 9. Turn−On Delay Time vs. Collector to Emitter Current

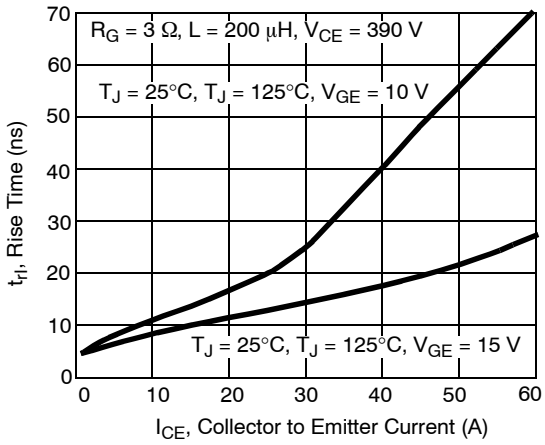


Figure 10. Turn−On Rise Time vs. Collector to Emitter Current

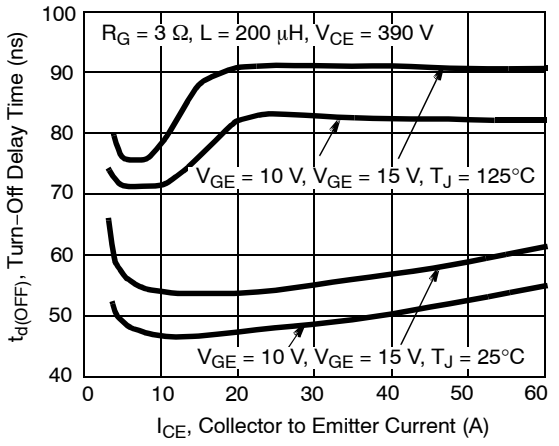


Figure 11. Turn−Off Delay Time vs. Collector to Emitter Current

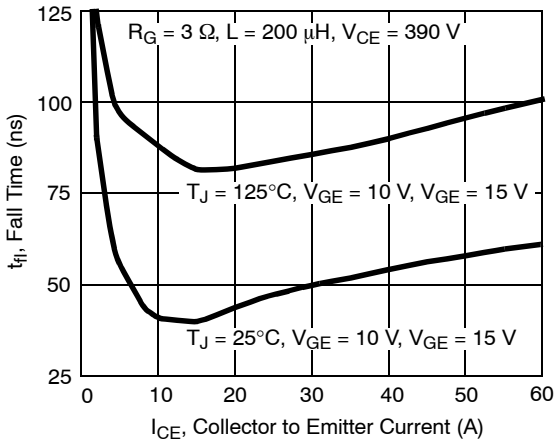


Figure 12. Fall Time vs. Collector to Emitter Current

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted) (continued)

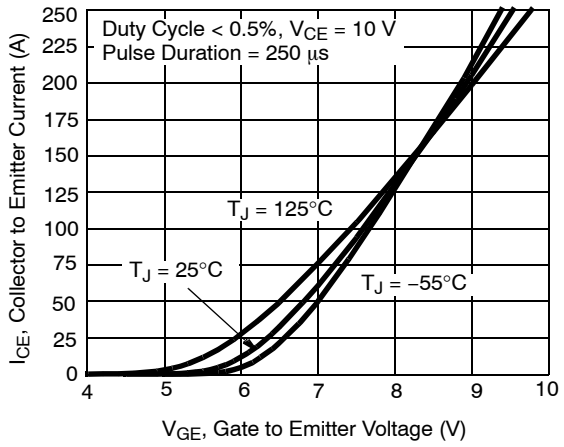


Figure 13. Transfer Characteristics

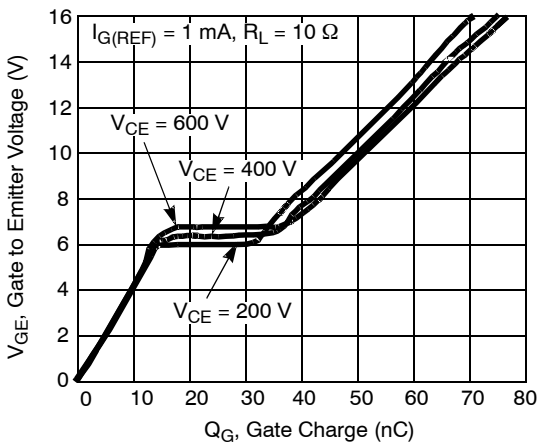


Figure 14. Gate Charge

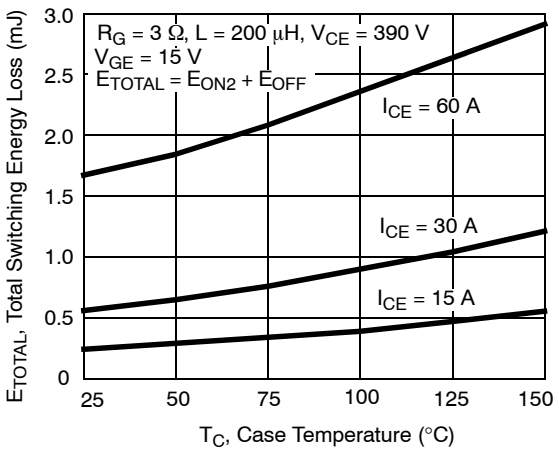


Figure 15. Total Switching Loss vs. Case Temperature

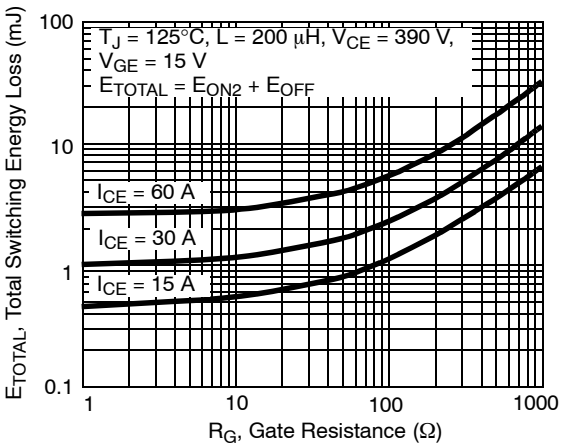


Figure 16. Total Switching Loss vs. Gate Resistance

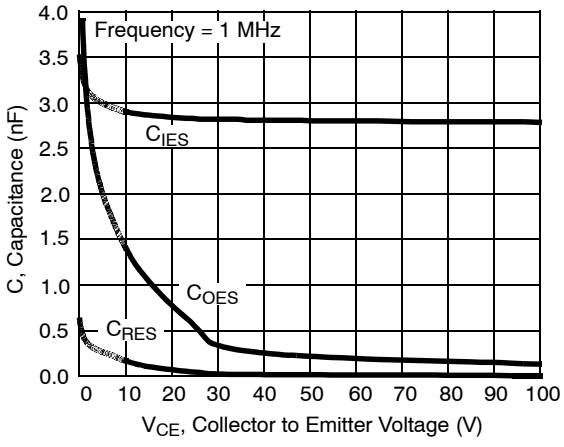


Figure 17. Capacitance vs. Collector to Emitter Voltage

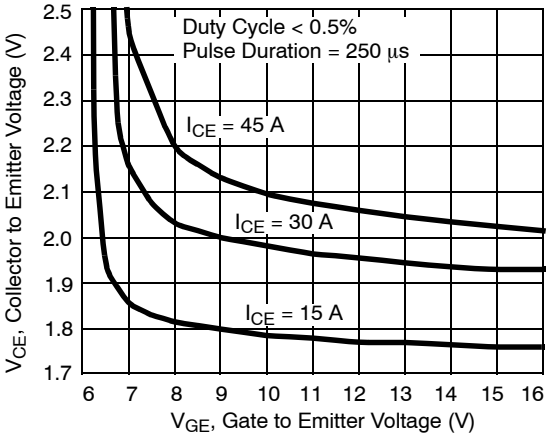


Figure 18. Collector to Emitter On−State Voltage vs. Gate to Emitter Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted) (continued)

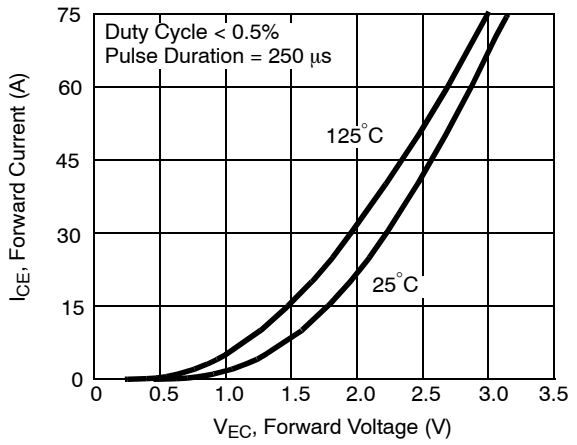


Figure 19. Diode Forward Current vs. Forward Voltage Drop

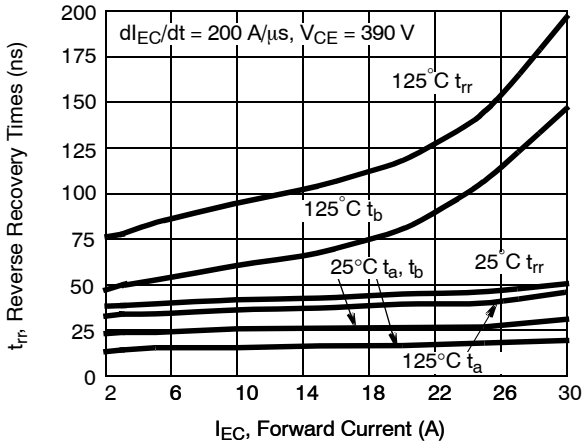


Figure 20. Recovery Times vs. Forward Current

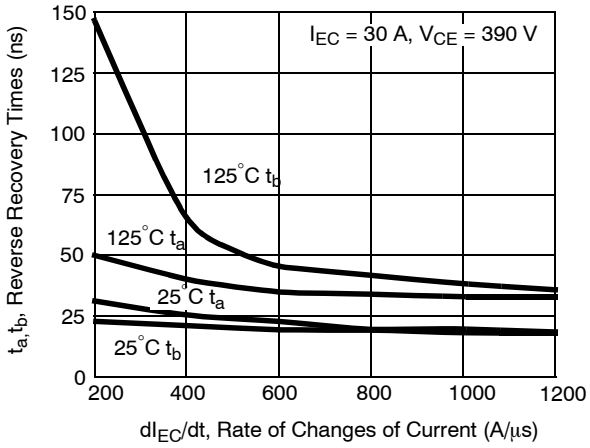


Figure 21. Recovery Times vs. Rate of Change of Current

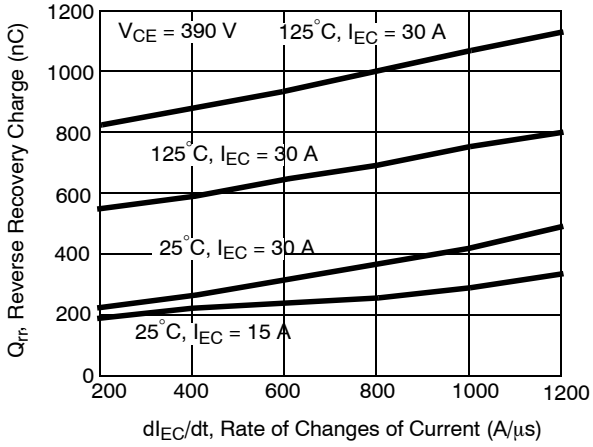


Figure 22. Stored Charge vs. Rate of Change of Current

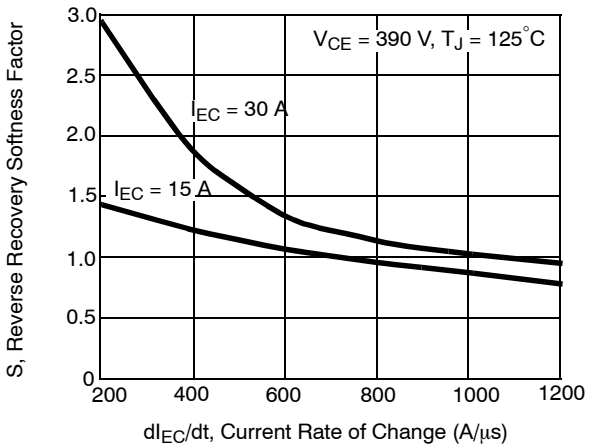


Figure 23. Reverse Recovery Softness Factor vs. Rate of Change of Current

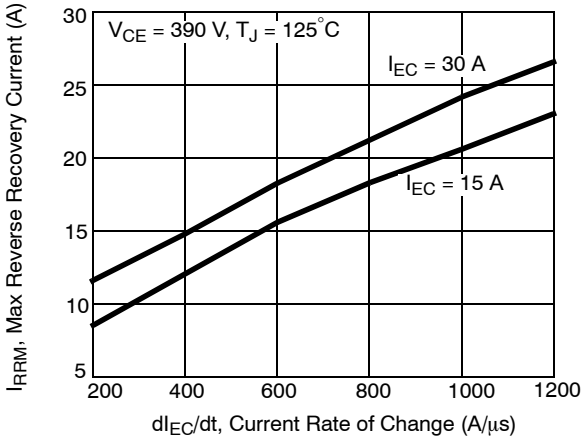


Figure 24. Maximum Reverse Recovery Current vs. Rate of Change of Current

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted) (continued)

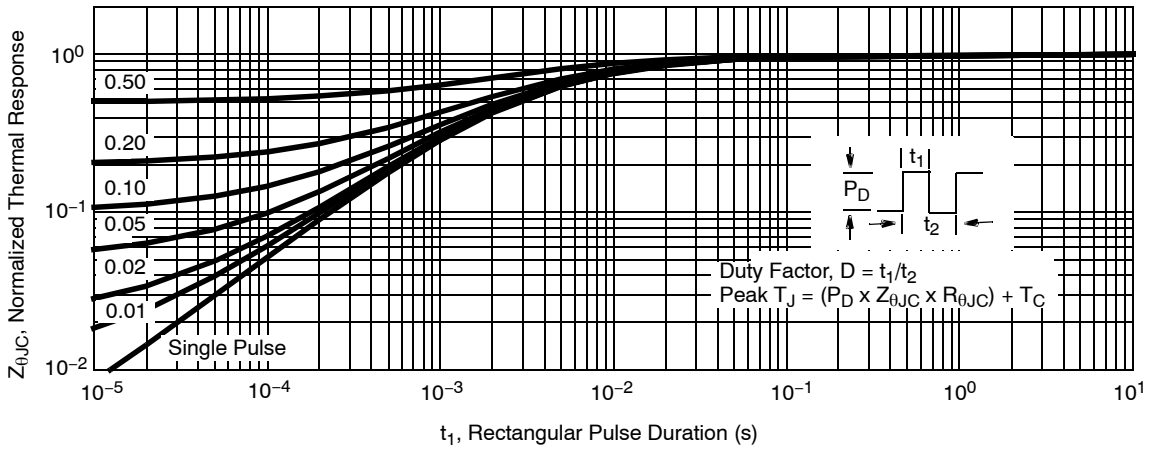


Figure 25. IGBT Normalized Transient Thermal Impedance, Junction to Case

TEST CIRCUIT AND WAVEFORMS

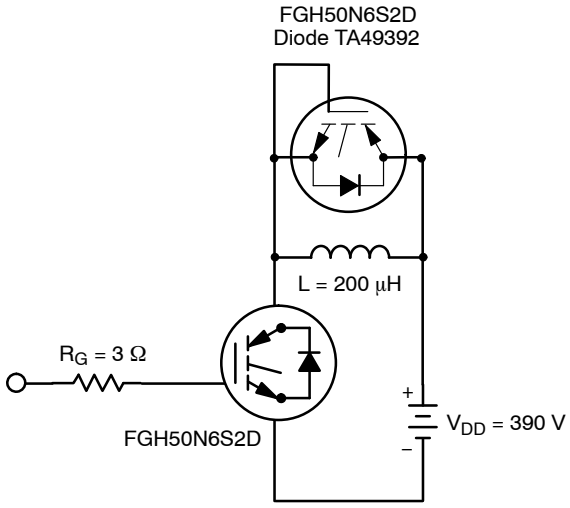


Figure 26. Inductive Switching Test Circuit

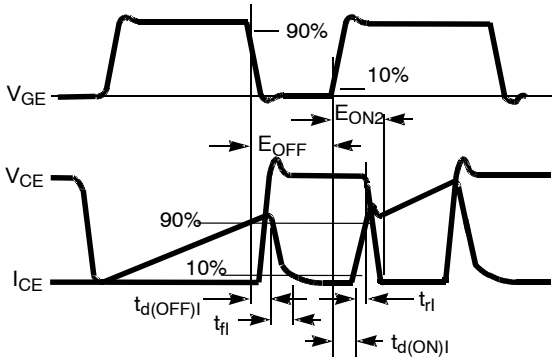


Figure 27. Switching Test Waveforms

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate−insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means − for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** − Never exceed the gate−voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** − The gates of these devices are essentially capacitors. Circuits that leave the gate open−circuited or floating should be avoided. These conditions can result in turn−on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** − These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

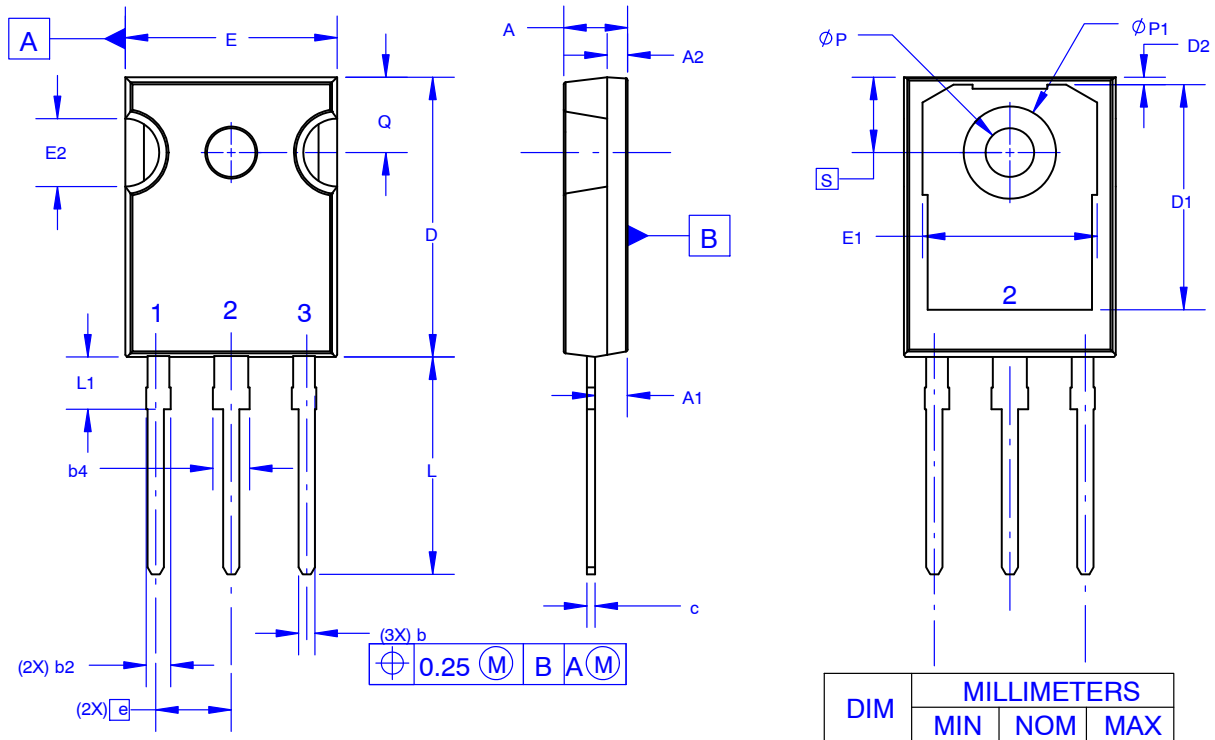
f_{MAX1} is defined by $f_{MAX1} = 0.05/_{(td(OFF)I} + td_{(ON)I)}$. Deadtime (the denominator) has been arbitrarily held to 10% of the on−state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 27. Device turn−off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 27. E_{ON2} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn−on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn−off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$)

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019

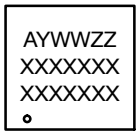


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TO−247−3LD SHORT LEAD**	**PAGE 1 OF 1**

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