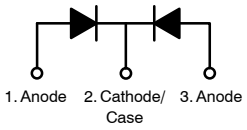
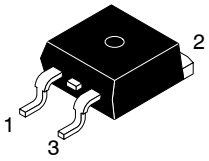
Silicon Carbide (SiC) Schottky Diode – EliteSiC, 20 A, 650 V, D2, D2PAK-3L

FFSB2065BDN-F085



Schottky Diode



D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ

Description

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size & cost.

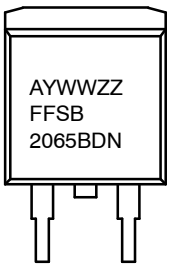
Features

- Max Junction Temperature 175°C
- Avalanche Rated 49 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- AEC–Q101 Qualified and PPAP Capable

Applications

- Automotive BEV–EV
- Automotive HEV–EV Onboard Chargers
- Automotive HEV–EV DC–DC Converters

MARKING DIAGRAM



A	= Assembly Plant Code
YWW	= Date Code (Year & Week)
ZZ	= Lot Code
FFSB2065BDN	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{RRM}	Peak Repetitive Reverse Voltage		650	V
E_{AS}	Single Pulse Avalanche Energy (Note 1)		49	mJ
I_F	Continuous Rectified Forward Current	@ T_C < 25°C	23.6	A
		@ T_C < 140°C	10	
$I_{F, Max}$	Non–Repetitive Peak Forward Surge Current	T_C = 25°C, 10 μs	600	A
		T_C = 150°C, 10 μs	554	
$I_{F, SM}$	Non–Repetitive Forward Surge Current, T_C = 25°C	Half–Sine Pulse, t_p = 8.3 ms	45	A
P_{tot}	Power Dissipation	T_C = 25°C	75	W
		T_C = 150°C	12.5	
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. E_{AS} of 49 mJ is based on starting T_J = 25°C, L = 0.5 mH, I_{AS} = 14 A, V = 50 V.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	2.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted − per leg)

Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Unit
V_F	Forward Voltage	I_F = 10 A, T_C = 25°C	−	1.38	1.75	V
		I_F = 10 A, T_C = 125°C	−	1.6	2.0	
		I_F = 10 A, T_C = 175°C	−	1.72	2.4	
I_R	Reverse Current	V_R = 650 V, T_C = 25°C	−	0.5	40	μA
		V_R = 650 V, T_C = 125°C	−	1	80	
		V_R = 650 V, T_C = 175°C	−	2	160	
Q_C	Total Capacitive Charge	V = 400 V	−	25	−	nC
C	Total Capacitance	V_R = 1 V, f = 100 kHz	−	421	−	pF
		V_R = 200 V, f = 100 kHz	−	46	−	
		V_R = 400 V, f = 100 kHz	−	35	−	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping†
FFSB2065BDN−F085	FFSB2065BDN	D2PAK	800 Units/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

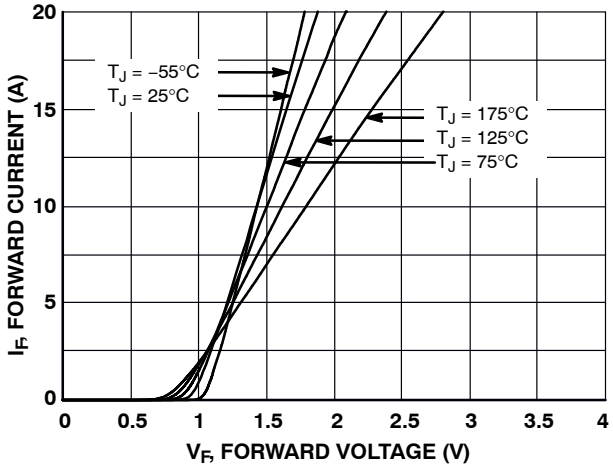


Figure 1. Forward Characteristics

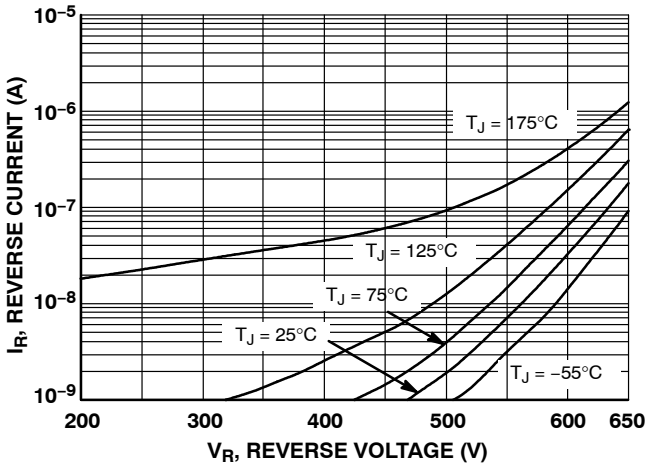


Figure 2. Reverse Characteristics

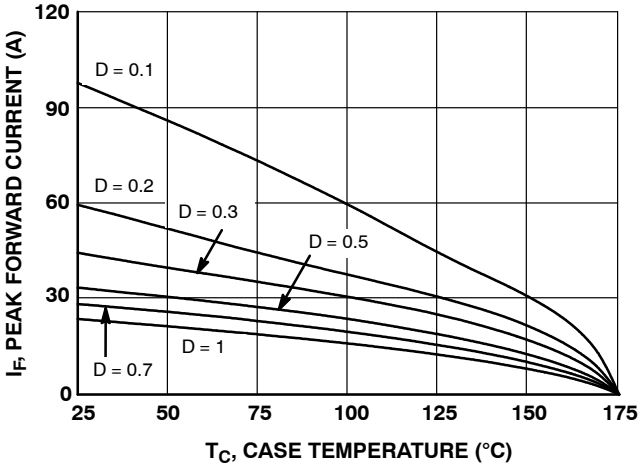


Figure 3. Current Derating

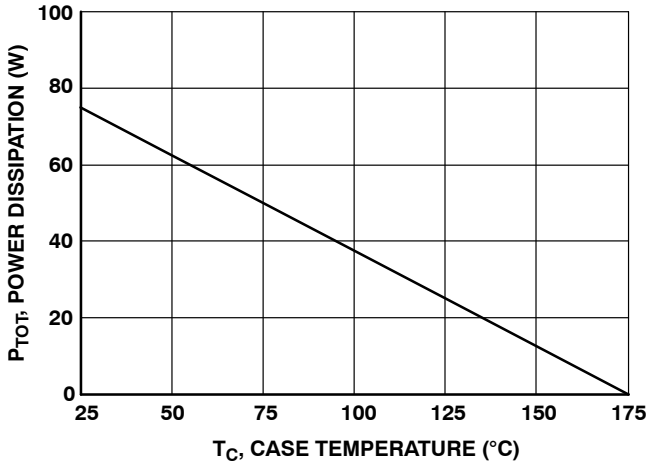


Figure 4. Power Derating

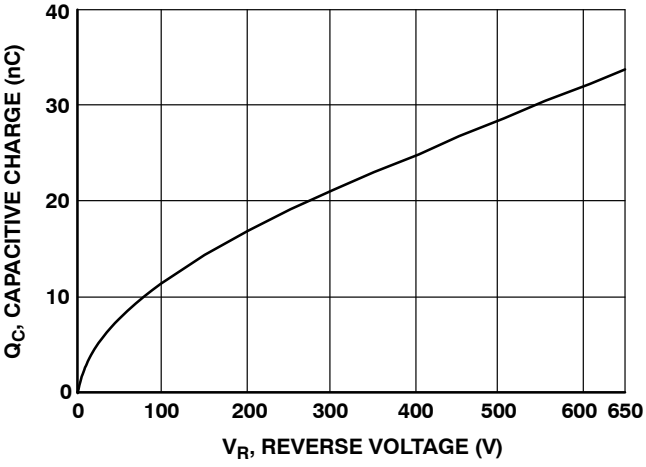


Figure 5. Capacitive Charge vs. Reverse Voltage

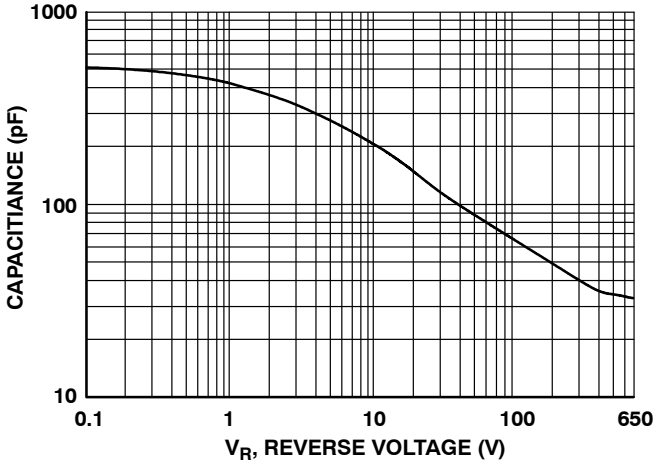


Figure 6. Capacitance vs. Reverse Voltage

TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (continued)

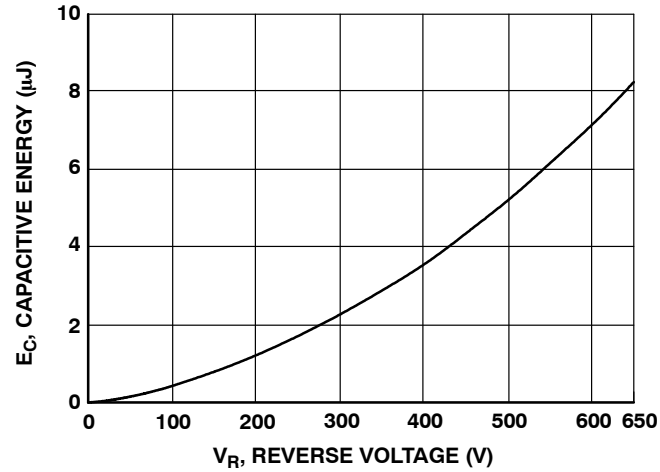


Figure 7. Capacitance Stored Energy

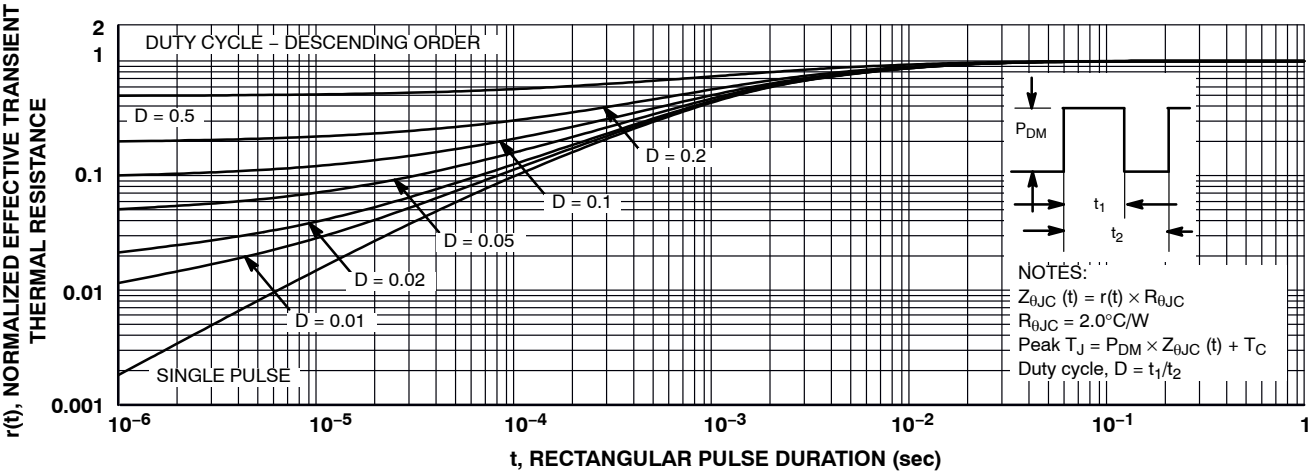


Figure 8. Junction−to−Case Transient Thermal Response Curve

TEST CIRCUIT AND WAVEFORMS

L = 0.5 mH
R < 0.1 Ω
V_{DD} = 50 V
EAVL = 1/2LI2 [$V_{R(AVL)}$ / ($V_{R(AVL)}$ − V_{DD})]
Q1 = IGBT (BV_{CES} > DUT $V_{R(AVL)}$)

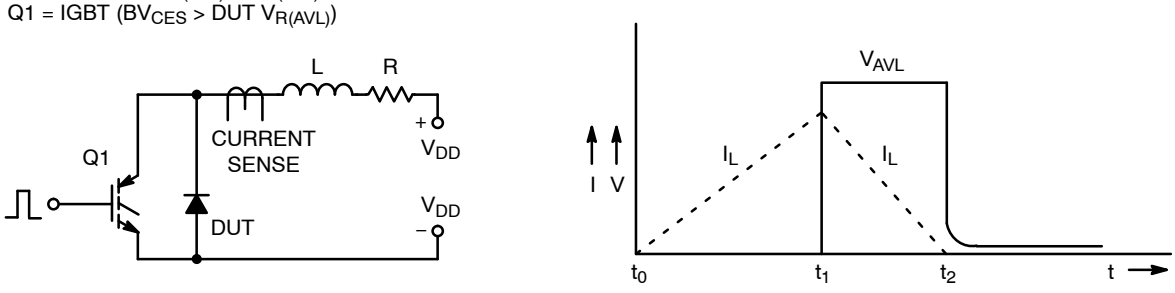


Figure 9. Unclamped Inductive Switching Test Circuit & Waveform

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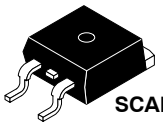
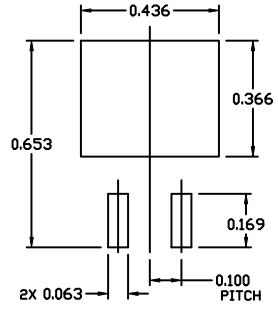
DATE 11 MAR 2021



SCALE 1:1



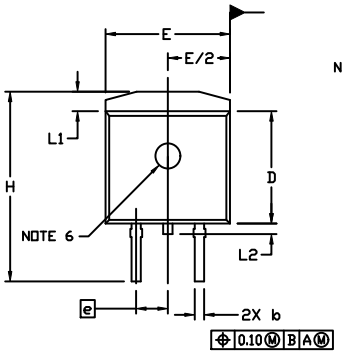
RECOMMENDED
MOUNTING FOOTPRINT

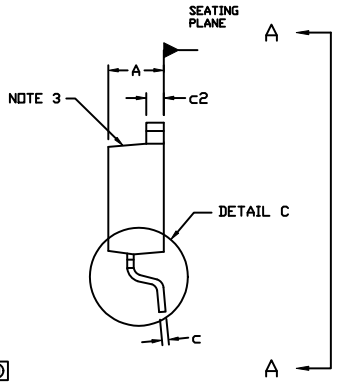
* For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

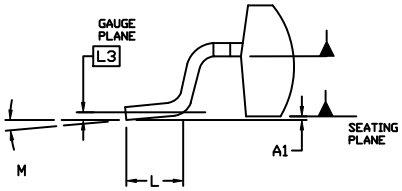
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② … OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

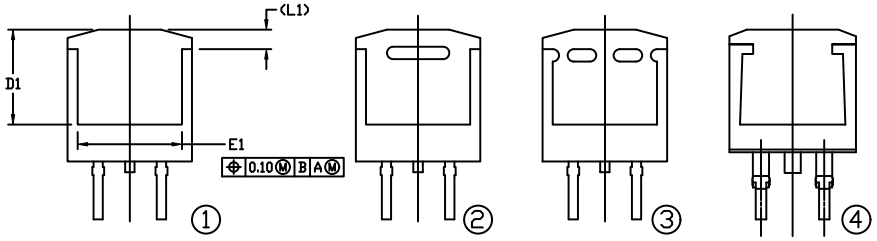
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°







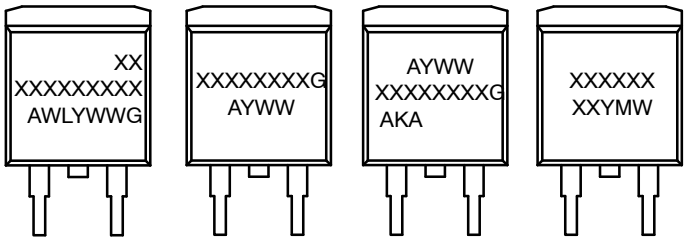
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC **Standard** **Rectifier** **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D²PAK–3 (TO–263, 3–LEAD)**	**PAGE 1 OF 1**

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