onsemi

MOSFET – N-Channel, POWERTRENCH[®]

100 V, 3.3 A, 100 m Ω

FDT86113LZ

General Description

This N–Channel logic Level MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been special tailored to minimize the on–state resistance and yet maintain superior switching performance. G–S zener has been added to enhance ESD voltage level.

Features

- Max $r_{DS(on)} = 100 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 3.3 \text{ A}$
- Max $r_{DS(on)} = 145 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 2.7 \text{ A}$
- High Performance Trench Technology for Extremely Low r_{DS(on)}
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- HBM ESD Protection Level > 3 kV Typical (Note 4)
- 100% UIL Tested
- This Device is Pb–Free and Halide Free

Applications

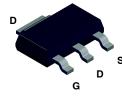
• DC – DC Switch

Specifications

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

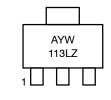
Symbol	Para	Ratings	Unit	
V _{DS}	Drain to Source Volta	100	V	
V _{GS}	Gate to Source Voltag	±20	V	
I _D	Drain Current	-Continuous	3.3	А
		-Pulsed	12	
E _{AS}	Single Pulse Avalance	9	mJ	
PD	Power Dissipation	T _A = 25°C (Note 1a)	2.2	W
		$T_A = 25^{\circ}C$ (Note 1b)	1.0	
T _J , T _{STG}	Operating and Storag Temperature Range	-55 to +150	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



SOT-223 CASE 318H

MARKING DIAGRAM



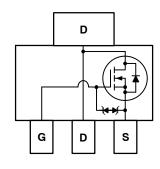
A = Assembly Location

= Year

Υ

- W = Work Week
- 113LZ = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARA	ACTERISTICS					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0 \ V$	100			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta \text{T}_{\text{J}}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu\text{A}, \text{Referenced to } 25^\circ\text{C}$		71		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μΑ
I _{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μΑ
ON CHARA	CTERISTICS					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \ \mu A$	1.0	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		-5		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 3.3 A		75	100	mΩ
. ,		V_{GS} = 4.5 V, I _D = 2.7 A		95	145	
		V_{GS} = 10 V, I _D = 3.3 A, T _J = 125°C		140	189	
9 FS	Forward Transconductance	V _{DS} = 10 V, I _D = 3.3 A		8		S
OYNAMIC C	HARACTERISTICS					
C _{iss}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		234	315	pF
C _{oss}	Output Capacitance			46	65	pF
C _{rss}	Reverse Transfer Capacitance			3.1	5	pF
SWITCHING	CHARACTERISTICS					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, \text{ I}_{D} = 3.3 \text{ A}, \text{ V}_{GS} = 10 \text{ V},$		3.8	10	ns
t _r	Rise Time	$R_{GEN} = 6 \Omega$		1.3	10	ns
t _{d(off)}	Turn-Off Delay Time			10	20	ns
t _f	Fall Time			1.5	10	ns
Qg	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_{D} = 3.3 A		4.1	6.8	nC
		V_{GS} = 0 V to 5 V, V_{DD} = 50 V, I_{D} = 3.3 A		2.3	3.9	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 50 V, I _D = 3.3 A		0.68		nC
Q _{gd}	Gate to Drain "Miller" Charge			0.85		nC
DRAIN-SOL	JRCE DIODE CHARACTERISTICS					
V _{SD} Source to Drain Diode Forward		$V_{GS} = 0 \text{ V}, \text{ I}_{S} = 3.3 \text{ A} \text{ (Note 2)}$		0.86	1.3	V
	Voltage			0.77	10	1

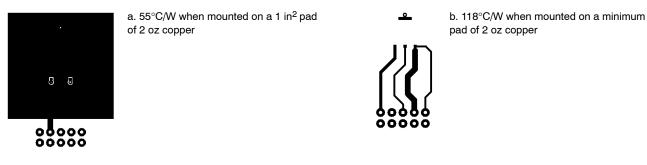
V _{SD}	Voltage	$V_{GS} = 0 V, I_S = 3.3 A (Note 2)$	0.86	1.3	v
	Voltage	V _{GS} = 0 V, I _S = 1.0 A (Note 2)	0.77	1.2	
t _{rr}	Reverse Recovery Time	I _F = 3.3 A, di/dt = 100 A/μs	31	49	ns
Q _{rr}	Reverse Recovery Charge		21	34	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

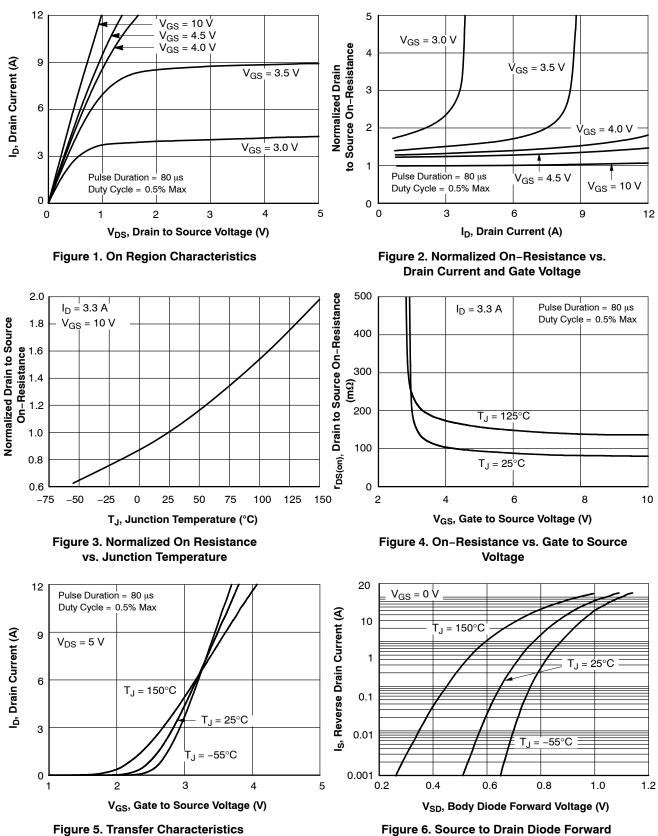
1. R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

 $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

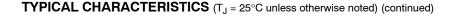


- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
 Starting T_J = 25°C, L = 0.3 mH, I_{AS} = 8 A, V_{DD} = 90 V, V_{GS} = 10 V.
 The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)



Voltage vs. Source Current



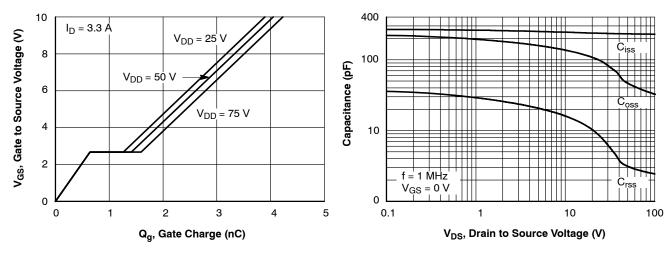


Figure 7. Gate Charge Characteristics

= 25°C

7

6

5

4

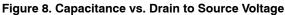
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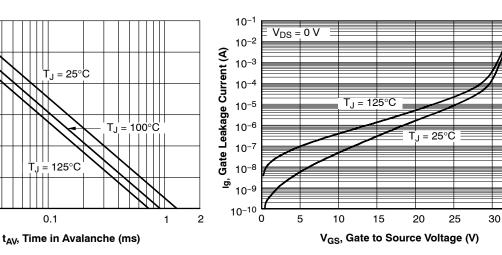
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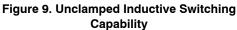
1

0.01

I_{AS}, Avalanche Current (A)







0.1

T_J = 125°C

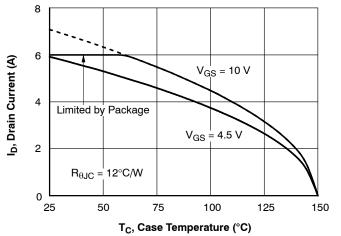
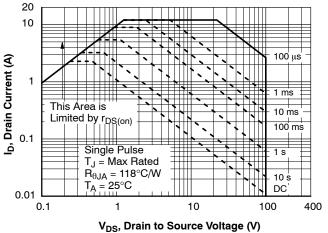




Figure 10. Gate Leakage Current vs Gate to Source Voltage

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TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

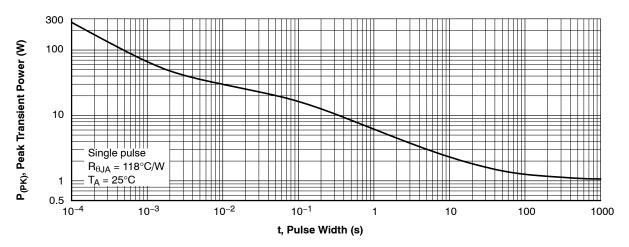


Figure 13. Single Pulse Maximum Power Dissipation

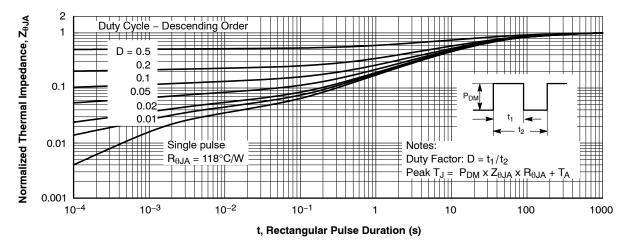


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

ORDERING INFORMATION

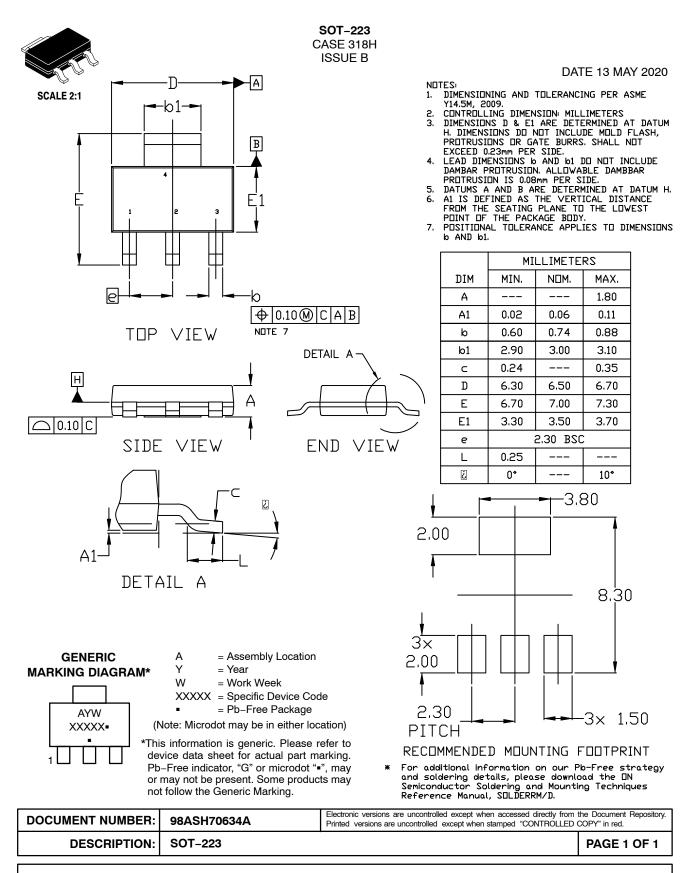
Device	Device Marking	Package Type	Shipping [†]
FDT86113LZ	113LZ	SOT-223 (Pb-Free)	4000 units / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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