

Transistor, N-Channel, Field Effect, Enhancement Mode, 2.5 V Specified

FDT439N

General Description

This N-Channel enhancement mode power field effect transistor is produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These products are well suited to low voltage, low current applications such as notebook computer power management, battery powered circuits, and DC motor control.

Features

• 6.3 A, 30 V

 $R_{DS(on)} = 0.045 \ \Omega \ @ \ V_{GS} = 4.5 \ V$ $R_{DS(on)} = 0.058 \ \Omega \ @ \ V_{GS} = 2.5 \ V$

- Fast switching speed.
- High power and current handling capability in a widely used surface mount package.
- This Device is Pb-Free

Applications

- DC/DC Converter
- Load Switch
- Motor Driving

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ unless otherwise noted)

Symbol	Pa	Ratings	Unit	
V _{DSS}	Drain-Source Volta	30	V	
V _{GSS}	Gate-Source Voltag	±8	V	
I _D	Drain Current	- Continuous (Note 1a)	6.3	Α
		- Pulsed	20	
P_{D}	Power	(Note 1a)	3	W
	Dissipation for Single Operation	(Note 1b)	1.3	
	g	(Note 1c)	1.1	
T _J , T _{stg}	Operating and Stora Temperature Range		-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

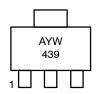
Symbol	Parameter	Ratings	Unit
RθJA	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	°C/W
Rejc	Thermal Resistance, Junction-to-Case (Note 1)	12	°C/W

V _{DSS}	R _{DS(ON)} MAX	I _D MAX	
30 V	0.045 Ω @ 4.5 V	6.3 A	
	0.058 Ω @ 2.5 V		



SOT-223 CASE 318H

MARKING DIAGRAM

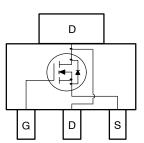


= Specific Device Code

Y = Date Code W = Work Week

439 = Specific Device Code

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARA	CTERISTICS					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	-	_	V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA,Referenced to 25°C	-	40	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	-	-	1	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 8 V, V _{DS} = 0 V	-	-	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	-100	nA
ON CHARAC	CTERISTICS (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.4	0.67	1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	-2.2	-	mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_{D} = 6.3 A V_{GS} = 4.5 V, I_{D} = 6.3 A, T_{J} = 125°C V_{GS} = 2.5 V, I_{D} = 5.5 A	- - -	0.038 0.055 0.048	0.045 0.072 0.058	Ω
I _{D(on)}	On-State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V	10	-	_	Α
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 6.3 A	-	17	_	S
DYNAMIC (CHARACTERISTICS					
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	-	500	_	pF
C _{oss}	Output Capacitance	1	-	185	_	pF
C _{rss}	Reverse Transfer Capacitance		-	43	_	pF
SWITCHING	CHARACTERISTICS (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, I_D = 1 \text{ A}, V_{GS} = 4.5 \text{ V},$	-	6	12	ns
t _r	Turn-On Rise Time	$R_{GEN} = 6 \Omega$	_	10	18	ns
t _{d(off)}	Turn-Off Delay Time		_	30	48	ns
t _f	Turn-Off Fall Time		-	10	18	ns
Q_g	Total Gate Charge	$V_{DS} = 15 \text{ V}, I_D = 6.3 \text{ A}, V_{GS} = 4.5 \text{ V}$	-	10.7	15	nC
Q _{gs}	Gate-Source Charge		_	0.9	_	nC
Q_{gd}	Gate-Drain Charge		_	3.7	_	nC
DRAIN-SOU	IRCE DIODE CHARACTERISTICS AND I	MAXIMUM RATIINGS				
I _S	Maximum Continuous Drain-Source Dio	de Forward Current	_	_	2.5	Α
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.5 \text{ A} \text{ (Note 2)}$	-	0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



 a. 42°C/W when mounted on a 1 in² pad of 2 oz copper.



b. 95°C/W when mounted on a 0.066 in² pad of 2 oz copper.



c. 110°C/W when mounted on a minimum mounting pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty cycle \leq 2.0 %.

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TYPICAL CHARACTERISTICS

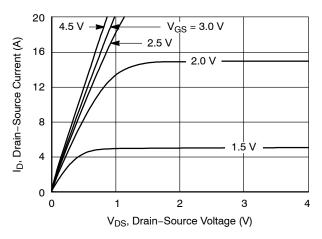


Figure 1. On-Region Characteristics

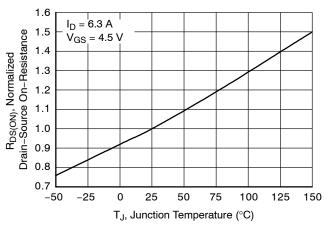


Figure 3. On–Resistance Variation with Temperature

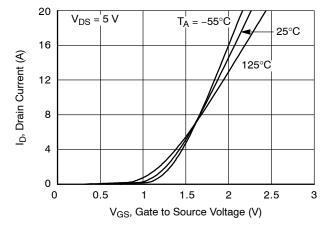


Figure 5. Transfer Characteristics

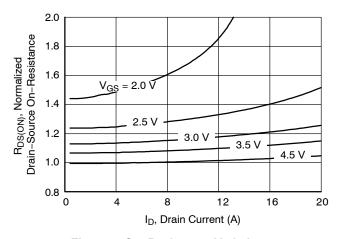


Figure 2. On–Resistance Variation with Drain Current and Gate Voltage

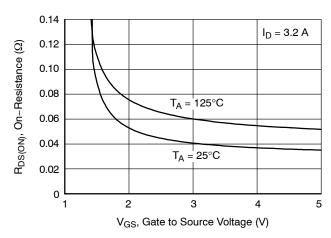


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

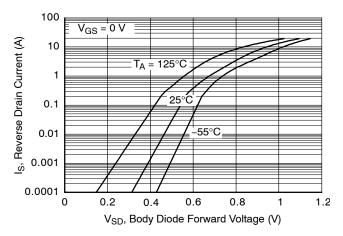


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

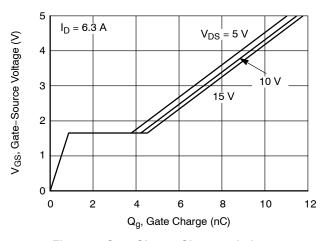


Figure 7. Gate Charge Characteristics

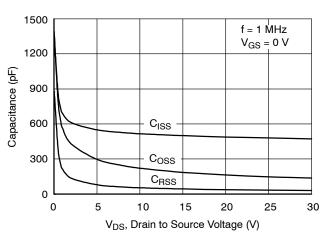


Figure 8. Capacitance Characteristics

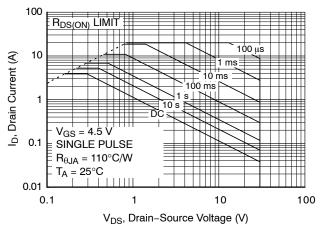


Figure 9. Maximum Safe Operating Area

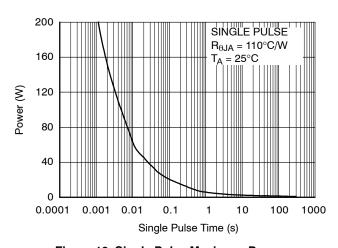


Figure 10. Single Pulse Maximum Power Dissipation

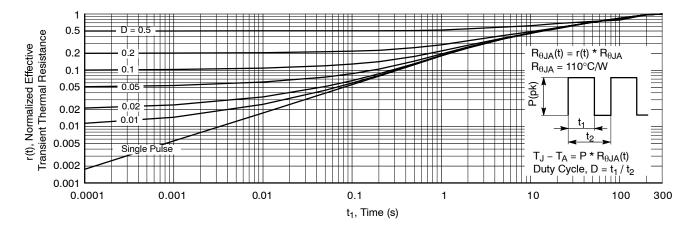


Figure 11. Transient Thermal Response Curve

(Note: Thermal characterization performed using the conditions described in Note 1. Transient thermal response will change depending on the circuit board design.)

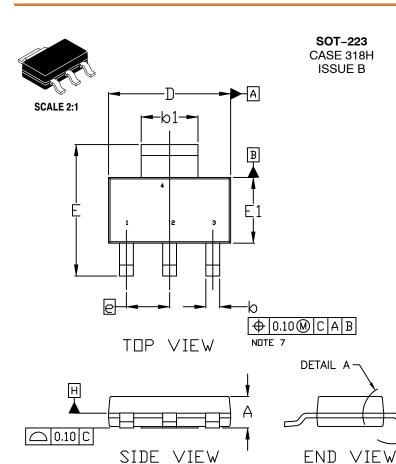
FDT439N

ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDT439N	439	SOT-223 (Pb-free)	13"	12 mm	4000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





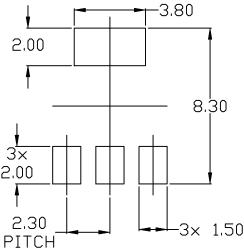
DATE 13 MAY 2020

NUTES:

- DIMENSIONING AND TOLERANCING PER ASME
- DIMENSIDNING AND TOLERANCING PER ASME Y14.5M, 2009.
 CONTROLLING DIMENSION: MILLIMETERS DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS DR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
 LEAD DIMENSIONS & AND &1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
 DATUMS A AND B ARE DETERMINED AT DATUM H. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
 POSITIONAL TOLERANCE APPLIES TO DIMENSIONS & AND &1.

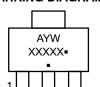
- b AND b1.

	MILLIMETERS			
DIM	MIN.	N□M.	MAX.	
Α			1.80	
A1	0.02	0.06	0.11	
b	0.60	0.74	0.88	
b1	2.90	3.00	3.10	
С	0.24		0.35	
D	6.30	6.50	6.70	
E	6.70	7.00	7.30	
E1	3.30	3.50	3.70	
е	2.30 BSC			
L	0.25			
Ż	0*		10°	



GENERIC MARKING DIAGRAM*

A1



= Assembly Location

Υ = Year

DETAIL A

W = Work Week

XXXXX = Specific Device Code

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the IIN Semiconductor Soldering and Mounting Techniques Reference Manual, SILDERRM/D.

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DESCRIPTION:	SOT-223		PAGE 1 OF 1	

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