ON Semiconductor

Is Now



To learn more about onsemi™, please visit our website at www.onsemi.com

onsemi and ONSEMI. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/ or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application,



ON Semiconductor®

FDS8896 N-Channel PowerTrench® MOSFET

30V, **15A**, **6**.0m Ω

Features

- $r_{DS(on)} = 6.0 \text{m}\Omega$, $V_{GS} = 10 \text{V}$, $I_D = 15 \text{A}$
- $r_{DS(on)} = 7.3 m\Omega$, $V_{GS} = 4.5 V$, $I_D = 14 A$
- High performance trench technology for extremely low r_{DS(on)}
- Low gate charge
- High power and current handling capability
- RoHS Compliant



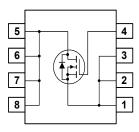
General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{\text{DS}(\text{on})}$ and fast switching speed.

Applications

■ DC/DC converters





Symbol	Parameter	Ratings	Units
V _{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
	Drain Current		
	Continuous ($T_A = 25^{\circ}$ C, $V_{GS} = 10$ V, $R_{\theta JA} = 50^{\circ}$ C/W)	15	Α
ID	Continuous ($T_A = 25^{\circ}$ C, $V_{GS} = 4.5$ V, $R_{\theta JA} = 50^{\circ}$ C/W)	14	Α
	Pulsed	110	Α
E _{AS}	Single Pulse Avalanche Energy (Note 1)	196	mJ
	Power dissipation	2.5	W
P_{D}	Derate above 25°C	20	mW/°C
T _J , T _{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{ heta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2b)	125	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8896	FDS8896	SO-8	330mm	12mm	2500 units

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Тур	Max	Units
Off Chara	cteristics						
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS}$	s = 0V	30	-	-	V
1	Zero Gate Voltage Drain Current	V _{DS} = 24V		-	1	1	^
IDSS	Zero Gate Voltage Drain Current	$V_{GS} = 0V$	$T_{\rm J} = 150^{\rm o}{\rm C}$	-	-	250	μА
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA

On Characteristics

V _{GS(TH)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1.2	-	2.5	V
		I _D = 15A, V _{GS} = 10V	-	4.9	6.0	
r · ·	Drain to Source On Resistance	$I_D = 14A, V_{GS} = 4.5V$	-	5.8	7.3	mΩ
r _{DS(on)}		$I_D = 15A, V_{GS} = 10V,$ $T_J = 150^{\circ}C$	-	7.8	10.1	11152

Dynamic Characteristics

C_{ISS}	Input Capacitance	\\ -45\\\\ -0\\	-	2525	-	pF
C _{OSS}	Output Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ = 1MHz	-	490	-	pF
C _{RSS}	Reverse Transfer Capacitance	1 11/11/2	ı	300	-	pF
R_G	Gate Resistance	$V_{GS} = 0.5V$, $f = 1MHz$	0.6	2.4	4.2	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V _{GS} = 0V to 10V	ı	50	67	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0V \text{ to } 5V$ $V_{DD} = 15V$ $I_{D} = 15A$	ı	28	36	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 1V$ $I_{G} = 1.0 \text{mA}$	ı	2.5	3.2	nC
Q_{gs}	Gate to Source Gate Charge	.g	-	7.0	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau		-	4.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	11	-	nC

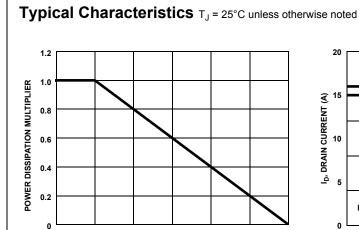
Switching Characteristics	$(V_{GS} = 10V)$
---------------------------	------------------

t _{ON}	Turn-On Time		-	-	68	ns
t _{d(ON)}	Turn-On Delay Time		-	8	-	ns
t _r	Rise Time	V _{DD} = 15V, I _D = 14A	-	37	-	ns
t _{d(OFF)}	Turn-Off Delay Time	$V_{GS} = 10V, R_{GS} = 6.2\Omega$	-	60	-	ns
t _f	Fall Time		-	24	-	ns
t _{OFF}	Turn-Off Time		-	-	126	ns

Drain-Source Diode Characteristics

V	Source to Drain Diode Voltage	I _{SD} = 15A	ı	ı	1.25	V
v_{SD}	Source to Drain Diode voltage	I _{SD} = 2.1A	-	-	1.0	V
t _{rr}	Reverse Recovery Time	I_{SD} = 15A, dI_{SD}/dt = 100A/ μ s	-	-	29	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 15A, dI_{SD}/dt = 100A/ μ s	-	-	15	nC

- Notes:
 1: Starting T_J = 25°C, L = 1mH, I_{AS} = 19.8A, V_{DD} = 30V, V_{GS} = 10V.
 2: R_{0,IA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,IC} is guaranteed by design while R_{0,JA} is determined by the user's board design.
 a) 50°C/W when mounted on a 1in² pad of 2 oz copper.
 - b) 125°C/W when mounted on a minimum pad.



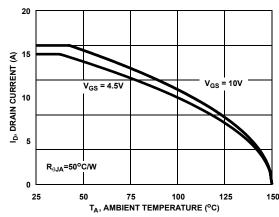


Figure 1. Normalized Power Dissipation vs
Ambient Temperature

75

T_A, AMBIENT TEMPERATURE (°C)

100

125

150

50

0

25

Figure 2. Maximum Continuous Drain Current vs
Ambient Temperature

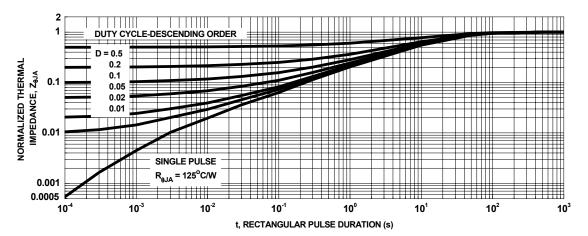


Figure 3. Normalized Maximum Transient Thermal Impedance

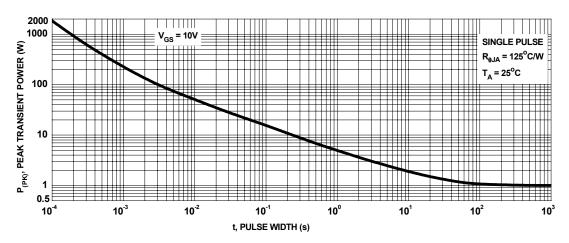
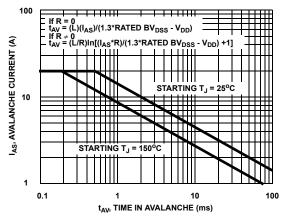
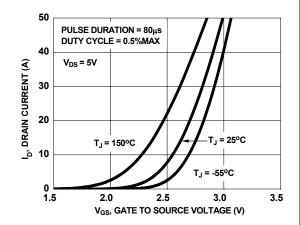


Figure 4. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

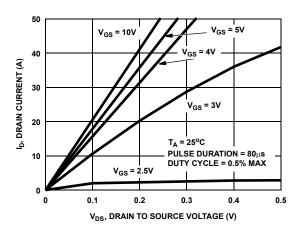




NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 5. Unclamped Inductive Switching Capability

Figure 6. Transfer Characteristics



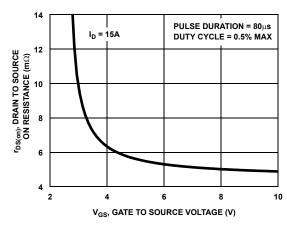
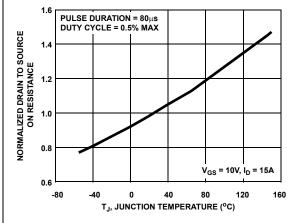


Figure 7. Saturation Characteristics

Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current



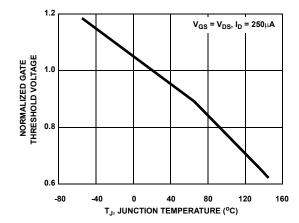


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics T_J = 25°C unless otherwise noted

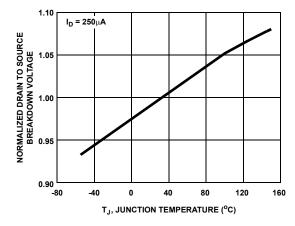


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

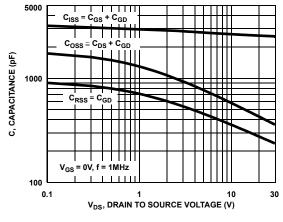


Figure 12. Capacitance vs Drain to Source Voltage

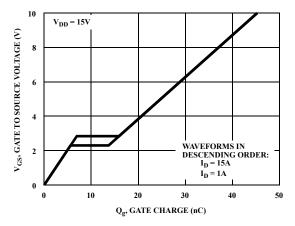


Figure 13. Gate Charge Waveforms for Constant Gate Currents

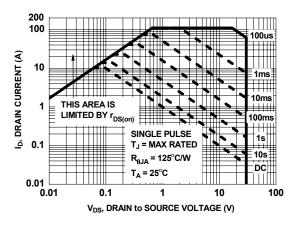


Figure 14. Forward Bias Safe Operating Area

Test Circuits and Waveforms

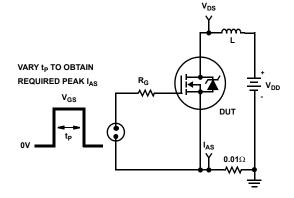


Figure 15. Unclamped Energy Test Circuit

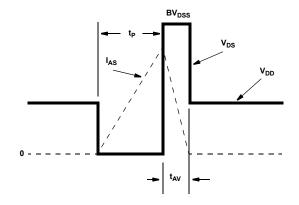


Figure 16. Unclamped Energy Waveforms

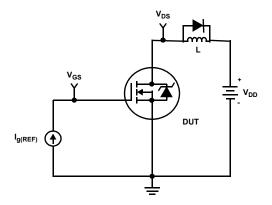


Figure 17. Gate Charge Test Circuit

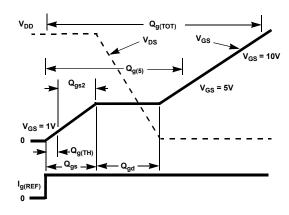


Figure 18. Gate Charge Waveforms

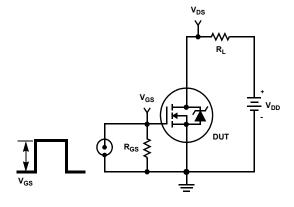


Figure 19. Switching Time Test Circuit

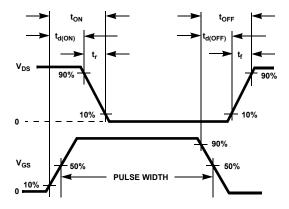


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}}$$
 (EQ. 1)

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

ON Semiconductor provides thermal information to assist the design-er's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (compo-nent side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary in-formation for calculation of the steady state junction temper-ature or power dissipation. Pulse applications can be evaluated using the ON Semiconductor device Spice thermal model or manually utilizing the normalized maximum transient

thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{0.23 + Area}$$
 (EQ. 2)

The transient thermal impedance $(Z_{\theta JA})$ is also effected by varied top copper board area. Figure 22 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

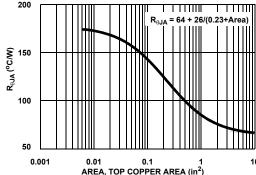


Figure 21. Thermal Resistance vs Mounting
Pad Area

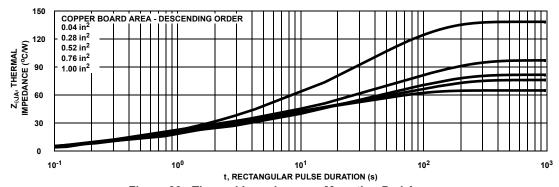


Figure 22. Thermal Impedance vs Mounting Pad Area

PSPICE Electrical Model .SUBCKT FDS8896 2 1 3; rev February 2004 Ca 12 8 1.8e-9 Cb 15 14 1.8e-9 Cin 6 8 2.2e-9 Dbody 7 5 DbodyMOD Dbreak 5 11 DbreakMOD LDRAIN DPLCAP DRAIN Dplcap 10 5 DplcapMOD 10 Ebreak 11 7 17 18 33.1 RLDRAIN ERSLC1 Eds 14 8 5 8 1 DBREAK Y Egs 13 8 6 8 1 RSLC2 Esa 6 10 6 8 1 **ESLC** 11 Evthres 6 21 19 8 1 Evtemp 20 6 18 22 1 50 ≶rdrain **DBODY EBREAK** ESG It 8 17 1 **EVTHRES** MWEAK Lgate 1 9 1.5e-9 **EVTEMP** LGATE Ldrain 2 5 1.0e-9 **RGATE** ■MMED Lsource 3 7 1e-9 RLGATE RLgate 1 9 15 LSOURCE CIN SOURCE RLdrain 2 5 10 RLsource 3 7 10 RSOURCE RLSOURCE Mmed 16 6 8 8 MmedMOD **RBREAK** Mstro 16 6 8 8 MstroMOD <u>13</u> 8 <u>14</u> 13 17 Mweak 16 21 8 8 MweakMOD S1B **RVTEMP** Rbreak 17 18 RbreakMOD 1 СВ 19 CA Rdrain 50 16 RdrainMOD 2.52e-3 IT 14 Rgate 9 20 2.4 VRAT FGS FDS RŠLC1 5 51 RSLCMOD 1e-6 RSLC2 5 50 1e3 Rsource 8 7 RsourceMOD 2e-3 **RVTHRES** Rvthres 22 8 RvthresMOD 1 Rvtemp 18 19 RvtempMOD 1 S1a 6 12 13 8 S1AMOD S1b 13 12 13 8 S1BMOD S2a 6 15 14 13 S2AMOD S2b 13 15 14 13 S2BMOD Vbat 22 19 DC 1 ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*500),10))} .MODEL DbodyMOD D (IS=4E-12 IKF=10 N=1.01 RS=2.6e-3 TRS1=8e-4 TRS2=2e-7 + CJO=8.8e-10 M=0.57 TT=1e-12 XTI=2.2) .MODEL DbreakMOD D (RS=8e-2 TRS1=1e-3 TRS2=-8.9e-6) .MODEL DplcapMOD D (CJO=9e-10 IS=1e-30 N=10 M=0.39) .MODEL MmedMOD NMOS (VTO=1.98 KP=10 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.4) .MODEL MstroMOD NMOS (VTO=2.4 KP=350 IS=1e-30 N=10 TOX=1 L=1u W=1u) .MODEL MweakMOD NMOS (VTO=1.63 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=24 RS=0.1) .MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-1e-6) .MODEL RdrainMOD RES (TC1=1e-4 TC2=8e-6) .MODEL RSLCMOD RES (TC1=9e-4 TC2=1e-6) .MODEL RsourceMOD RES (TC1=7e-3 TC2=1e-6) .MODEL RvthresMOD RES (TC1=-1.3e-3 TC2=-7e-6) .MODEL RytempMOD RES (TC1=-2.6e-3 TC2=2e-7) .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3) .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3 VOFF=-4) .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-0.5) .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-2) .ENDS Note: For further discussion of the PSPICE model, consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model REV February 2004 template FDS8896 n2,n1,n3 electrical n2,n1,n3 var i iscl dp..model dbodymod = (isl=4e-12,ikf=10,nl=1.01,rs=2.6e-3,trs1=8e-4,trs2=2e-7,cjo=8.8e-10,m=0.57,tt=1e-12,xti=2.2) dp..model dbreakmod = (rs=8e-2.trs1=1e-3.trs2=-8.9e-6) dp..model dplcapmod = (cjo=9e-10,isl=10e-30,nl=10,m=0.39) $m..model mmedmod = (type=_n,vto=1.98,kp=10,is=1e-30,tox=1)$ m..model mstrongmod = (type=_n,vto=2.4,kp=350,is=1e-30, tox=1) m..model mweakmod = $(type=_n, vto=1.63, kp=0.05, is=1e-30, tox=1, rs=0.1)$ sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-3) LDRAIN sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3,voff=-4) DPLCAP DRAIN sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2,voff=-0.5) 10 sw vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2) RLDRAIN FRSLC1 $c.\bar{ca}$ n12 n8 = 1.8e-9 c.cb n15 n14 = 1.8e-9 51 RSLC2 ₹ c.cin n6 n8 = 2.2e-9Ŧ ISCL dp.dbody n7 n5 = model=dbodymod 50 DBREAK _ dp.dbreak n5 n11 = model=dbreakmod ≨rdrain 8 dp.dplcap n10 n5 = model=dplcapmod **ESG** DBODY **EVTHRES** spe.ebreak n11 n7 n17 n18 = 33.1 19 8 MWEAK **LGATE EVTEMP** spe.eds n14 n8 n5 n8 = 1 **RGATE EBREAK** spe.eqs n13 n8 n6 n8 = 1 20 ■MSTRO spe.esg n6 n10 n6 n8 = 1 RLGATE spe.evthres n6 n21 n19 n8 = 1 LSOURCE CIN SOURCE spe.evtemp n20 n6 n18 n22 = 1 Q RSOURCE i.it n8 n17 = 1 RLSOURCE I.lgate n1 n9 = 1.5e-9 RBREAK 14 13 I.ldrain n2 n5 = 1.0e-9 17 I.Isource n3 n7 = 1e-9 RVTEMP СВ 19 res.rlgate n1 n9 = 15 CA IT res.rldrain n2 n5 = 10 VBAT res.rlsource n3 n7 = 10 EGS **EDS** m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u **RVTHRES** m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u res.rbreak n17 n18 = 1, tc1=8.3e-4,tc2=-1e-6 res.rdrain n50 n16 = 2.52e-3, tc1=1e-4,tc2=8e-6 res.rgate n9 n20 = 2.4 res.rslc1 n5 n51 = 1e-6, tc1=9e-4,tc2=1e-6 res.rslc2 n5 n50 = 1e3 res.rsource n8 n7 = 2e-3, tc1=7e-3,tc2=1e-6 res.rvthres n22 n8 = 1, tc1=-1.3e-3,tc2=-7e-6 res.rvtemp n18 n19 = 1, tc1=-2.6e-3,tc2=2e-7 sw vcsp.s1a n6 n12 n13 n8 = model=s1amod sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod v.vbat n22 n19 = dc=1 equations { i (n51->n50) +=iscl |sc| = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/500))** 10))

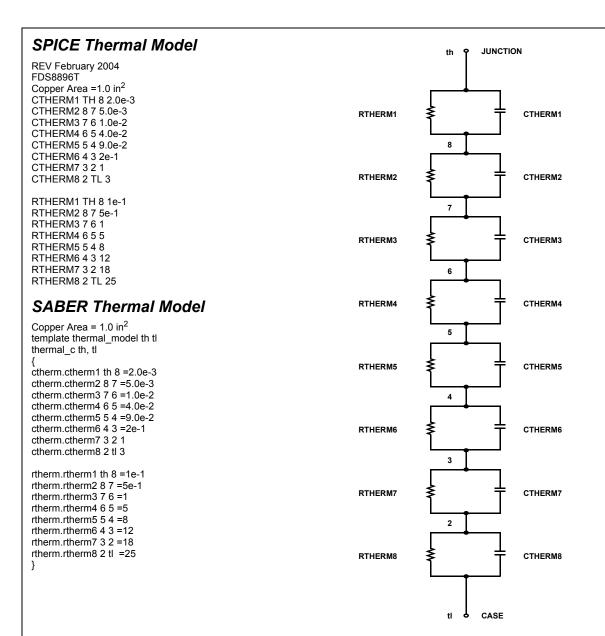


TABLE 1. THERMAL MODELS

COMPONANT	0.04 in ²	0.28 in ²	0.52 in ²	0.76 in ²	1.0 in ²
CTHERM6	1.2e-1	1.5e-1	2.0e-1	2.0e-1	2.0e-1
CTHERM7	0.5	1.0	1.0	1.0	1.0
CTHERM8	1.3	2.8	3.0	3.0	3.0
RTHERM6	26	20	15	13	12
RTHERM7	39	24	21	19	18
RTHERM8	55	38.7	31.3	29.7	25

ON Semiconductor and III) are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages.

Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative