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FDS4675-F085 40V P-Channel PowerTrench® MOSFET

General Description

This P-Channel MOSFET is a rugged gate version of ON Semiconductor's advanced Power Tranch process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5 V - 20 V).

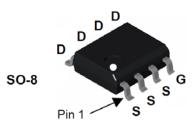
Applications

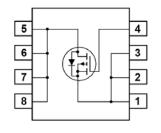
- Powermanagement
- Load switch
- Battery protection



Features

- -11 A, -40 V $R_{DS(ON)} = 0.013 \Omega$ @ $V_{GS} = -10 \text{ V}$ $R_{DS(ON)} = 0.017 \Omega$ @ $V_{GS} = -4.5 \text{ V}$
- Fast switching speed
- High performance trench technology for extremely low RDS/ONI
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units	
V_{DSS}	Drain-Source Voltage		-40	V	
V _{GSS}	Gate-Source Voltage		±20	V	
	Drain Current	Continuous	-11 ^(Note 1a)	Α	
I _D		Pulsed	-50	А	
	Power Dissipation for Single Operation		2.4 (steady state) (Note 1a)	W	
P_D			1.4 (Note 1b)	W	
			1.2 ^(Note 1c)	W	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C	

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5 (steady state), 50 (10 sec) (Note 1a)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 ^(Note 1c)	°C/W
R _{BJC} Thermal Resistance, Junction to Case		25 ^(Note 1)	°C/W

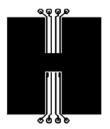
Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4675	FDS4675-F085	13"	12mm	2500 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Characteristic	cs			•	•	•
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-40			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, Referenced to 25°C		-34		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -32 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-1.4	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = -250μA, Referenced to 25°C		4.6		mV/°C
		V _{GS} = -10 V, I _D = -11 A		10	13	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -9.5 \text{ A}$		13	17	mΩ
		V _{GS} = -10 V, I _D = -11 A, T _J = 125°C		15	21	
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -11 A		44		S
Dynamic Charact	eristics					
C _{ISS}	Input Capacitance			4350		pF
Coss	Output Capacitance	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		622		pF
C _{RSS}	Reverse Transfer Capacitance			290		pF
Switching Charac	cteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time			40	64	ns
t _r	Tum-On Rise Time	$V_{DD} = -20 \text{ V}, I_D = -1 \text{ A}$		49	79	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		100	160	ns
t _f	Turn-Off Fall Time			60	96	ns
Qg	Total Gate Charge			40	56	nC
Q_gs	Gate-Source Charge	$V_{DS} = -20 \text{ V}, I_{D} = -11 \text{ A}, V_{GS} = -4.5 \text{ V}$		11		nC
Q_{gd}	Gate-Drain Charge			13		nC
Drain-Source Dio	de Characteristics and Maximum Ra	tings				
Is	Maximum Continuous Drain-Source	Diode Forward Current			-2.1	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ A}, I_S = -2.1 \text{ A}^{\text{(Note 2)}}$		-0.7	-1.2	V

 R_{BLA} is the sum of the junction to case and case to ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a) 50°C/W when mounted on a 1in2 pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

Pulse Test: Pulse Width < 300 $\mu s,$ Duty Cycle < 2.0%

Typical Characteristics

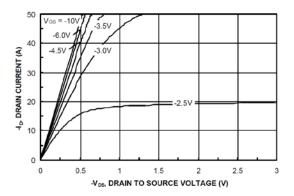


Figure 1. On-Region Characteristics

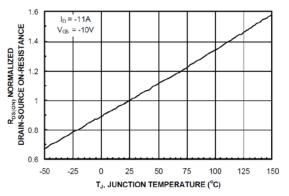


Figure 3. On-Resistance Variation with Temperature

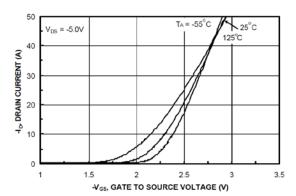


Figure 5. Transfer Characteristics

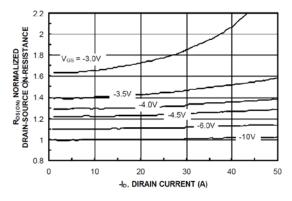


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

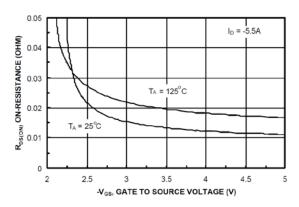


Figure 4. On-Resistance Variation with Gate to Source Voltage

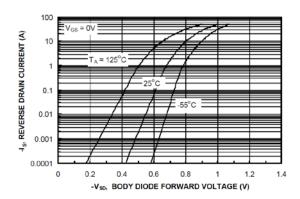


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

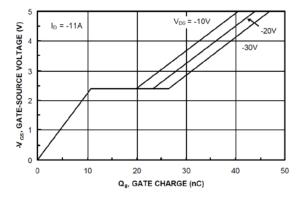


Figure 7. Gate Charge Characteristics

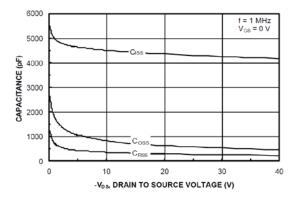


Figure 8. Capacitance Characteristics

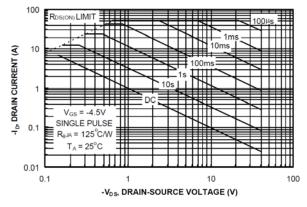


Figure 9. Maximum Safe Operating Area

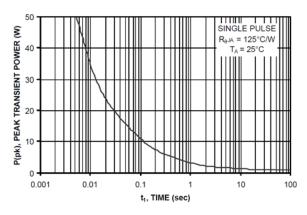


Figure 10. Single Pulse Maximum Power Dissipation

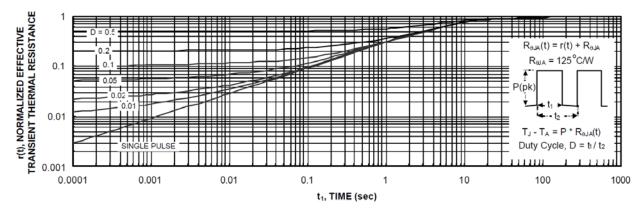


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

Physical Dimension

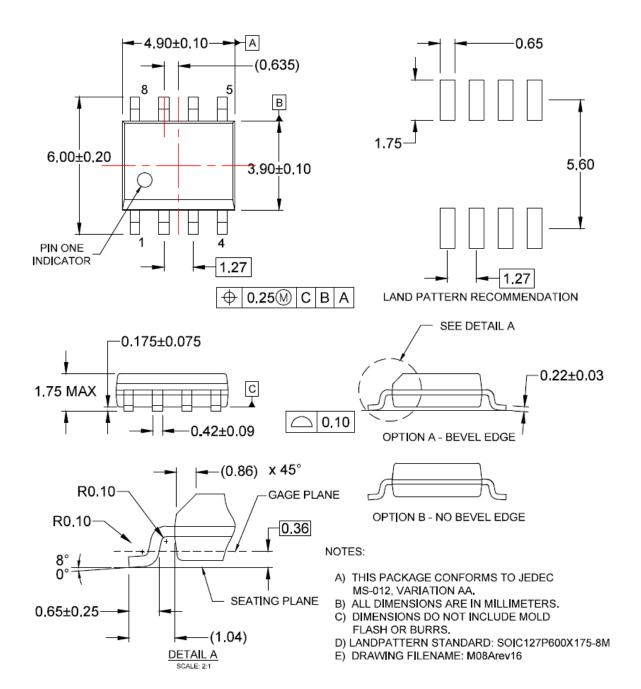


Figure 12. 8LD, SOIC, JEDEC MS-012, .150" NARROW BODY

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