

MOSFET – Dual, N-Channel, POWER TRENCH[®], 80 V

FDS3890

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC-DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC-DC power supply designs with higher overall efficiency.

Features

- 4.7 A, 80 V:
 - ◆ $R_{DS(ON)} = 44 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 - ◆ $R_{DS(ON)} = 50 \text{ m}\Omega @ V_{GS} = 6 \text{ V}$
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability
- Pb-Free and Halide Free

ABSOLUTE MAXIMUM RATINGS

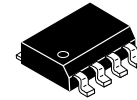
($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-Source Voltage	80	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current Continuous (Note 1a) Pulsed	4.7 20	A
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1.0	
	(Note 1c)	0.9	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to $+175$	$^\circ\text{C}$

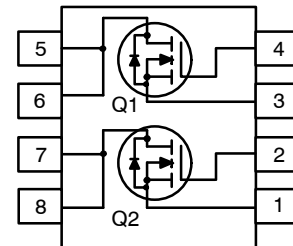
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

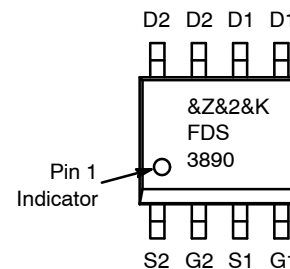
Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$



SOIC8
CASE 751EB



MARKING DIAGRAM



&Z = Assembly Plant Code
 &2 = Date Code (Year & Week)
 &K = Lot Traceability Code
 FDS3890 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDS3890	SOIC8 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDS3890

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATINGS (Note 2)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 40\text{ V}$, $I_D = 4.7\text{ A}$	–	–	175	mJ
I_{AR}	Maximum Drain-Source Avalanche Current		–	–	4.7	A

OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	80	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	86	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{ V}$, $V_{GS} = 0\text{ V}$	–	–	1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	-100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	2.3	4	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	-6	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.7\text{ A}$ $V_{GS} = 6\text{ V}$, $I_D = 4.4\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 4.7\text{ A}$, $T_J = 125^\circ\text{C}$	–	34 37 60	44 50 82	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 5\text{ V}$	20	–	–	A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 4.7\text{ A}$	–	24	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	–	1180	–	pF
C_{oss}	Output Capacitance		–	171	–	pF
C_{rss}	Reverse Transfer Capacitance		–	50	–	pF

SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$	–	11	20	ns
t_r	Turn-On Rise Time		–	8	16	ns
$t_{d(off)}$	Turn-Off Delay Time		–	26	50	ns
t_f	Turn-Off Fall Time		–	12	25	ns
Q_g	Total Gate Charge	$V_{DS} = 40\text{ V}$, $I_D = 4.7\text{ A}$, $V_{GS} = 10\text{ V}$	–	25	35	nC
Q_{gs}	Gate-Source Charge		–	4.5	–	nC
Q_{gd}	Gate-Drain Charge		–	5.8	–	nC

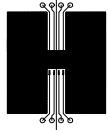
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	1.3	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)	–	0.74	1.2	V

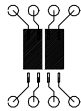
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

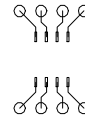
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 1 in^2 pad of 2 oz. copper.



b) 125°C/W when mounted on a 0.04 in^2 pad of 2 oz. copper.



c) 135°C/W when mounted on a minimum pad.

- Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

TYPICAL CHARACTERISTICS

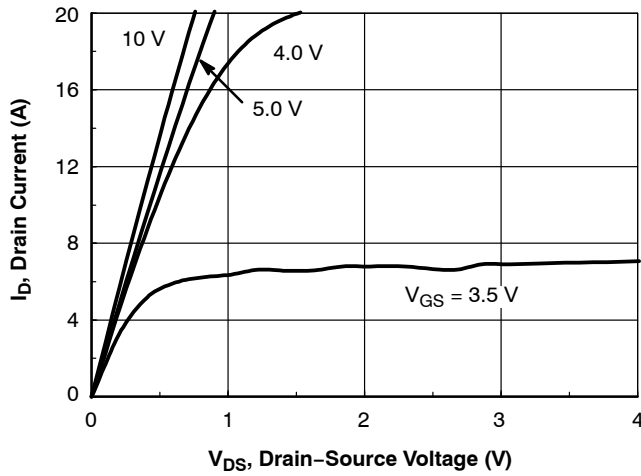


Figure 1. On-Region Characteristic

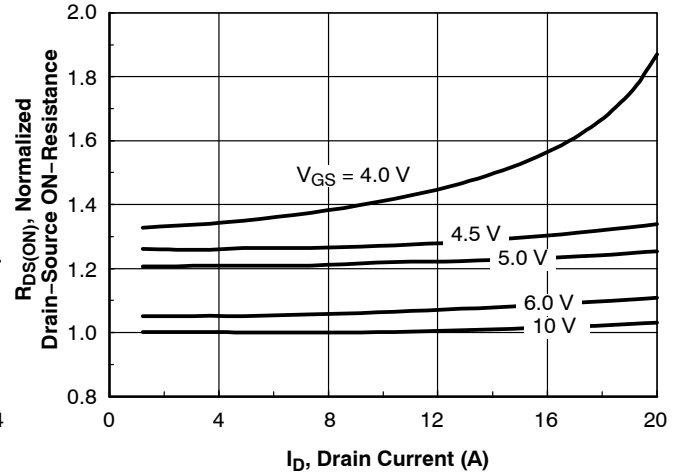


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

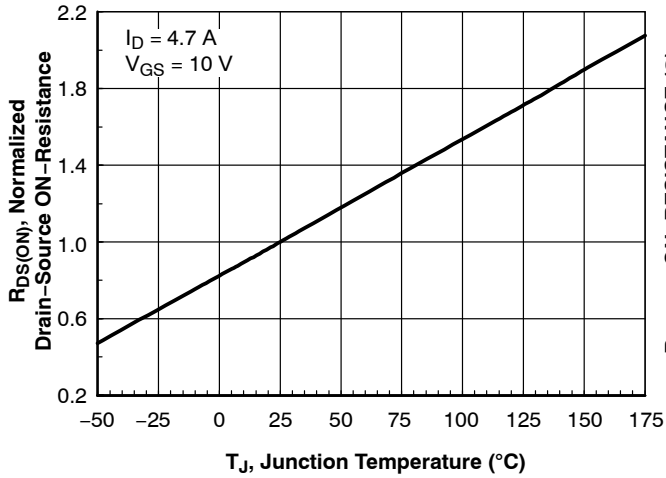


Figure 3. On-Resistance Variation with Temperature

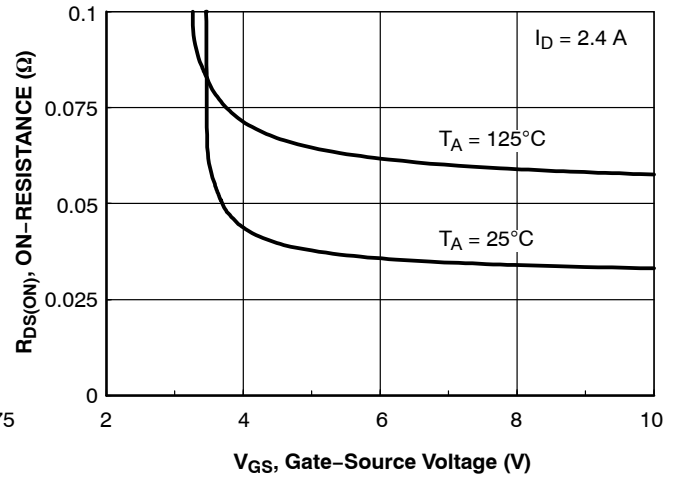


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

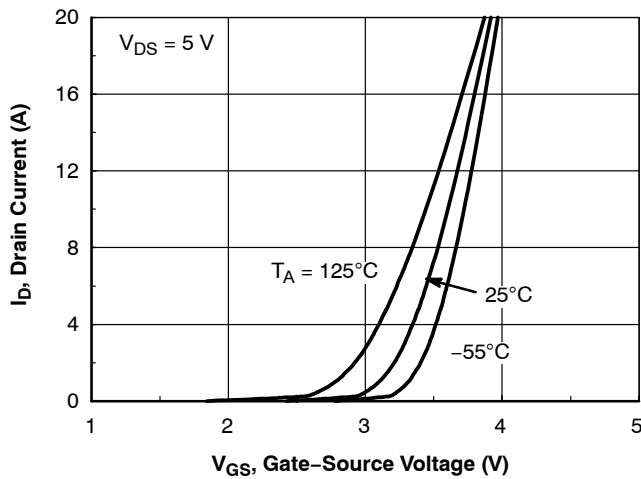


Figure 5. Transfer Characteristics

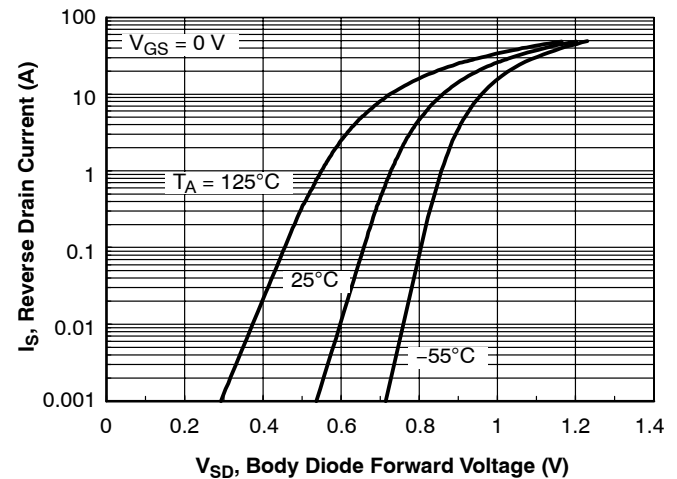


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (Continued)

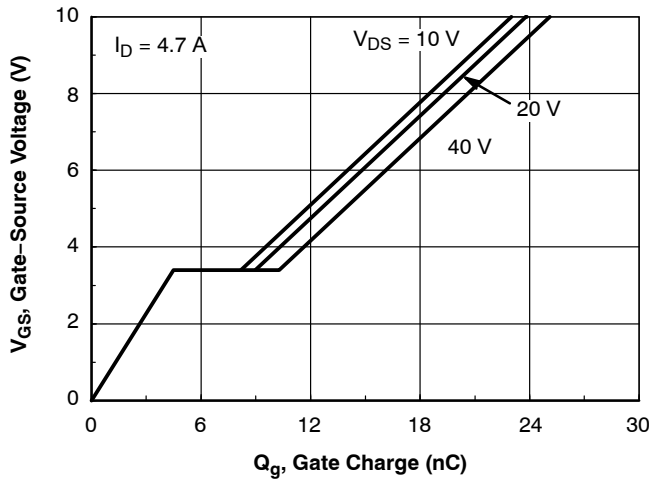


Figure 7. Gate-Charge Characteristics

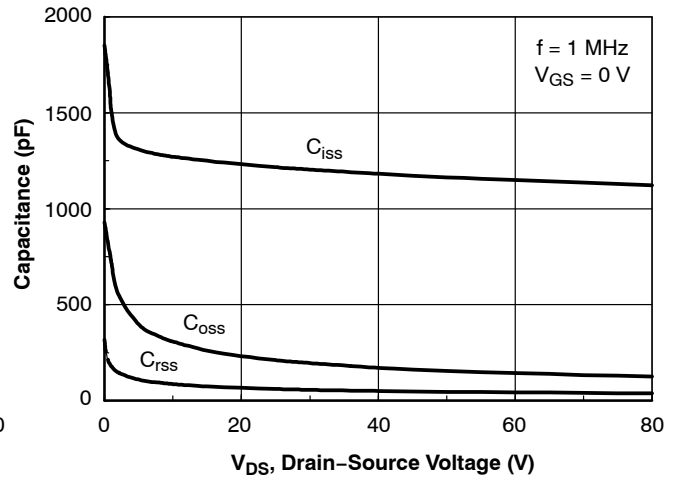


Figure 8. Capacitance Characteristics

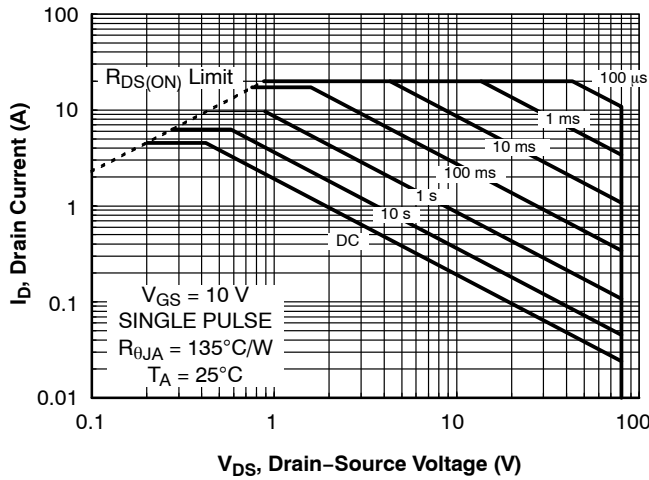


Figure 9. Maximum Safe Operating Area

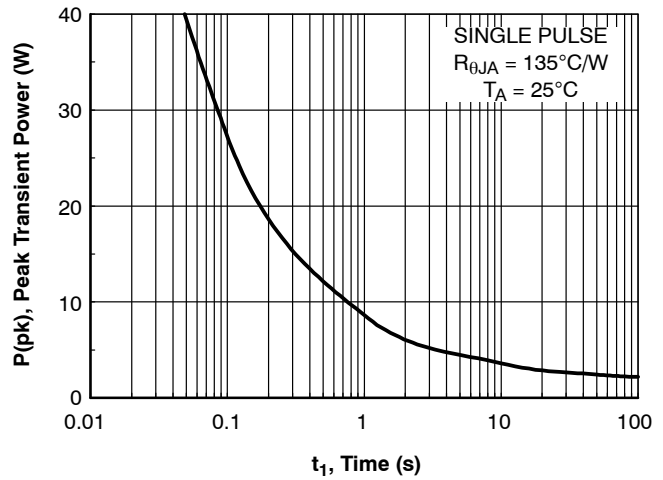


Figure 10. Single Pulse Maximum Power Dissipation

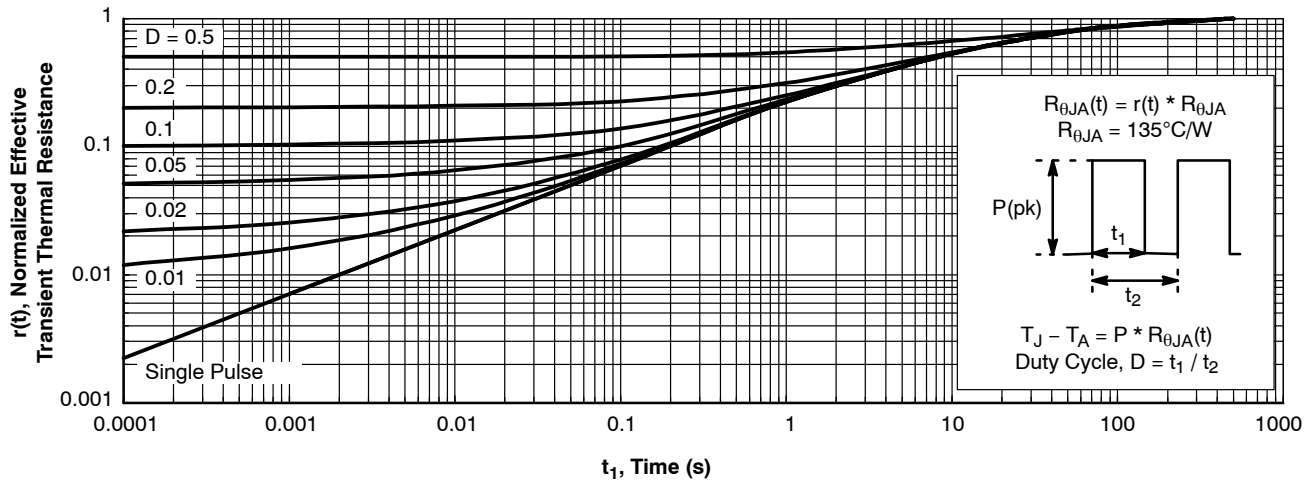
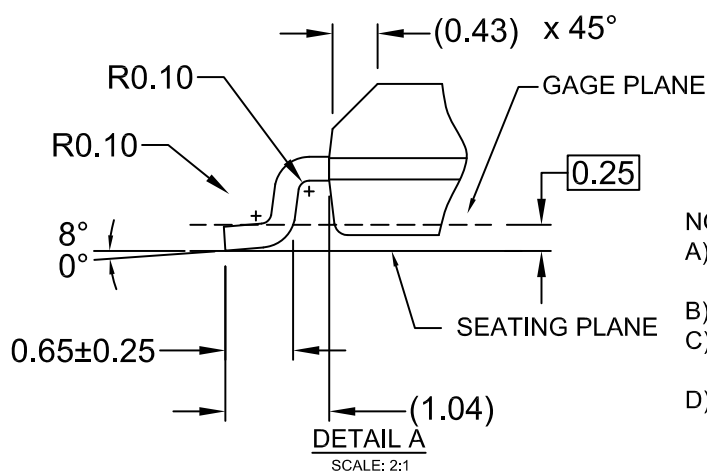
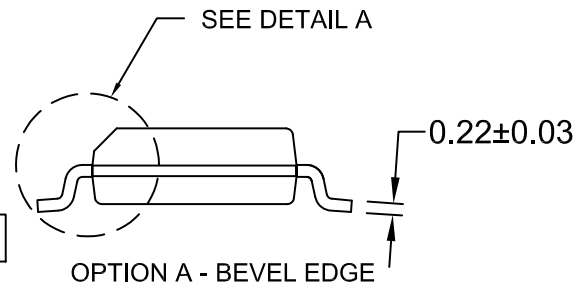
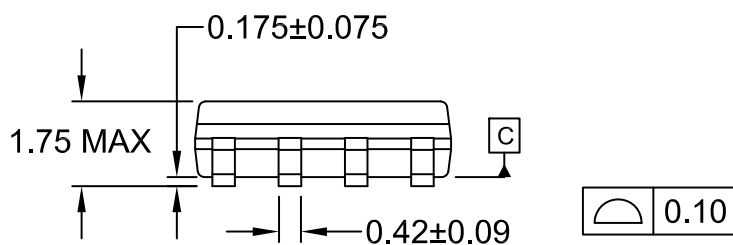
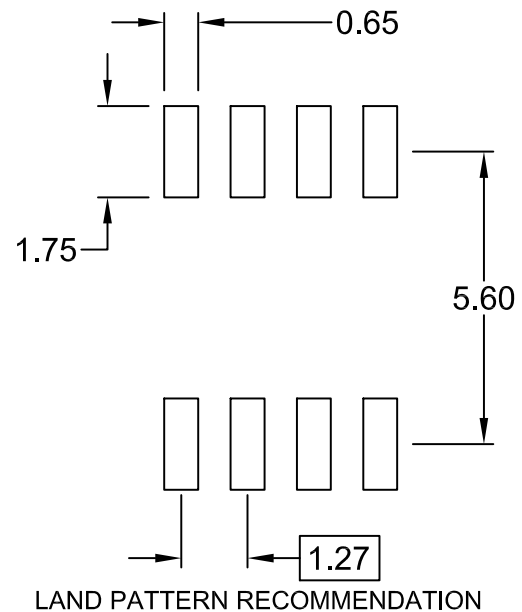
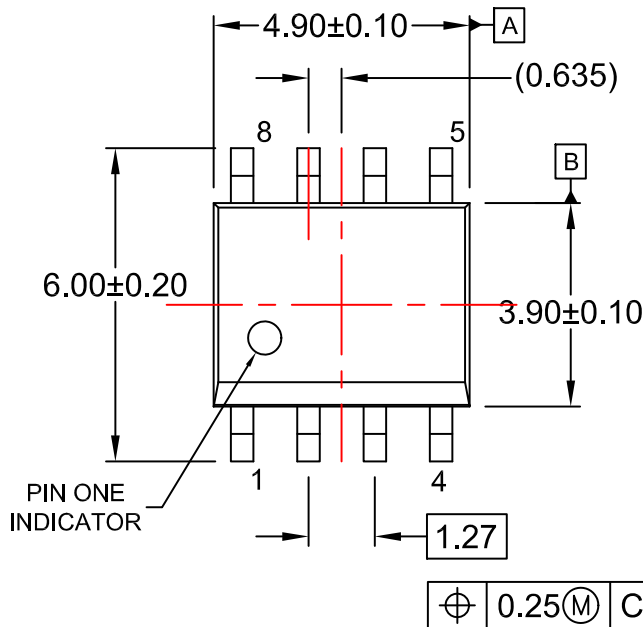


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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CASE 751EB
ISSUE A

DATE 24 AUG 2017



- NOTES:
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
 - D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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