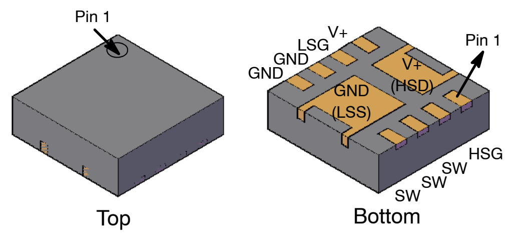
# MOSFET – Dual, N-Channel, Asymmetric, POWERTRENCH®, Power Clip, 25 V

# FDPC8011S




**PQFN8 3.3X3.3, 0.65P**
**CASE 483AZ**

### General Description

This device includes two specialized N−Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

### Features

Q1: N−Channel

- Max $R_{DS(on)}$ = 7.3 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 12 A

Q2: N−Channel

- Max $R_{DS(on)}$ = 2.1 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 24 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- RoHS Compliant

### Applications

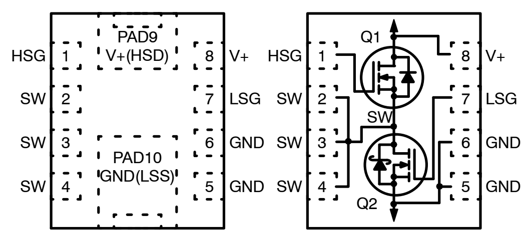
- Computing
- Communications
- General Purpose Point of Load

### MARKING DIAGRAM

&Z&3&K
13OD
15OD

| | |
|---|---|
| &Z | = Assembly Plant Code |
| &3 | = 3−Digit Date Code |
| &K | = 2−Digits Lot Run Traceability Code |
| 13OD15OD | = Device Code |

### PIN ASSIGNMENT




### ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

**MOSFET MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | | Q1 | Q2 | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 25 | 25 | V |
| $V_{GS}$ | Gate to Source Voltage | | 12 | 12 | V |
| $I_D$ | Drain Current | – Continuous $T_C$ = 25°C | 20 | 60 | A |
| | | – Continuous $T_A$ = 25°C | 13 (Note 1a) | 27 (Note 1b) | |
| | | – Pulsed | 40 | 120 | |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | | 21 | 97 | mJ |
| $P_D$ | Power Dissipation for Single Operation | $T_A$ = 25°C | 1.6 (Note 1a) | 2.0 (Note 1b) | W |
| | | $T_A$ = 25°C | 0.8 (Note 1c) | 0.9 (Note 1d) | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS**

| Symbol | Characteristic | Value | Value | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 77 (Note 1a) | 63 (Note 1b) | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 151 (Note 1c) | 135 (Note 1d) | |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 5.0 | 3.5 | |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

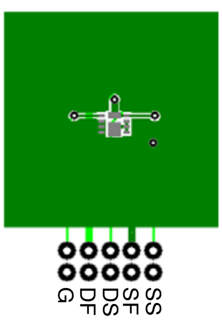
| Symbol | Parameter | Test Condition | Type | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V<br>$I_D$ = 1 mA, $V_{GS}$ = 0 V | Q1<br>Q2 | 25<br>25 | –<br>– | –<br>– | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C<br>$I_D$ = 10 mA, referenced to 25°C | Q1<br>Q2 | –<br>– | 14<br>24 | –<br>– | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = 20 V, $V_{GS}$ = 0 V | Q1<br>Q2 | –<br>– | –<br>– | 1<br>500 | μA<br>μA |
| $I_{GSS}$ | Gate to Source Leakage Current, Forward | $V_{GS}$ = 12 V/–8 V, $V_{DS}$ = 0 V<br>$V_{GS}$ = 12 V/–8 V, $V_{DS}$ = 0 V | Q1<br>Q2 | –<br>– | –<br>– | ±100<br>±100 | nA<br>nA |
| **ON CHARACTERISTICS** | | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA<br>$V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA | Q1<br>Q2 | 0.8<br>1.1 | 1.2<br>1.4 | 2.2<br>2.2 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C<br>$I_D$ = 10 mA, referenced to 25°C | Q1<br>Q2 | –<br>– | –4<br>–3 | –<br>– | mV/°C |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 13 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 12 A<br>$V_{GS}$ = 10 V, $I_D$ = 13 A, $T_J$ = 125°C | Q1 | –<br>–<br>– | 4.6<br>5.4<br>5.6 | 6.0<br>7.3<br>7.3 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 27 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 24 A<br>$V_{GS}$ = 10 V, $I_D$ = 27 A, $T_J$ = 125°C | Q2 | –<br>–<br>– | 1.2<br>1.4<br>1.7 | 1.8<br>2.1<br>2.4 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 13 A<br>$V_{DS}$ = 5 V, $I_D$ = 27 A | Q1<br>Q2 | –<br>– | 97<br>231 | –<br>– | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $C_{iss}$ | Input Capacitance | Q1:<br>$V_{DS}$ = 13 V, $V_{GS}$ = 0 V, f = 1 MHz<br>Q2:<br>$V_{DS}$ = 13 V, $V_{GS}$ = 0 V, f = 1 MHz | Q1<br>Q2 | –<br>– | 1240<br>4335 | –<br>– | pF |
| $C_{oss}$ | Output Capacitance | | Q1<br>Q2 | –<br>– | 332<br>1126 | –<br>– | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q1<br>Q2 | –<br>– | 49<br>143 | –<br>– | pF |
| $R_g$ | Gate Resistance | | Q1<br>Q2 | –<br>– | 0.4<br>0.5 | –<br>– | Ω |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (continued)

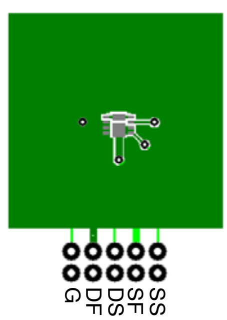
| Symbol | Parameter | Test Condition | Type | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | Q1: $V_{DD}$ = 13 V, $I_D$ = 13 A, $R_{GEN}$ = 6 Ω<br>Q2: $V_{DD}$ = 13 V, $I_D$ = 27 A, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | –<br>– | 7<br>13 | –<br>– | ns |
| $t_r$ | Rise Time | | Q1<br>Q2 | –<br>– | 2<br>5 | –<br>– | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | Q1<br>Q2 | –<br>– | 20<br>38 | –<br>– | ns |
| $t_f$ | Fall Time | | Q1<br>Q2 | –<br>– | 2<br>4 | –<br>– | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; Q1: $V_{DD}$ = 13 V, $I_D$ = 13 A; Q2: $V_{DD}$ = 13 V, $I_D$ = 27 A | Q1<br>Q2 | –<br>– | 19<br>64 | –<br>– | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V; Q1: $V_{DD}$ = 13 V, $I_D$ = 13 A; Q2: $V_{DD}$ = 13 V, $I_D$ = 27 A | Q1<br>Q2 | –<br>– | 9<br>30 | –<br>– | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | Q1: $V_{DD}$ = 13 V, $I_D$ = 13 A; Q2: $V_{DD}$ = 13 V, $I_D$ = 27 A | Q1<br>Q2 | –<br>– | 2.6<br>9.3 | –<br>– | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | Q1<br>Q2 | –<br>– | 2.3<br>7.7 | –<br>– | nC |
| **DRAIN–SOURCE CHARACTERISTICS** | | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 13 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = 27 A (Note 2) | Q1<br>Q2 | –<br>– | 0.8<br>0.8 | 1.2<br>1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | Q1: $I_F$ = 13 A, di/dt = 100 A/μs<br>Q2: $I_F$ = 27 A, di/dt = 300 A/μs | Q1<br>Q2 | –<br>– | 22<br>30 | –<br>– | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | Q1<br>Q2 | –<br>– | 8<br>32 | –<br>– | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.




a. 77°C/W when mounted on a 1 in$^2$ pad of 2 oz copper




b. 63°C/W when mounted on a 1 in$^2$ pad of 2 oz copper


c. 151°C/W when mounted on a minimum pad of 2 oz copper


d. 135°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1: $E_{AS}$ of 21 mJ is based on starting $T_J$ = 25°C; N−ch: L = 1.2 mH, $I_{AS}$ = 6 A, $V_{DD}$ = 23 V, $V_{GS}$ = 10 V. 100% test at L= 0.1 mH, $I_{AS}$ = 14.5 A.
   Q2: $E_{AS}$ of 97 mJ is based on starting $T_J$ = 25°C; N−ch: L = 0.6 mH, $I_{AS}$ = 18 A, $V_{DD}$ = 23 V, $V_{GS}$ = 10 V. 100% test at L= 0.1 mH, $I_{AS}$ = 32.9 A.

## TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) ($T_J$ = 25°C unless otherwise noted)

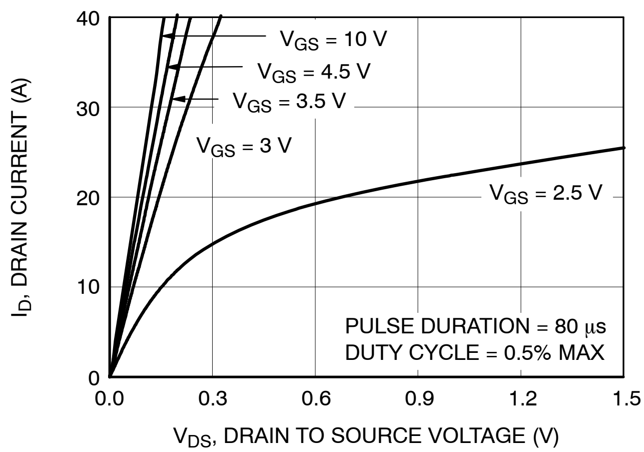



**Figure 1. On−Region Characteristics**

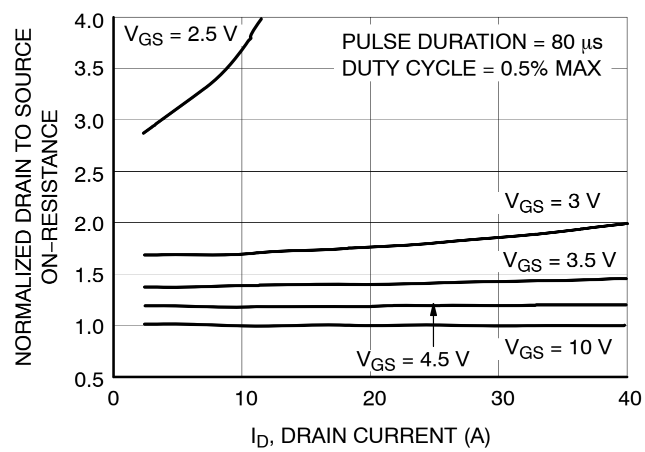



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

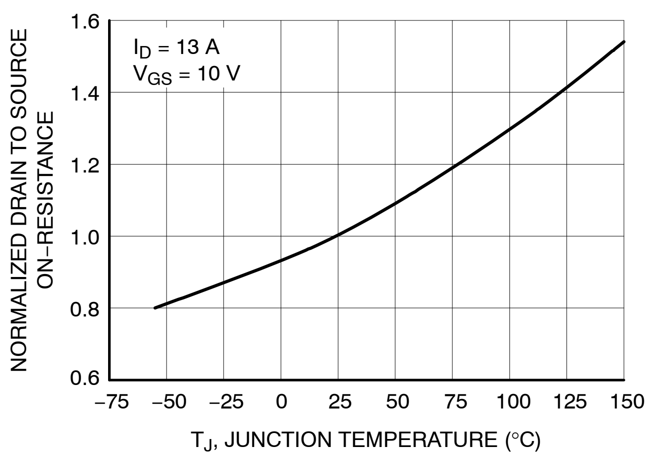



**Figure 3. Normalized On−Resistance vs. Junction Temperature**

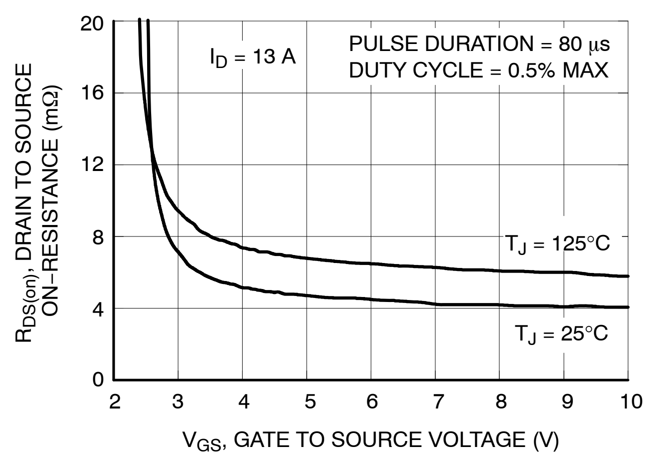



**Figure 4. On−Resistance vs. Gate to Source Voltage**

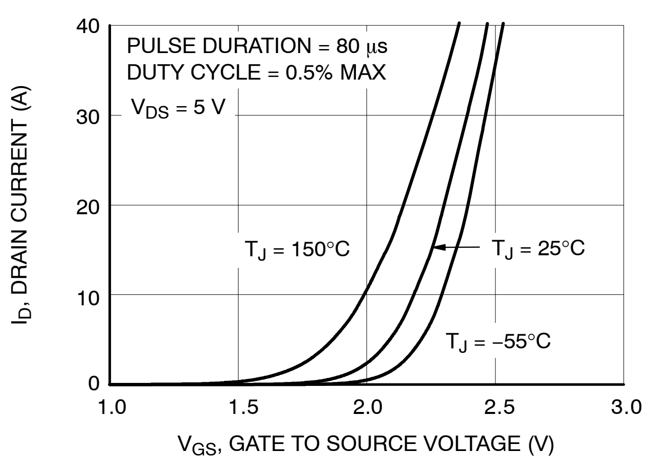



**Figure 5. Transfer Characteristics**

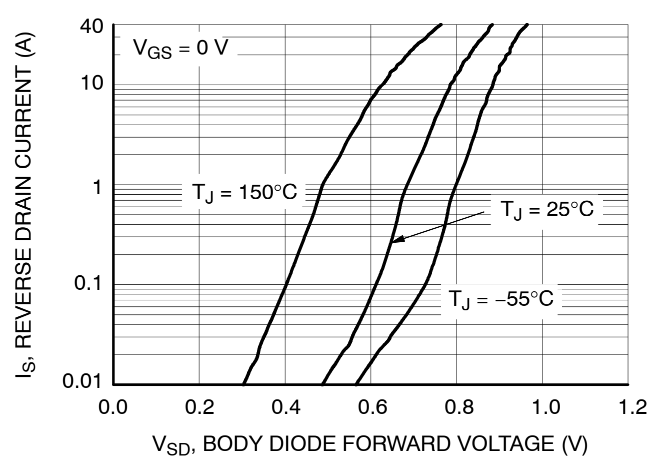



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) ($T_J$ = 25°C unless otherwise noted) (continued)

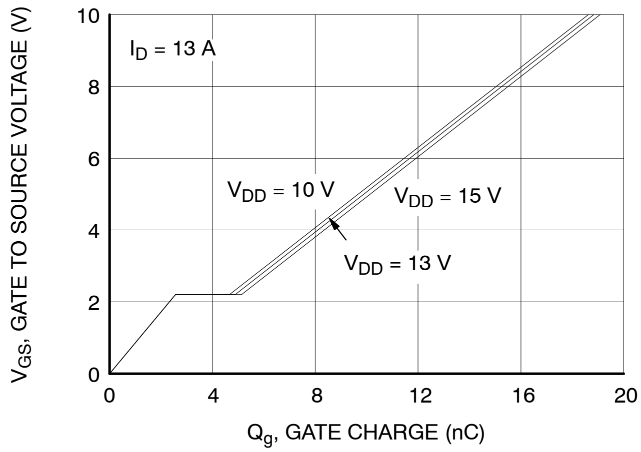



**Figure 7. Gate Charge Characteristics**

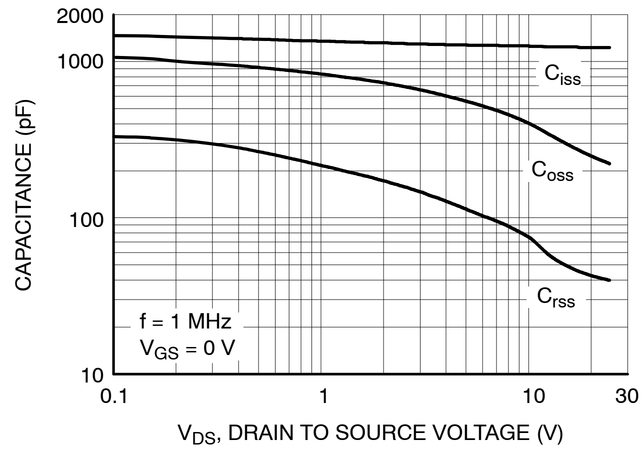



**Figure 8. Capacitance vs. Drain to Source Voltage**

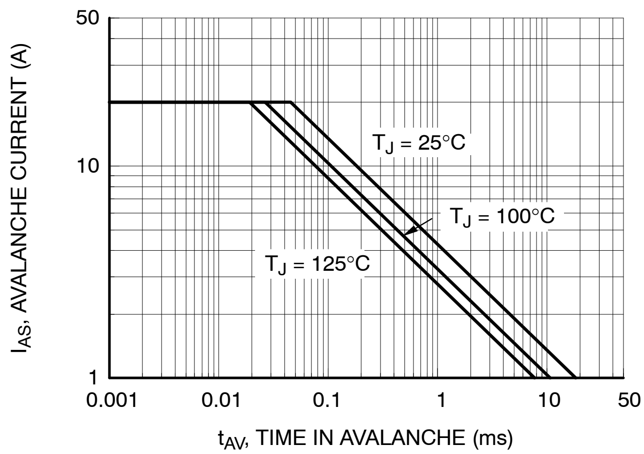



**Figure 9. Unclamped Inductive Switching Capability**

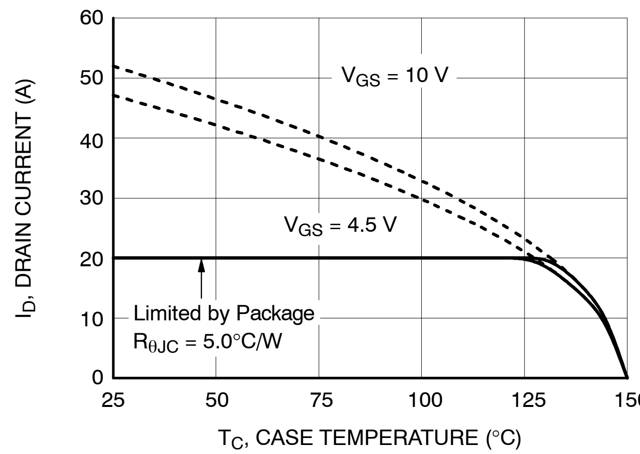



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

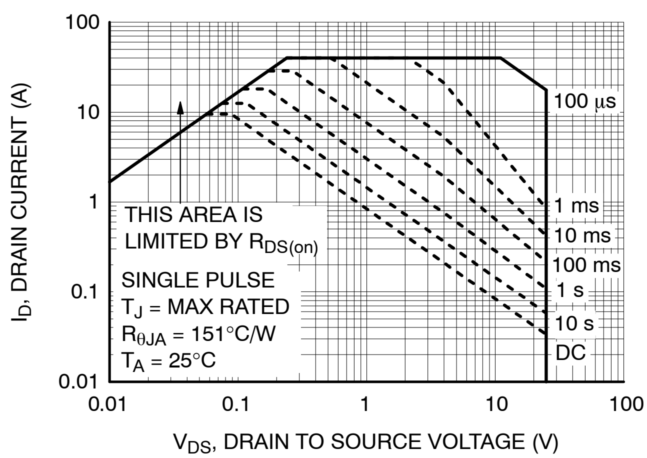



**Figure 11. Forward Bias Safe Operating Area**

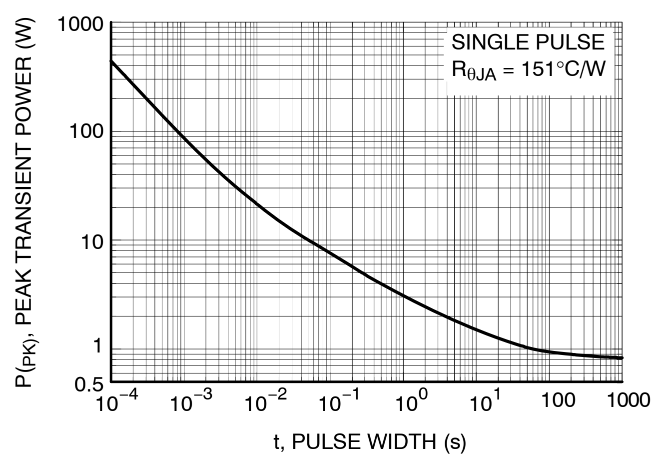



**Figure 12. Single Pulse Maximum Power Dissipation**

**TYPICAL CHARACTERISTICS (Q1 N−CHANNEL)** ($T_J$ = 25°C unless otherwise noted) (continued)

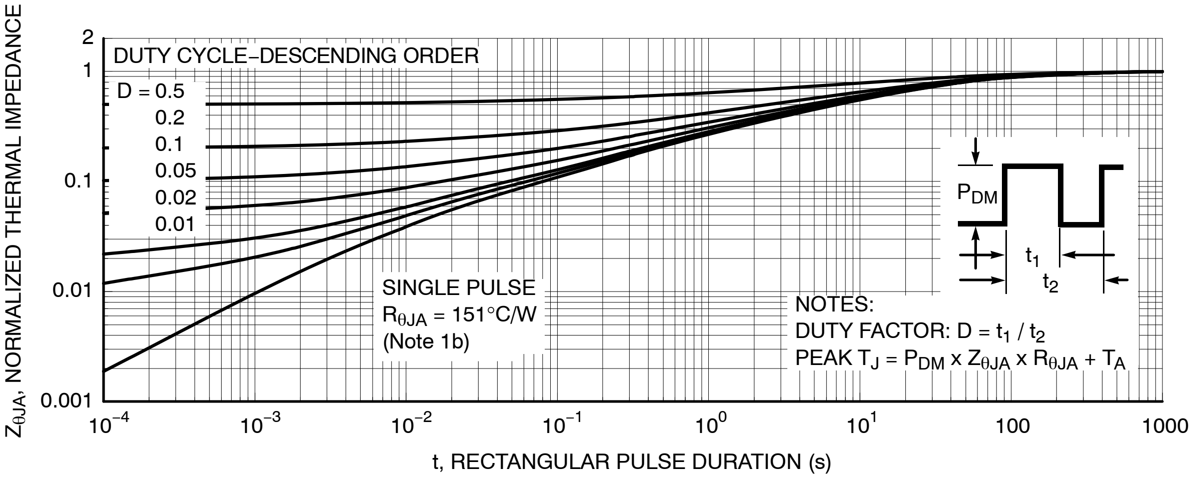



**Figure 13. Junction−to−Ambient Transient Thermal Response Curve**

## TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) ($T_J$ = 25°C unless otherwise noted)

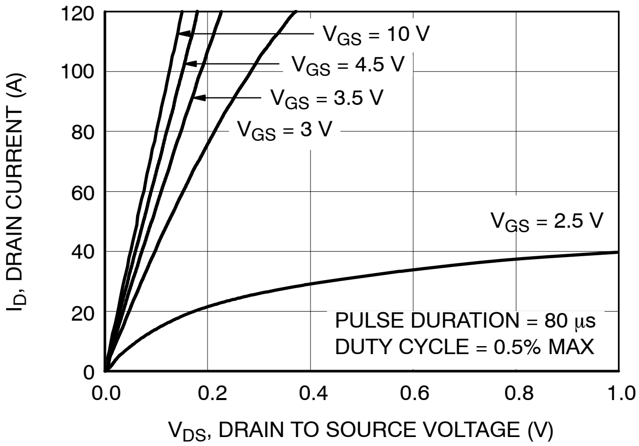



**Figure 14. On−Region Characteristics**

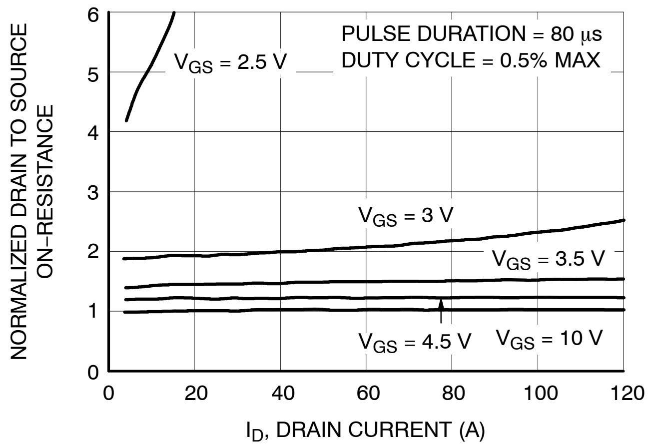



**Figure 15. Normalized On−Resistance vs. Drain Current and Gate Voltage**

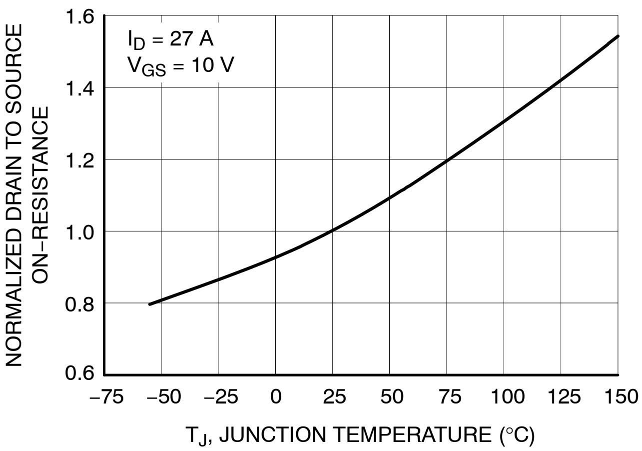



**Figure 16. Normalized On−Resistance vs. Junction Temperature**

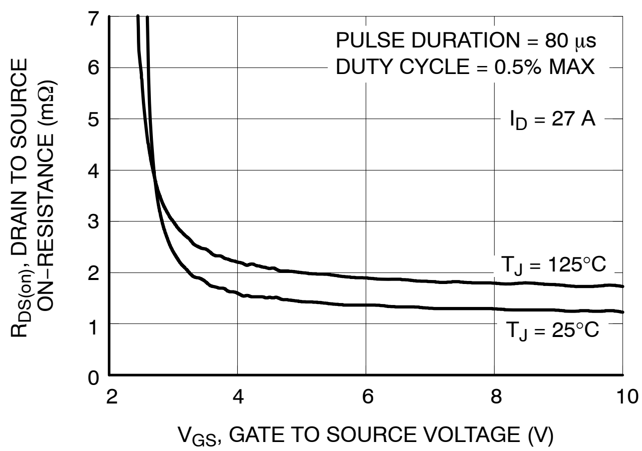



**Figure 17. On−Resistance vs. Gate to Source Voltage**

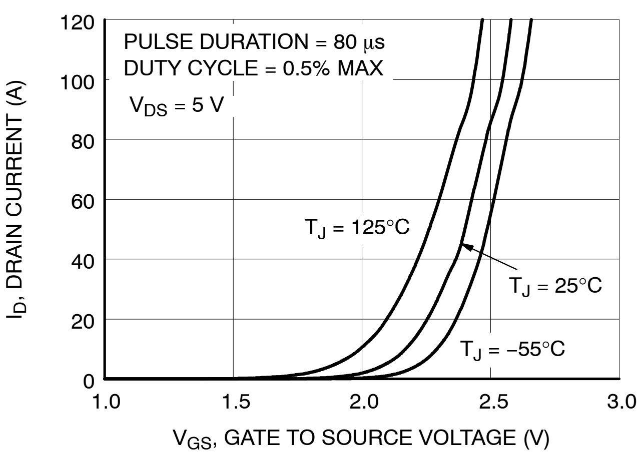



**Figure 18. Transfer Characteristics**

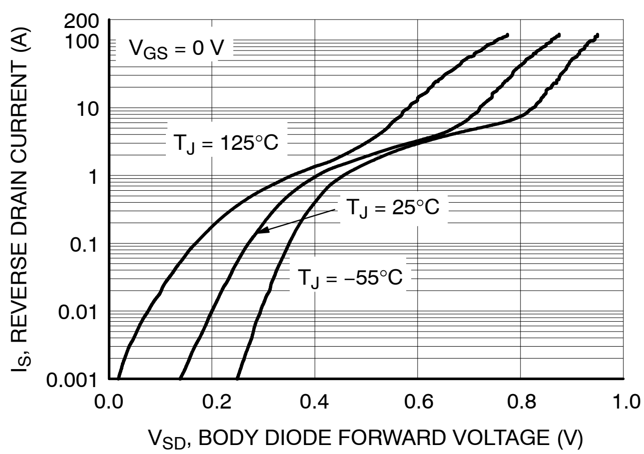



**Figure 19. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) ($T_J$ = 25°C unless otherwise noted) (continued)

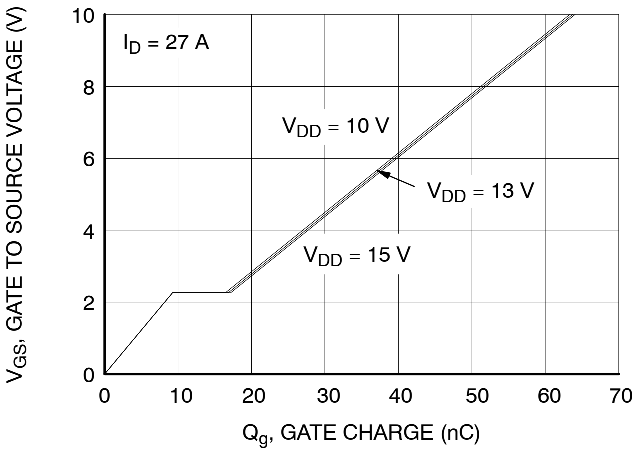



Figure 20. Gate Charge Characteristics

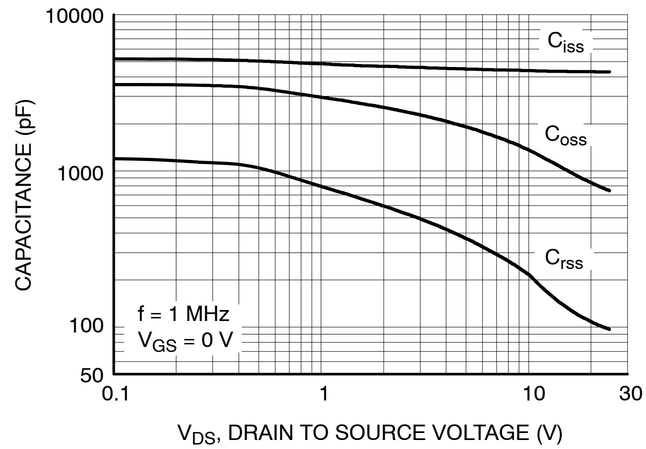



Figure 21. Capacitance vs. Drain to Source Voltage

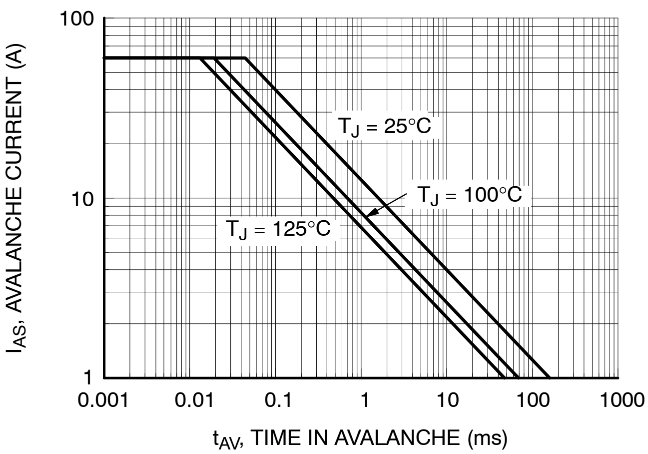



Figure 22. Unclamped Inductive Switching Capability

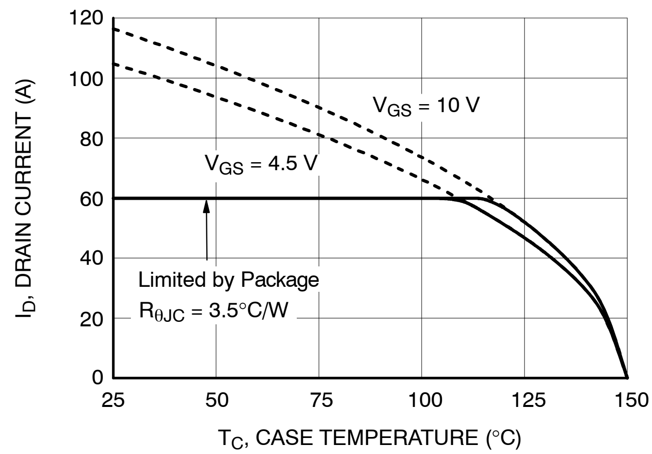



Figure 23. Maximum Continuous Drain Current vs. Case Temperature

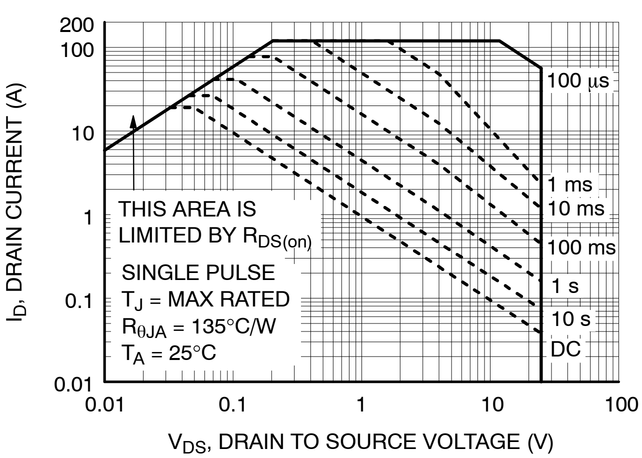



Figure 24. Forward Bias Safe Operating Area

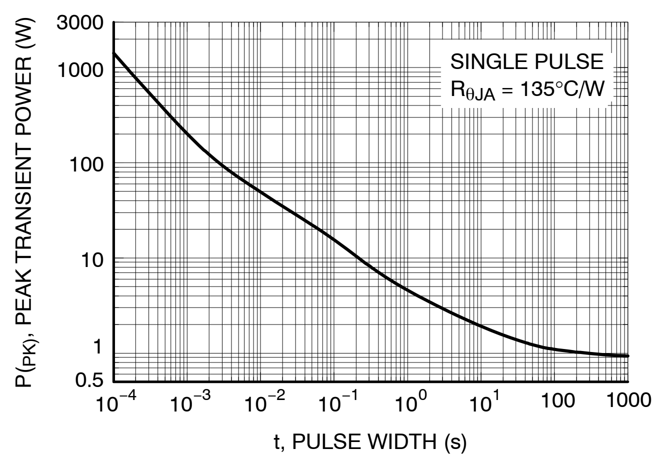



Figure 25. Single Pulse Maximum Power Dissipation

**TYPICAL CHARACTERISTICS (Q2 N−CHANNEL)** ($T_J$ = 25°C unless otherwise noted) (continued)

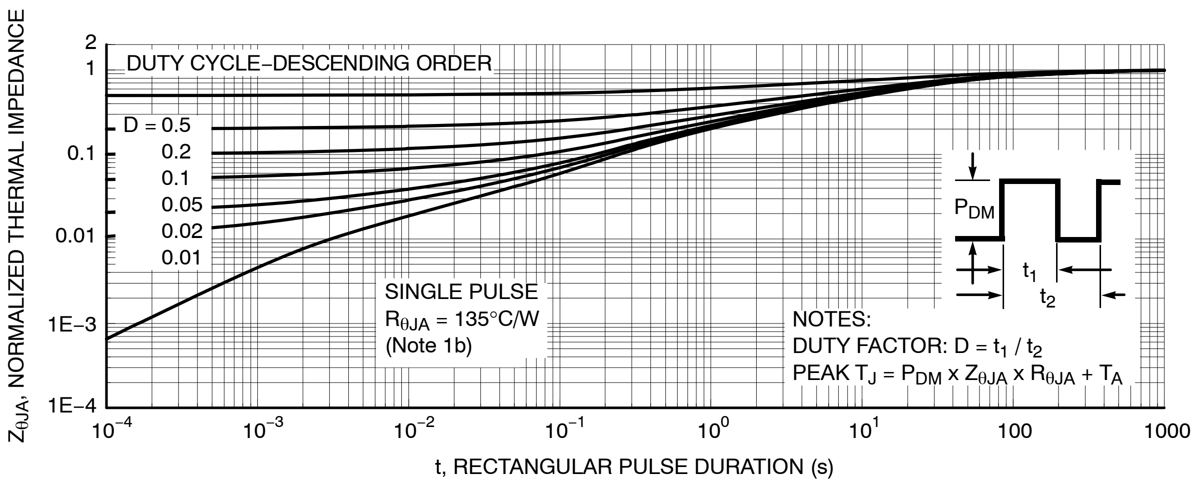



**Figure 26. Junction−to−Ambient Transient Thermal Response Curve**

## TYPICAL CHARACTERISTICS (continued)

### SyncFET Schottky Body Diode Characteristics

**onsemi**'s SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8011S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

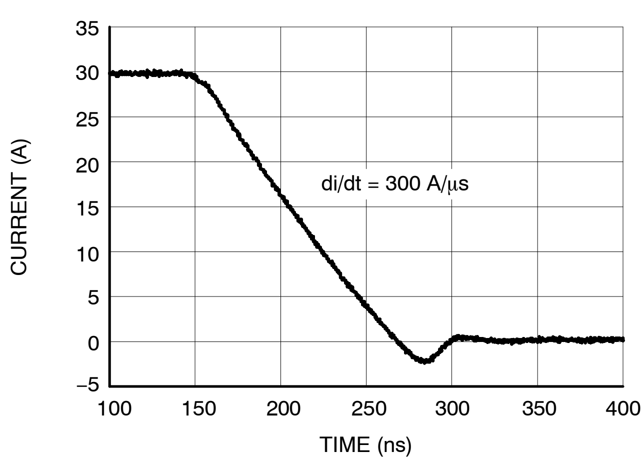



**Figure 27. FDPC8011S SyncFET Body Diode Reverse Recovery Characteristic**

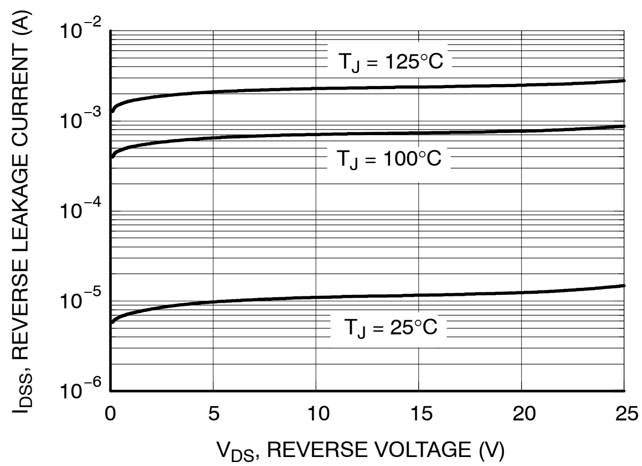



**Figure 28. SyncFET Body Diode Reverse Leakage versus Drain−Source Voltage**

## APPLICATION INFORMATION

**Typical Application Diagram (Synchronous Rectifier Buck Converter)**

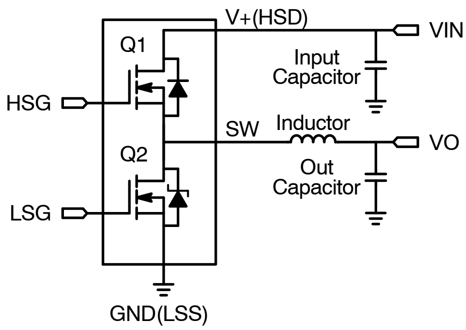



**Figure 29. Power Clip in Buck Converter Topology**

As shown in Figure 29 in the Power Clip package Q1 is the High Side MOSFET (Control MOSFET) and Q2 is the Low Side MOSFET (Synchronous MOSFET). Figure 30 below shows the package pin out. The blue overlay on the drawing indicates a typical PCB land pattern for the part.

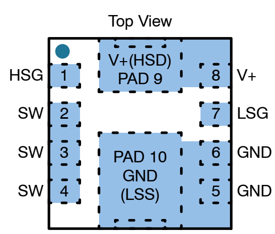



**Figure 30. Top View of Power Clip**

Table 1 Pin Information shows the name and description of each pin.

**Table 1. PIN INFORMATION**

| PIN | | Description |
|---|---|---|
| **Number** | **Name** | |
| 1 | HSG | Gate signal input of Q1 Gate |
| 2, 3, 4 | SW | Switch or Phase node, Source of Q1 and Drain of Q2 |
| 5, 6, PAD 10 | GND, GND(LSS) PAD | Ground, Source of Q2 |
| 7 | LSG | Gate signal input of Q2 Gate |
| 8, PAD 9 | V+, V+(HSD) PAD | Input voltage of SR Buck converter, Drain of Q1 |

## RECOMMENDED PCB LAYOUT GUIDELINES

As a PCB designer, it is necessary to address critical issues in layout to minimize losses and optimize the performance of the power train. Power Clip is a high power density solution and all high current flow paths, such as V+(HSD), SW and GND(LSS) should be short and wide for minimal resistance and inductance. V+(HSD) and GND(LSS) are the primary heat flow paths for the Power Clip. A recommended layout procedure is discussed below to maximize the electrical and thermal performance of the part.

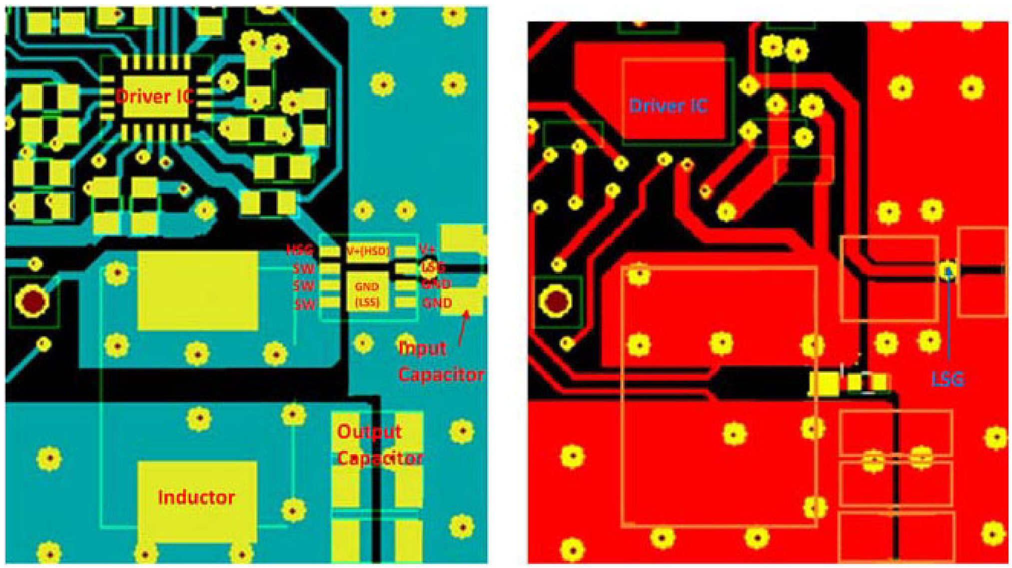



**Figure 31. Top/Component (Green) View and Bottom (Red) PCB View**

*Following is a guideline, not a requirement which the PCB designer should consider.*

Figure 31 shows an example of a well designed layout. The discussion that follows summarizes the key features of this layout.

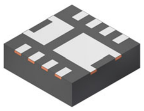
- “The input ceramic bypass capacitor between VIN and GND should be placed as close as possible to the pins V+ / V+(HSD) PAD and GND / GND(LSS) PAD to help reduce parasitic inductance and high frequency ringing. Several capacitors may be placed in parallel, and capacitors may be placed on both the top and bottom side of the board. The capacitor located immediately adjacent to the Power Clip will be the most effective at reducing HF parasitic. Caps located farther away, or on the opposite side of the board will also assist, but will be less effective due to increased trace inductance.
- “The Power Clip package design, with very short distance between pins V+ and GND, allows for a short connect distance to the input cap. This is a factor that enables the Power Clip switch loop to have very low parasitic inductance.
- “Use large copper areas on the component side to connect the V+ pin and V+ (HSD) pad, and the GND and GND(LSS) PAD.
- “The SW to inductor copper trace is a high current path. It will also be a high noise region due to switching voltage transients. The trace should be short and wide to enable a low resistance path and to minimize the size of the noise region. Care should be taken to minimize coupling of this trace to adjacent traces. The layout in Figure 31 shows a good example of this short, wide path.
- “The POWERTRENCH Technology MOSFETs used in the Power Clip are effective at minimizing SW node ringing. They incorporate a proprietary design1 that minimizes the peak overshoot ring voltage on the switch node (SW). They allow the part to operate well within the breakdown voltage limits. For most layouts, this eliminates the need to add an external snubber circuit. If the designer chooses to use an RC snubber, it should be placed close to the part between the SW pins and GND / GND(LSS) PAD to dampen the high frequency ringing.
- “The Driver IC should be placed relatively closed to HSG pin and LSG pin to minimize G drive trace inductance. Excessive G trace length may slow the switching speed of the HS drive. And it may lead to excessive ringing on the LS G. If the designer must place the driver a significant distance away from the Power Clip, it would be a good practice to include a 0 Ohm resistor in the LS G path as a place holder. In the final design, if the LS G exhibits excessive LF ringing, efficiency can often be improved by changing this resistor to a few Ohms to dampen the LS G LF ringing.

- "The Power Clip has very good Junction−PCB heat transfer from all power pins. It has much better heat transfer Junction−GND (LSS) than traditional dual FET packages. In most cases, board ground will be the most effective heat transfer path on the PCB. Use a large copper area between GND / GND(LSS) PAD pins and board ground. To ensure the best thermal and electrical connection to ground, we recommend using multiple vias to interconnect ground plane layers as shown in Figure 31.
- "Use multiple vias in parallel on each copper region to interconnect top, inner and bottom layers. This will reduce resistance and inductance of the vias and will improve thermal conductivity. Vias should be relatively large, around 8 mils to 10 mils.
- "Avoid using narrow thermal relief traces on the V+ / V+(HSD) PAD and GND / GND(LSS) PAD pins. These will increase HF switch loop inductance. And these will increase ringing of the HF power loop and the SW node.

## PACKAGE MARKING AND ORDERING INFORMATION

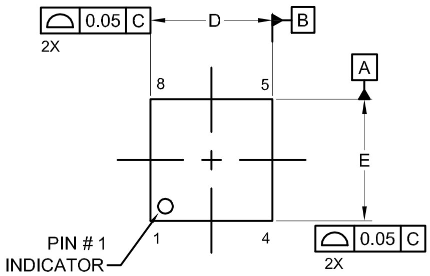
| Device | Device Marking | Package | Shipping† |
|---|---|---|---|
| FDPC8011S | 13OD/15OD | PQFN8 3.3X3.3, 0.65P<br>Power Clip 33 | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

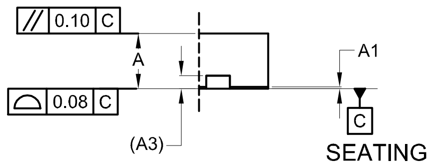


**PQFN8 3.3X3.3, 0.65P**
CASE 483AZ
ISSUE B

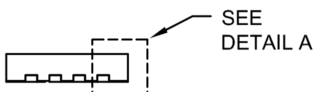
DATE 14 FEB 2022



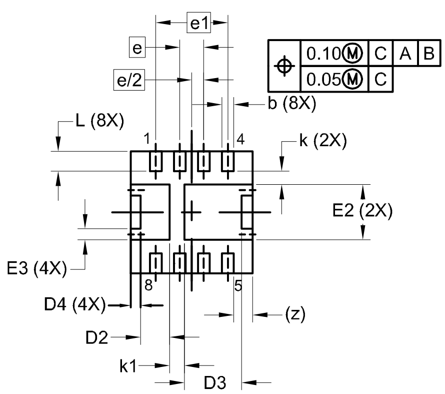

TOP VIEW




DETAIL 'A'
SCALE 2:1



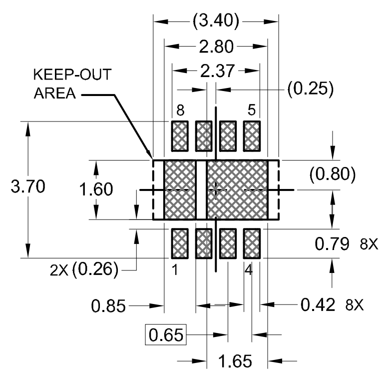

FRONT VIEW




BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS DO NOT INCLUDE BURSS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.




LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | -- | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.27 | 0.32 | 0.37 |
| D | 3.20 | 3.30 | 3.40 |
| D2 | 0.69 | 0.79 | 0.89 |
| D3 | 1.45 | 1.55 | 1.65 |
| D4 | 0.16 | 0.26 | 0.36 |
| E | 3.20 | 3.30 | 3.40 |
| E2 | 1.40 | 1.50 | 1.60 |
| E3 | 0.30 REF | | |
| e | 0.65 BSC | | |
| e1 | 1.95 BSC | | |
| e/2 | 0.325 BSC | | |
| k | 0.36 REF | | |
| k1 | 0.40 REF | | |
| L | 0.44 | 0.54 | 0.64 |
| z | 0.52 REF | | |

| | | |
|---|---|---|
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| **DESCRIPTION:** | **PQFN8 3.3X3.3, 0.65P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT:** www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales

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