

MOSFET – N-Channel, POWERTRENCH®

100 V, 50 A, 15 mΩ

FDP150N10A

Description

This N-Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

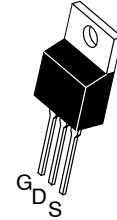
Features

- $R_{DS(on)} = 12.5 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$
- Fast Switching Speed
- Low Gate Charge, $Q_G = 16.2 \text{ nC}$ (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Applications

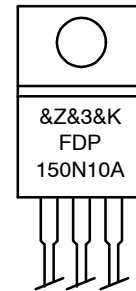
- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
100 V	15.0 mΩ @ 10 V	50 A

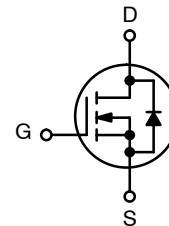


TO-220
 CASE 221A

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code Format
- &K = 2-Digits Lot Run Traceability Code
- FDP150N10A = Device Code



N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	FDP150N10A_F102	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	50
		- Continuous ($T_C = 100^\circ\text{C}$)	36
I_{DM}	Drain Current	- Pulsed (Note 1)	200
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	84.6	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	91
		- Derate Above 25°C	0.61
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 2\text{ mH}$, $I_{AS} = 9.2\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 100\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP150N10A_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	–	0.08	–	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$	–	–	1	μA
		$V_{DS} = 80 \text{ V}$, $T_C = 150^\circ\text{C}$	–	–	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$	–	12.5	15.0	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}$, $I_D = 50 \text{ A}$	–	40	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	–	1080	1440	pF
C_{oss}	Output Capacitance		–	267	355	pF
C_{rss}	Reverse Transfer Capacitance		–	11	–	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$	–	436	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$, (Note 4)	–	16.2	21.0	nC
Q_{gs}	Gate to Source Gate Charge		–	5.3	–	nC
Q_{gs2}	Gate Charge Threshold to Plateau		–	2.6	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	3.7	–	nC
ESR	Equivalent Series Resistance (G–S)	$f = 1 \text{ MHz}$	–	1.3	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 50 \text{ V}$, $I_D = 50 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_G = 4.7 \Omega$ (Note 4)	–	13	36	ns
t_r	Turn–On Rise Time		–	16	42	ns
$t_{d(off)}$	Turn–Off Delay Time		–	21	52	ns
t_f	Turn–Off Fall Time		–	5	20	ns

DRAIN–SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current	–	–	50	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	–	–	200	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 50 \text{ A}$	–	–	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $V_{DD} = 50 \text{ V}$, $I_{SD} = 50 \text{ A}$, $di_F/dt = 100 \text{ A}/\mu\text{s}$	–	50	–	ns
Q_{rr}	Reverse Recovery Charge		–	55	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

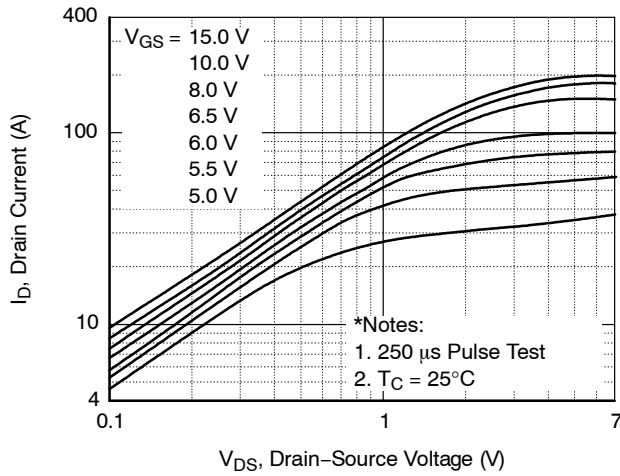


Figure 1. On-Region Characteristics

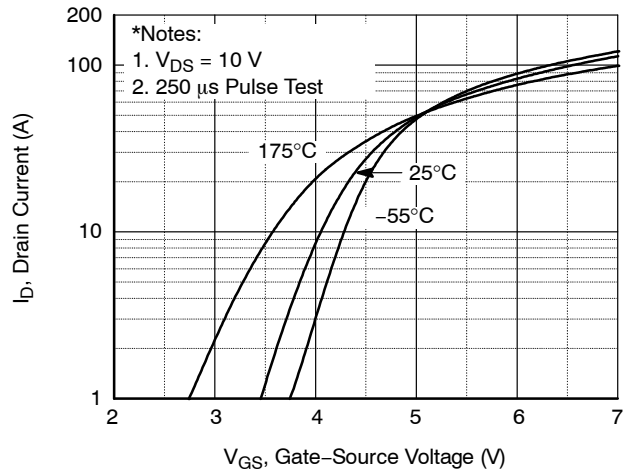


Figure 2. Transfer Characteristics

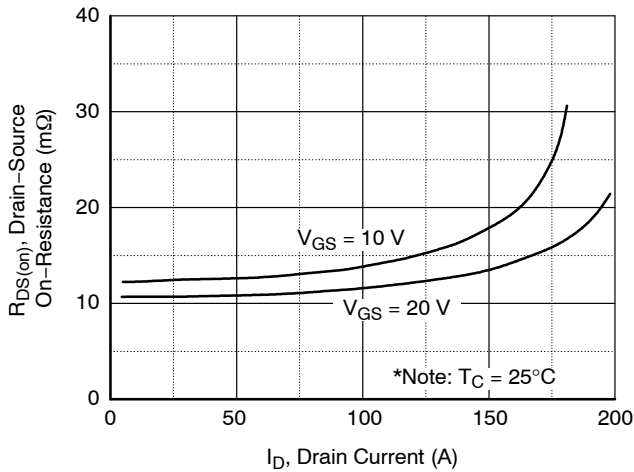


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

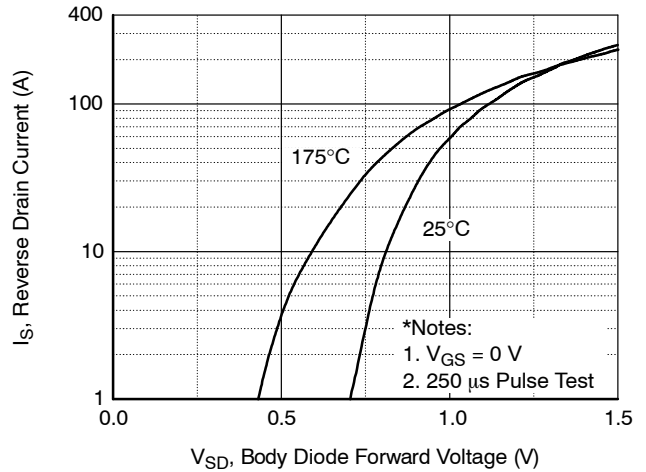


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

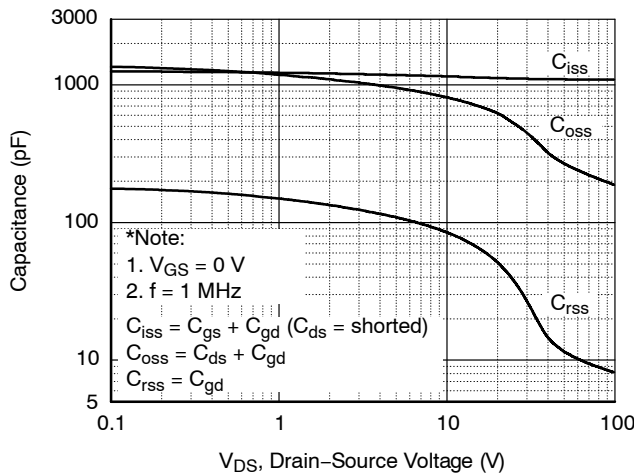


Figure 5. Capacitance Characteristics

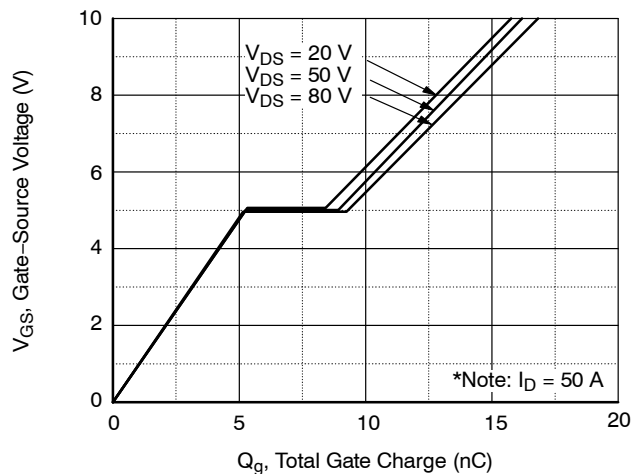


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

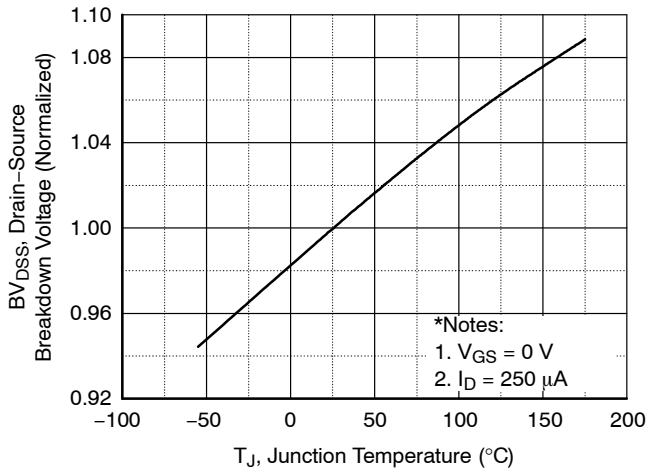


Figure 7. Breakdown Voltage Variation vs. Temperature

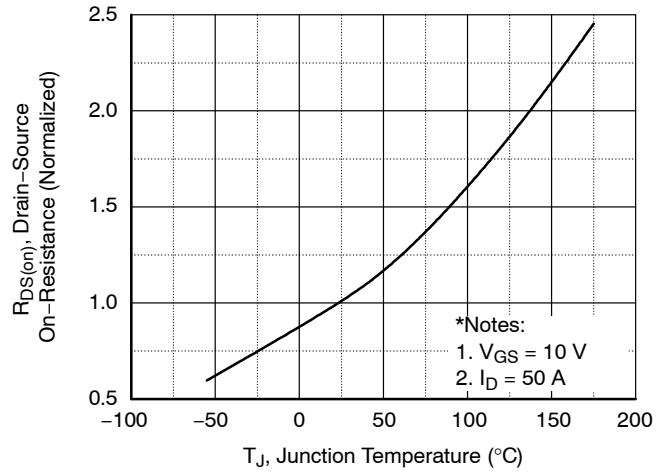


Figure 8. On-Resistance Variation vs. Temperature

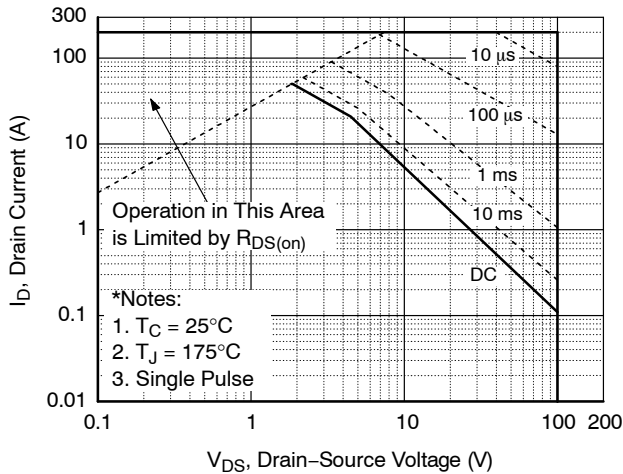


Figure 9. Maximum Safe Operating Area

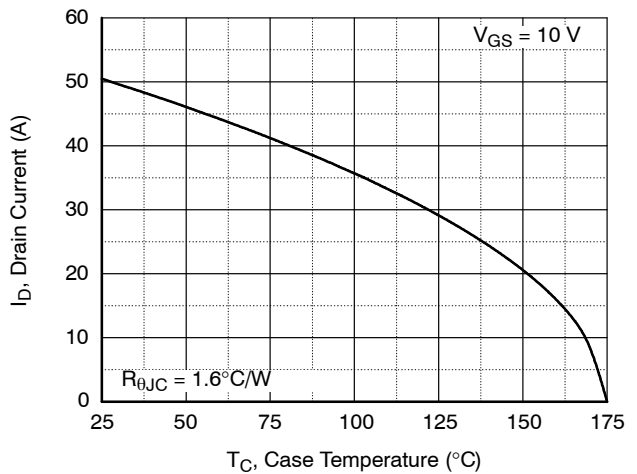


Figure 10. Maximum Drain Current vs. Case Temperature

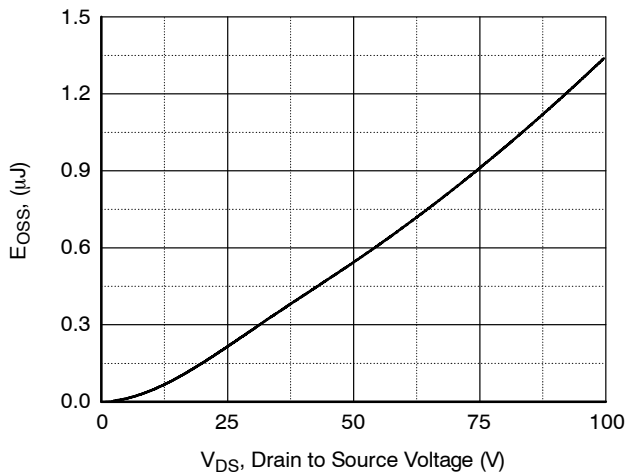


Figure 11. E_{oss} vs. Drain to Source Voltage

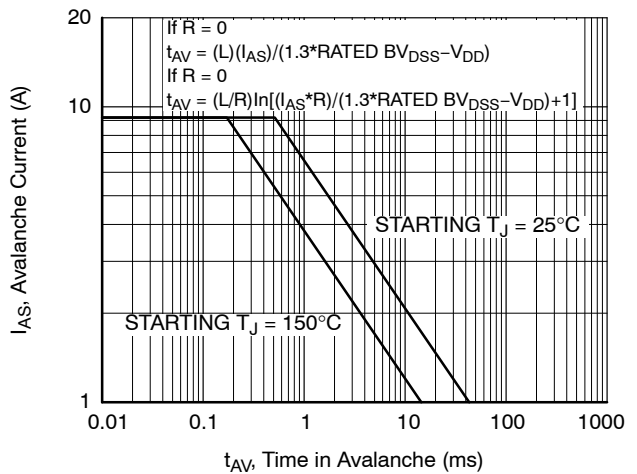


Figure 12. Unclamped Inductive Switching Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

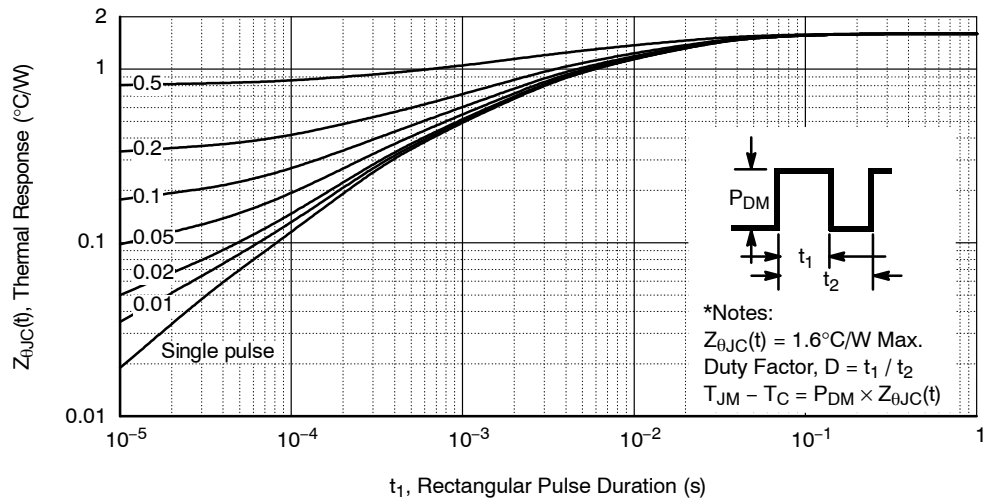


Figure 13. Transient Thermal Response Curve

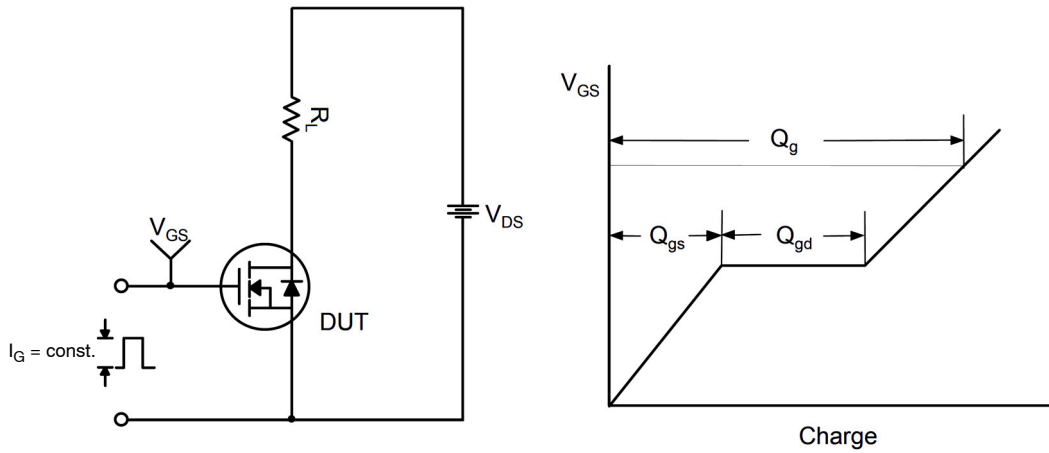


Figure 14. Gate Charge Test Circuit & Waveform

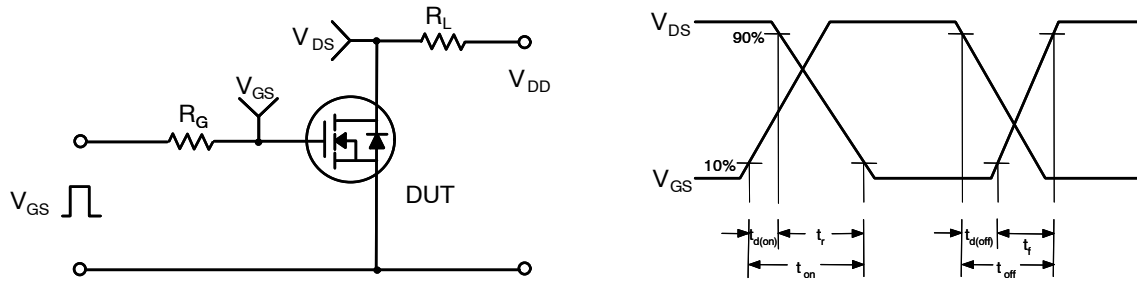


Figure 15. Resistive Switching Test Circuit & Waveforms

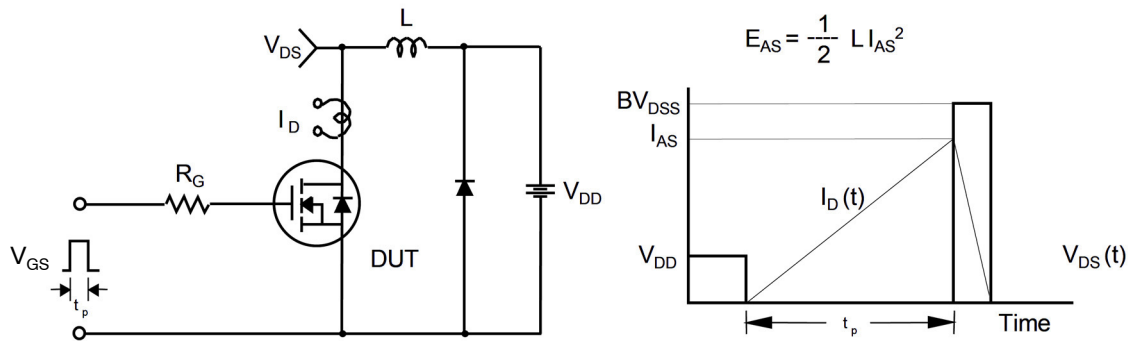


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

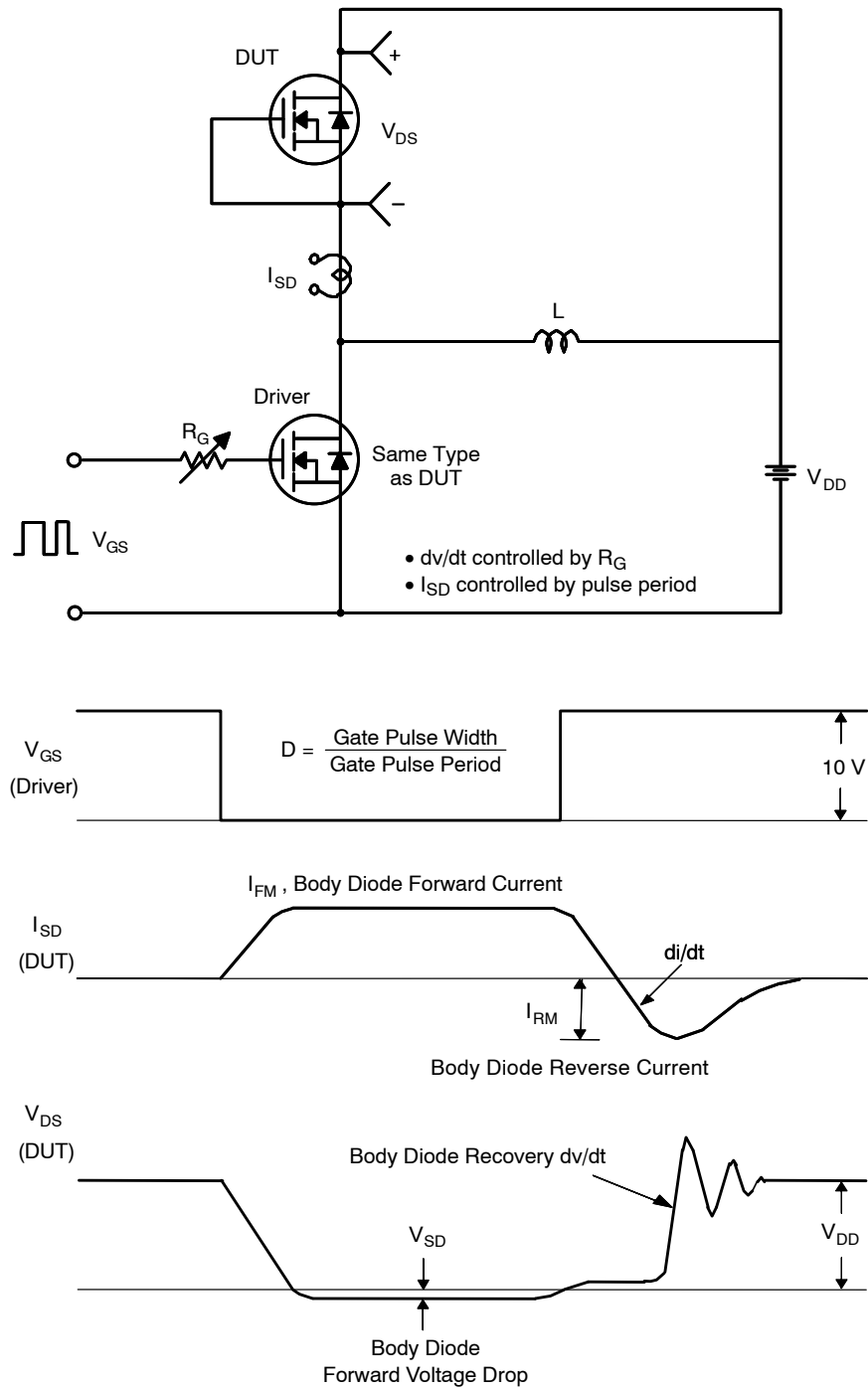


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

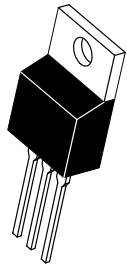
ORDERING INFORMATION

Part Number	Device Marking	Package	Reel Size	Tape Width	Shipping
FDP150N10A-F102	FDP150N10A	TO-220	N/A	N/A	800 Units / Tube

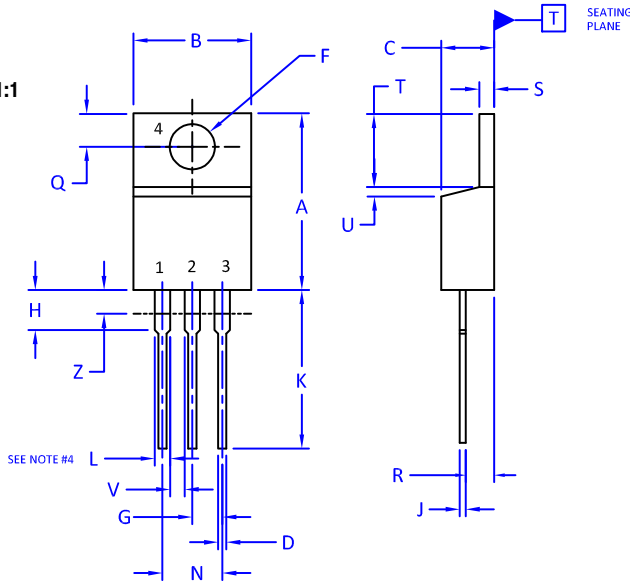
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CASE 221A
ISSUE AK

DATE 13 JAN 2022



SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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