

MOSFET – N-Channel DUAL COOL[®] 88 POWERTRENCH[®] 80 V, 254 A, 1.35 mΩ

FDMT80080DC

Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest $R_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Features

- Max $R_{DS(on)}$ = 1.35 mΩ at V_{GS} = 10 V, I_D = 36 A
- Max $R_{DS(on)}$ = 1.82 mΩ at V_{GS} = 8 V, I_D = 31 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Next Generation Enhanced Body diode technology, Engineered for Soft recovery
- Low profile 8x8mm MLP package
- MSL1 Robust Package Design
- 100% UIL tested
- These Device is Pb-Free, Halide Free, and is RoHS Compliant

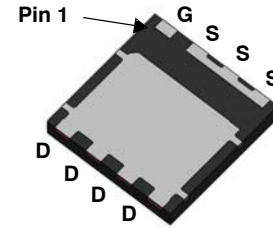
Typical Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion

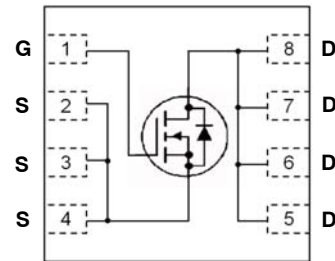
MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous $T_C = 25^\circ\text{C}$ (Note 5) – Continuous $T_C = 100^\circ\text{C}$ (Note 5) – Continuous $T_A = 25^\circ\text{C}$ (Note 1) – Pulsed (Note 4)	254 160 36 1453	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	1734	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$ Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1)	156 3.2	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

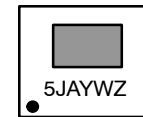
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



PQFN8 8X8, 2P
CASE 483AQ



MARKING DIAGRAM



- 5J = Specific Device Code
A = Assembly Plant Code
YW = Data Code (Year & Week)
Z = Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMT80080DC

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	41	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	–12	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 36\ \text{A}$ $V_{GS} = 8\ \text{V}$, $I_D = 31\ \text{A}$, $V_{GS} = 10\ \text{V}$, $I_D = 36\ \text{A}$, $T_J = 125^\circ\text{C}$	– – –	1.06 1.23 1.74	1.35 1.82 2.22	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 36\ \text{A}$	–	116	–	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	14800	20720	pF
C_{oss}	Output Capacitance		–	2080	2915	pF
C_{rss}	Reverse Transfer Capacitance		–	56	125	pF
R_g	Gate Resistance		0.1	1.8	4.5	Ω

Switching Characteristics

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 40\ \text{V}$, $I_D = 36\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	67	108	ns
t_r	Rise Time		–	65	104	ns
$t_{d(off)}$	Turn–Off Delay Time		–	75	120	ns
t_f	Fall Time		–	30	48	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$, to $10\ \text{V}$, $V_{DD} = 40\ \text{V}$, $I_D = 36\ \text{A}$	–	195	273	nC
	Total Gate Charge	$V_{GS} = 0\ \text{V}$, to $8\ \text{V}$, $V_{DD} = 40\ \text{V}$, $I_D = 36\ \text{A}$	–	159	223	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 40\ \text{V}$, $I_D = 36\ \text{A}$	–	69	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	36	–	nC

Drain–Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2.6\ \text{A}$ (Note 2)	–	0.7	1.1	V
		$V_{GS} = 0\ \text{V}$, $I_S = 36\ \text{A}$ (Note 2)	–	0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 36\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	81	130	ns
Q_{rr}	Reverse Recovery Charge		–	88	141	nC

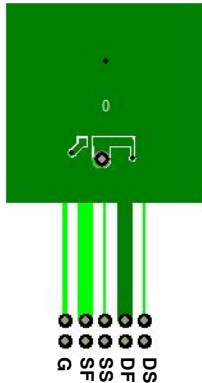
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top Source)	1.6	$^{\circ}\text{C/W}$
	Thermal Resistance, Junction-to-Case (Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	38	
	Thermal Resistance, Junction-to-Ambient (Note 1b)	81	
	Thermal Resistance, Junction-to-Ambient (Note 1c)	26	
	Thermal Resistance, Junction-to-Ambient (Note 1d)	34	
	Thermal Resistance, Junction-to-Ambient (Note 1e)	14	
	Thermal Resistance, Junction-to-Ambient (Note 1f)	16	
	Thermal Resistance, Junction-to-Ambient (Note 1g)	26	
	Thermal Resistance, Junction-to-Ambient (Note 1h)	60	
	Thermal Resistance, Junction-to-Ambient (Note 1i)	15	
	Thermal Resistance, Junction-to-Ambient (Note 1j)	21	
	Thermal Resistance, Junction-to-Ambient (Note 1k)	9	
	Thermal Resistance, Junction-to-Ambient (Note 1l)	11	

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta CA}$ is determined by the user's board design.



a) 38 $^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper.



b) 81 $^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

- Still air, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
 - Still air, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
 - Still air, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
 - Still air, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
 - 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
 - 200FPM Airflow, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
 - 200FPM Airflow, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.
 - E_{AS} of 1734 mJ is based on starting $T_J = 25^{\circ}\text{C}$, $L = 3$ mH, $I_{AS} = 34$ A, $V_{DD} = 80$ V, $V_{GS} = 10$ V. 100% test at $L = 0.3$ mH, $I_{AS} = 75$ A
 - Pulsed Id please refer to Figure 11 SOA graph for more details.
 - Computed Continuous Current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED

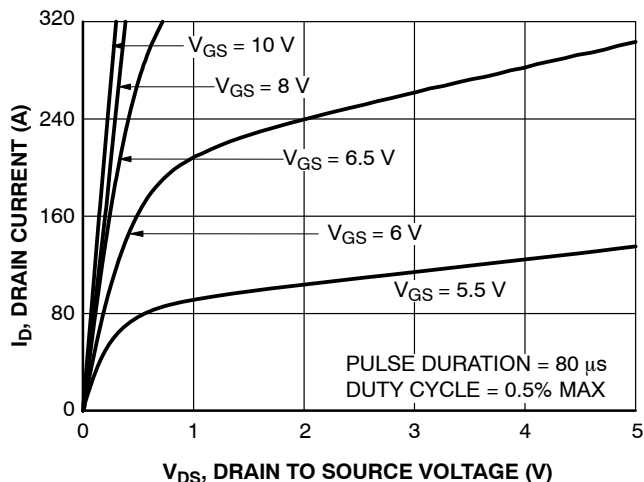


Figure 1. On-Region Characteristics

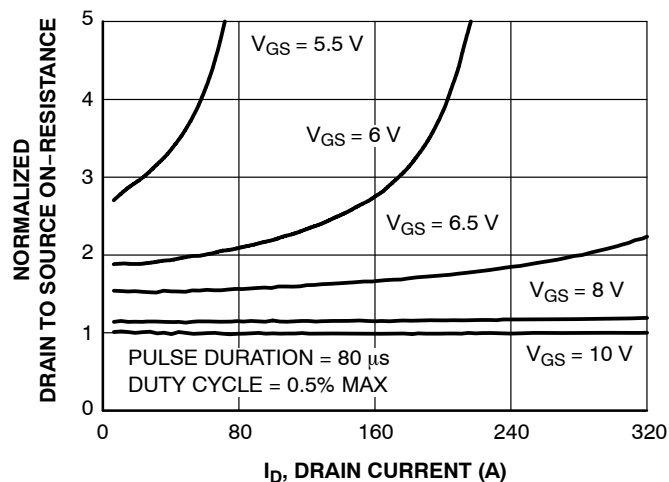


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

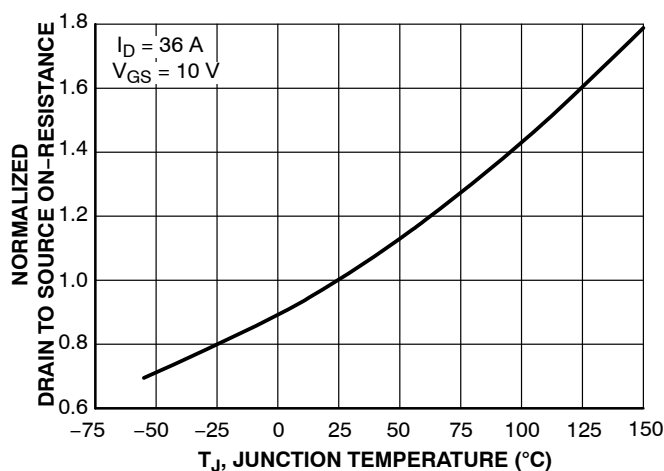


Figure 3. Normalized On Resistance vs. Junction Temperature

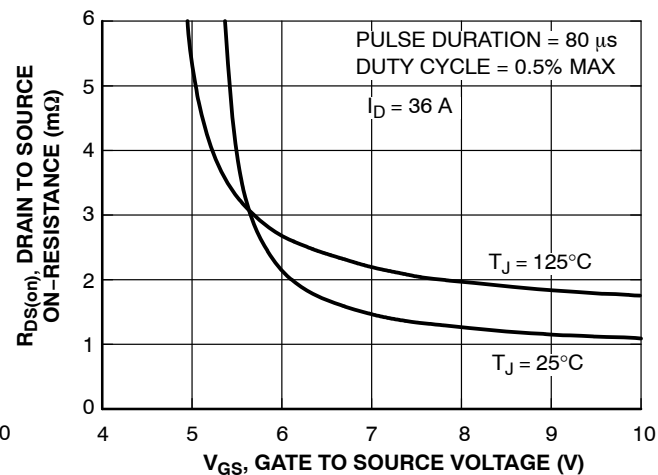


Figure 4. On Resistance vs. Gate to Source Voltage

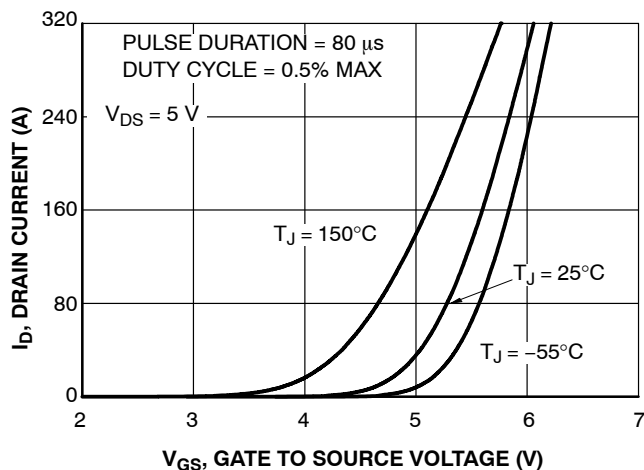


Figure 5. Transfer Characteristics

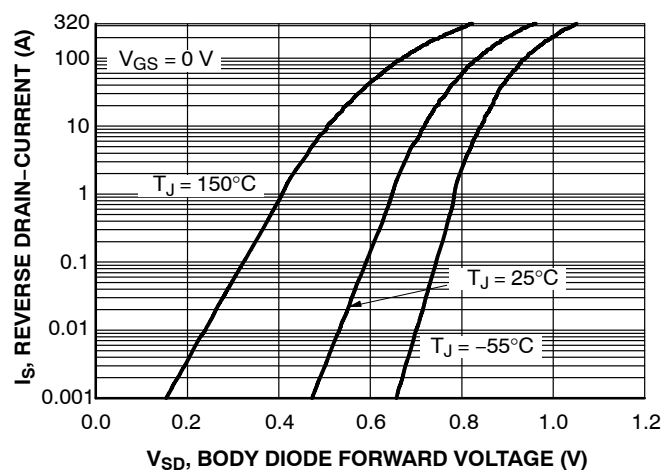


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (CONTINUED) $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED

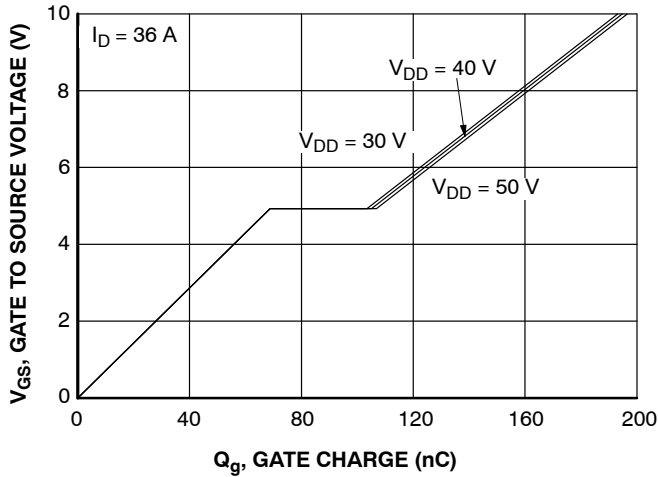


Figure 7. Gate Charge Characteristics

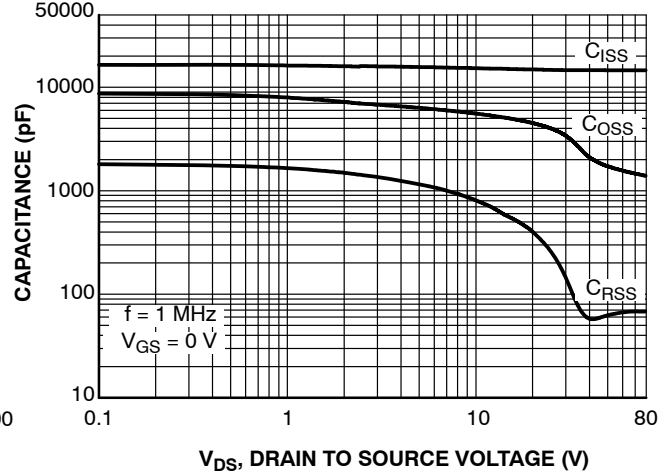


Figure 8. Capacitance vs. Drain to Source Voltage

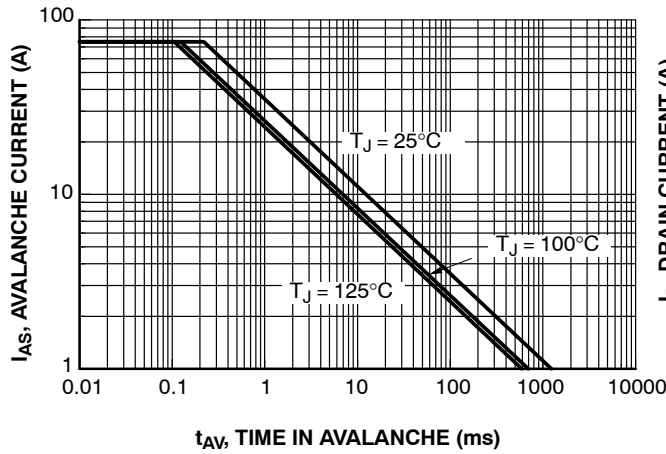


Figure 9. Unclamped Inductive Switching Capability

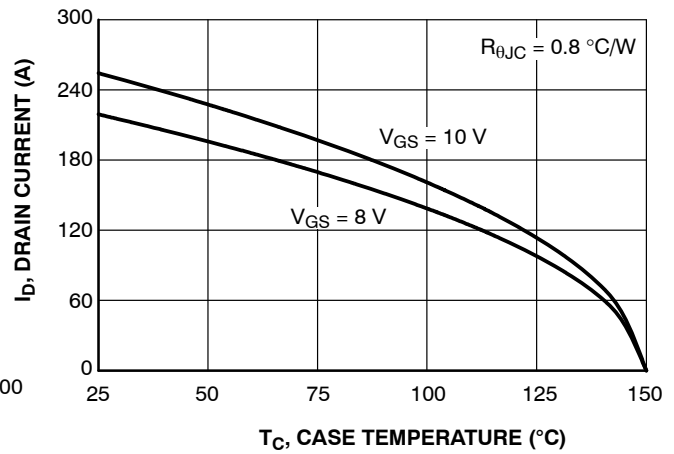


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

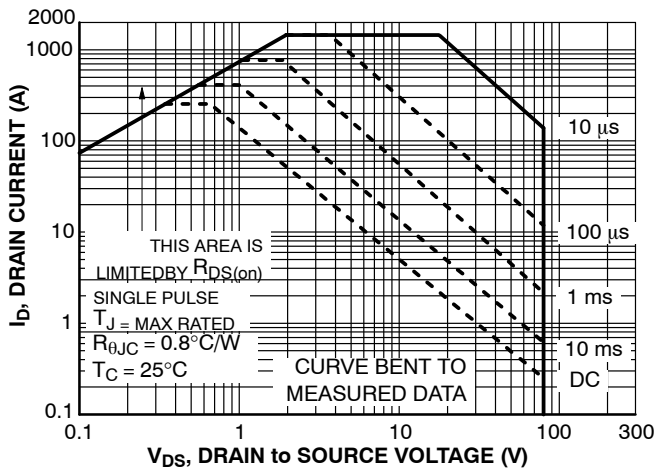


Figure 11. Forward Bias Safe Operating Area

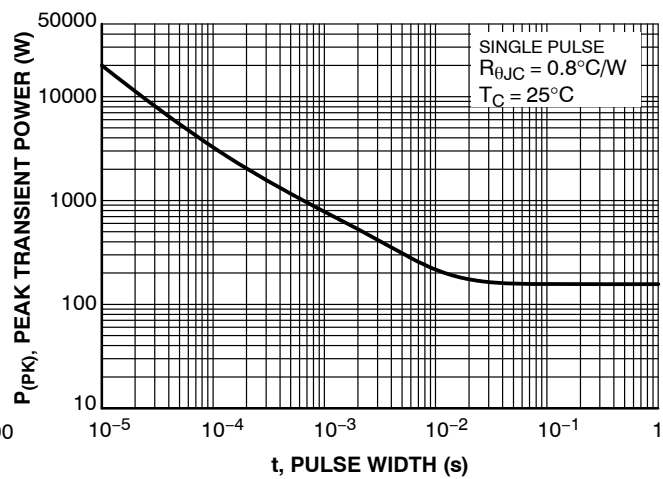


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED) $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED

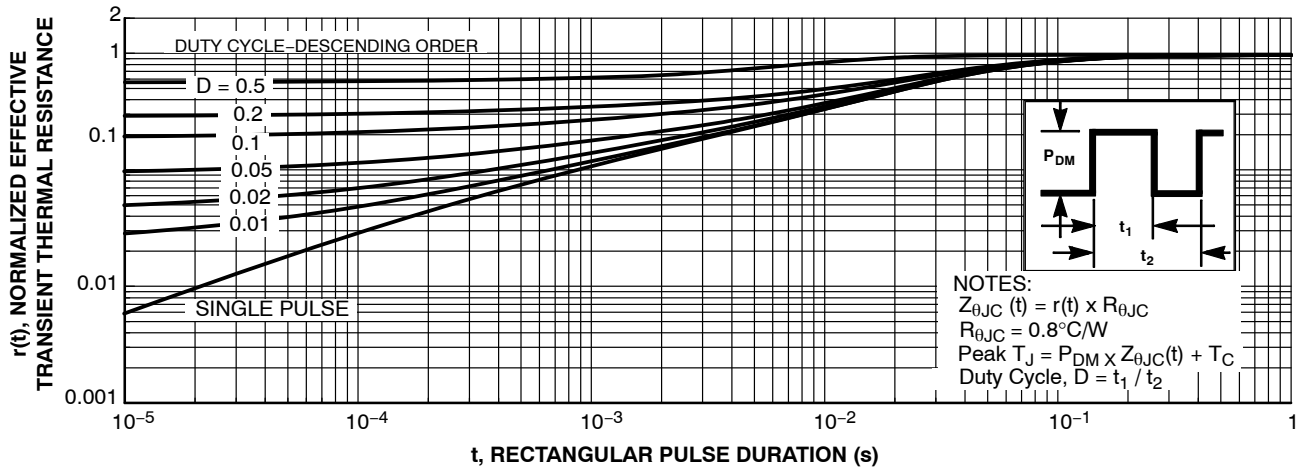
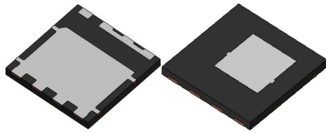


Figure 13. Junction-to-Case Transient Thermal Response Curve

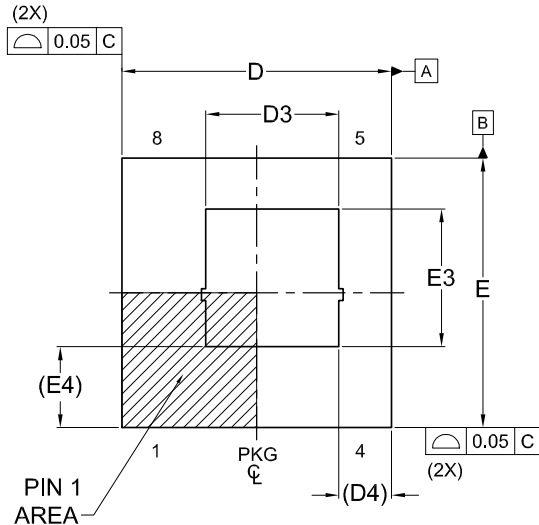
ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping (Qty / Packing) [†]
5J	FDMT80080DC	Dual Cool™88	13"	13.3 mm	3000 / Tape & Reel

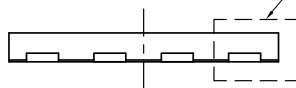
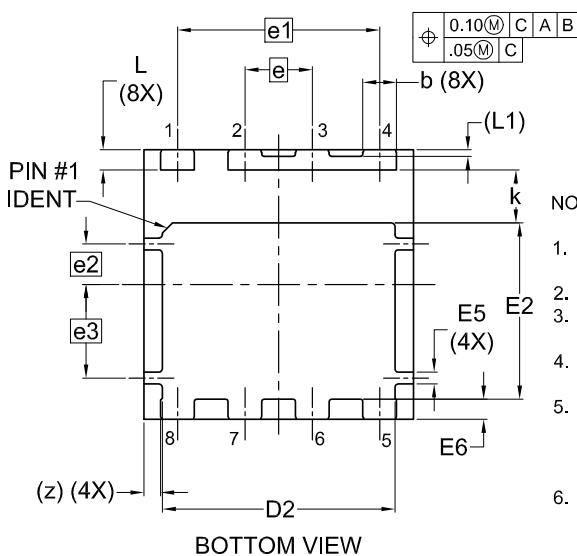
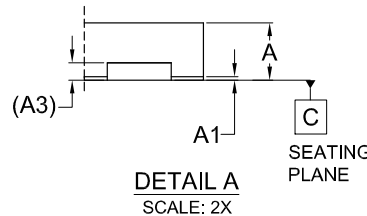
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).


PQFN8 8X8, 2P
CASE 483AQ
ISSUE B

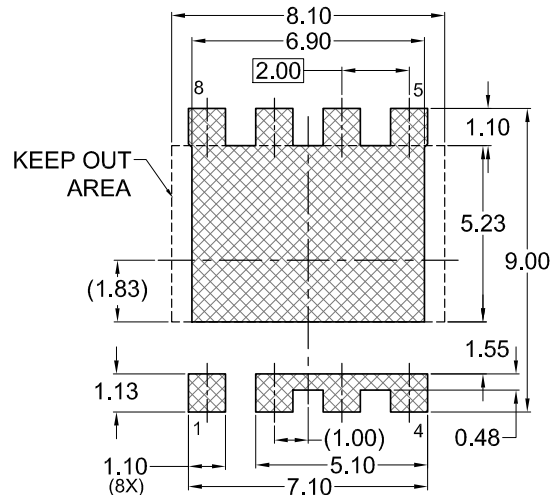
DATE 24 OCT 2022


TOP VIEW

SEE DETAIL A


FRONT VIEW

BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.85	0.95
A1	0.00	-	0.05
A3	0.25 REF		
b	0.90	1.00	1.10
D	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	3.68	3.86	4.03
D4	1.56 REF		
E	7.90	8.00	8.10
E2	5.13	5.23	5.33
E3	3.99	4.09	4.19
E4	2.41 REF		
E5	0.35 REF		
E6	0.60 REF		
e	2.00 BSC		
e1	6.00 BSC		
e2	1.20 BSC		
e3	2.78 BSC		
k	1.48	1.58	1.68
L	0.50	0.60	0.70
L1	0.20 REF		
z	0.50 REF		

DOCUMENT NUMBER: 98AON13665G

Electronic versions are uncontrolled except when accessed directly from the Document Repository.
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: PQFN8 8X8, 2P

PAGE 1 OF 1

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales