

# FDMS86200

## MOSFET, N-Channel, Shielded Gate, POWERTRENCH®

150 V, 35 A, 18 mΩ

### General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 18 mΩ at  $V_{GS} = 10$  V,  $I_D = 9.6$  A
- Max  $r_{DS(on)}$  = 21 mΩ at  $V_{GS} = 6$  V,  $I_D = 8.8$  A
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

### Applications

- DC-DC Conversion

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

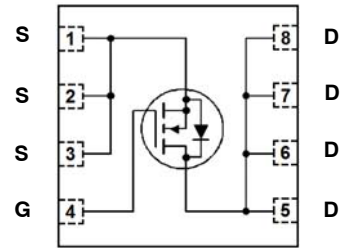
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current: – Continuous $T_C = 25^\circ\text{C}$ – Continuous $T_A = 25^\circ\text{C}$ (Note 1a) – Pulsed	35 9.6 100	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	220	mJ
$P_D$	Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	104 2.5	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

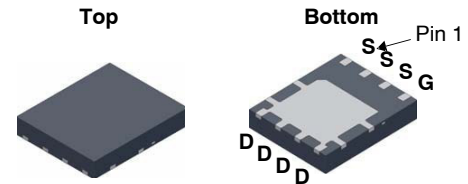


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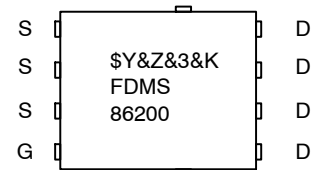


N-Channel MOSFET



Power 56  
(PQFN8)  
CASE 483AE

### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
 &Z = Assembly Plant Code  
 &3 = Data Code (Year & Week)  
 &K = Lot  
 FDMS86200 = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDMS86200

## PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Quantity
FDMS86200	FDMS86200	Power 56 (PQFN8) (Pb-Free / Halogen Free)	3000/Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$	150			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		110		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120 \text{ V}$ , $V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$			100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu\text{A}$	2.0	2.5	4.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-10		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 9.6 \text{ A}$		15	18	m $\Omega$
		$V_{GS} = 6 \text{ V}$ , $I_D = 8.8 \text{ A}$		17	21	
		$V_{GS} = 10 \text{ V}$ , $I_D = 9.6 \text{ A}$ , $T_J = 125^\circ\text{C}$		28	34	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}$ , $I_D = 9.6 \text{ A}$		33		S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 75 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		2041	2715	pF
$C_{oss}$	Output Capacitance			203	270	pF
$C_{rss}$	Reverse Transfer Capacitance			10	16	pF
$R_g$	Gate Resistance	$f = 1 \text{ MHz}$	0.1	1.2	3	$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75 \text{ V}$ , $I_D = 9.6 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_{GEN} = 6 \Omega$		13	23	ns
$t_r$	Rise Time			7.9	16	ns
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns
$t_f$	Fall Time			5.8	12	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V}$ to $10 \text{ V}$ , $V_{DD} = 75 \text{ V}$ , $I_D = 9.6 \text{ A}$		33	46	nC
		$V_{GS} = 0 \text{ V}$ to $5 \text{ V}$ , $V_{DD} = 75 \text{ V}$ , $I_D = 9.6 \text{ A}$		18	26	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 75 \text{ V}$ , $I_D = 9.6 \text{ A}$		7.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7.7		nC

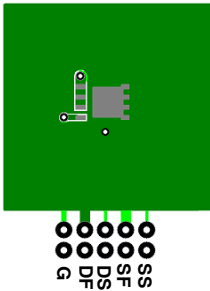
**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.69	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 9.6\text{ A}$ (Note 2)		0.77	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 9.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		76	120	ns
$Q_{rr}$	Reverse Recovery Charge			113	181	nC

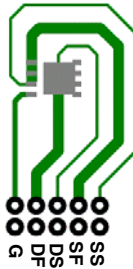
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**NOTES:**

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- $E_{AS}$  of 220 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 21\text{ A}$ ,  $V_{DD} = 150\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 46\text{ A}$ .

**TYPICAL CHARACTERISTICS**

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

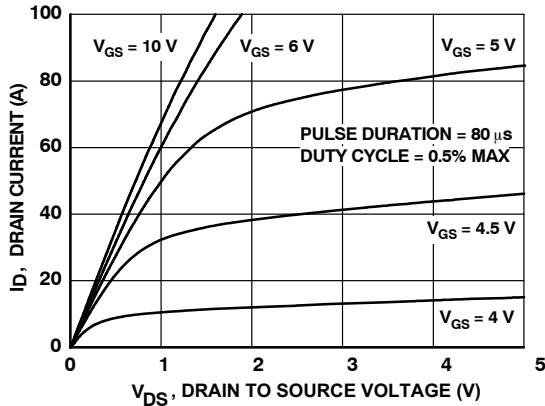


Figure 1. On Region Characteristics

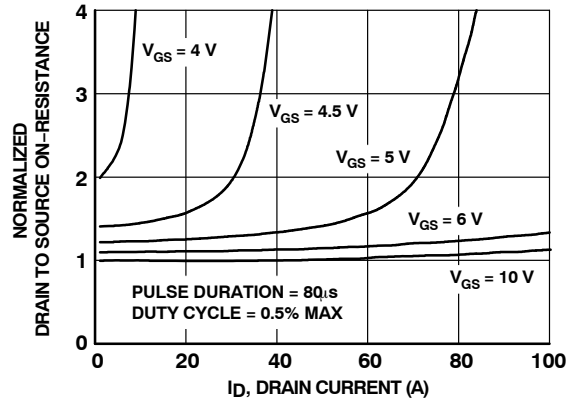


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

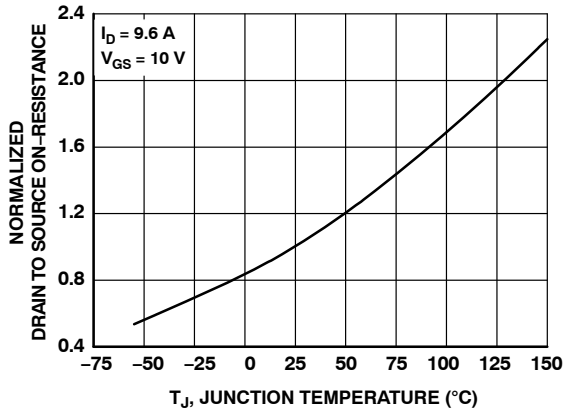


Figure 3. Normalized On Resistance vs. Junction Temperature

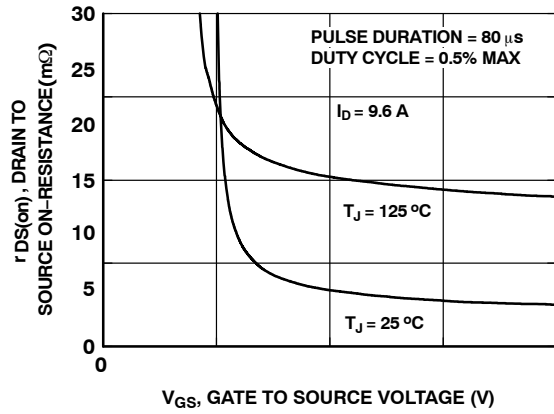


Figure 4. On-Resistance vs. Gate to Source Voltage

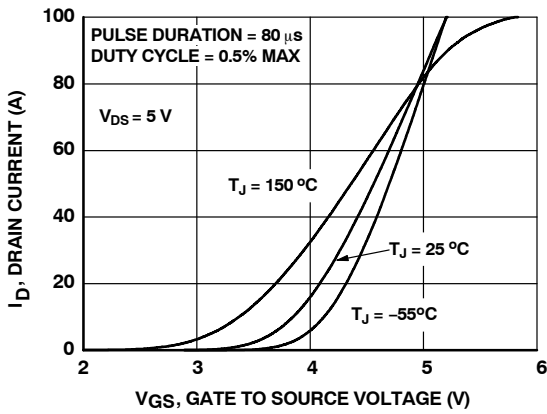


Figure 5. Transfer Characteristics

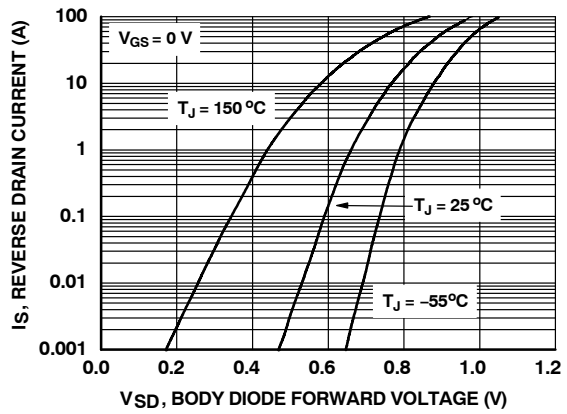


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

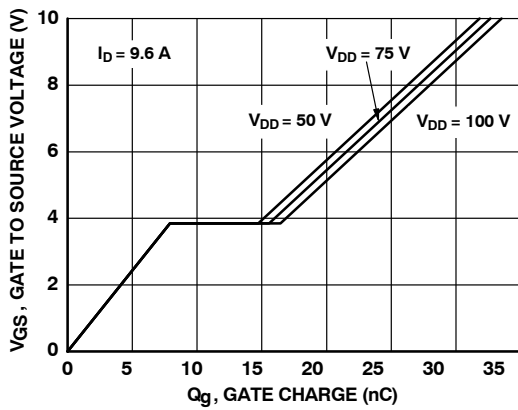


Figure 7. Gate Charge Characteristics

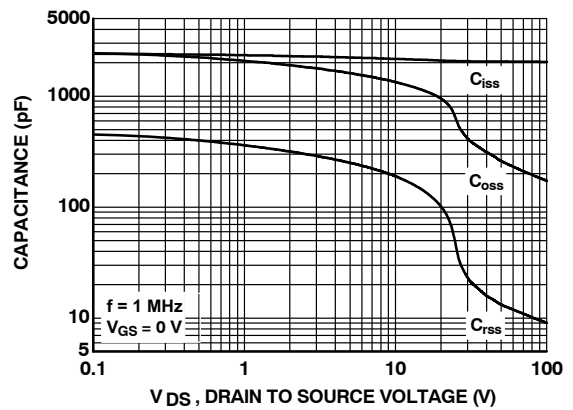


Figure 8. Capacitance vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

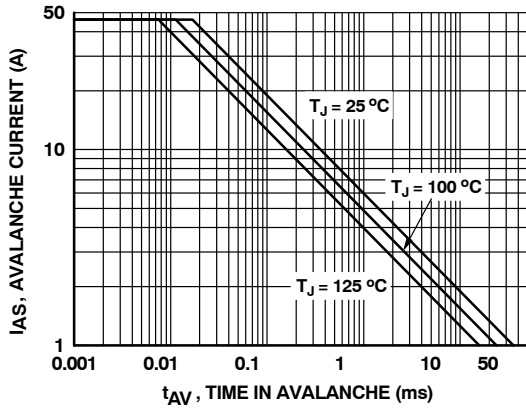


Figure 9. Unclamped Inductive Switching Capability

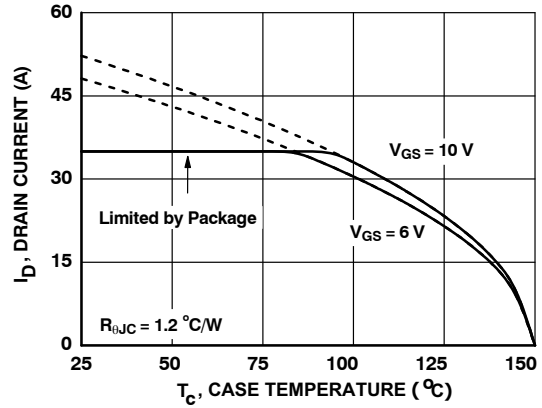


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

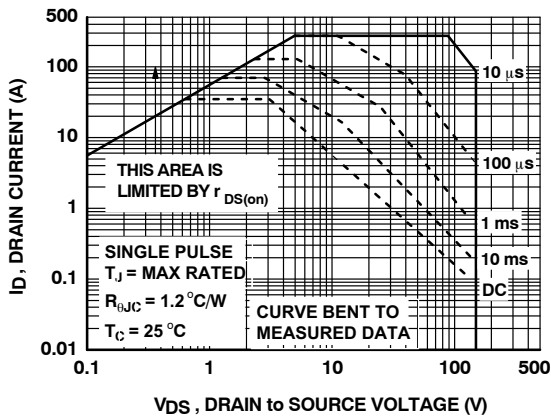


Figure 11. Forward Bias Safe Operating Area

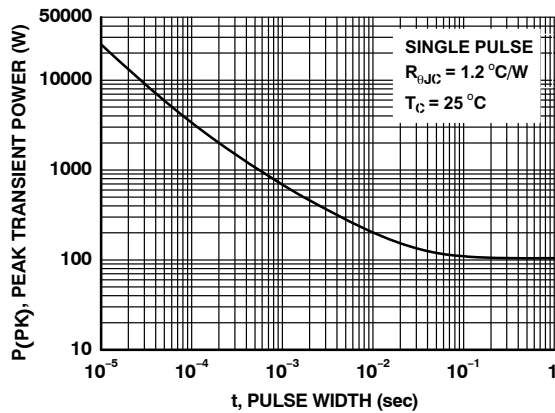


Figure 12. Single Pulse Maximum Power Dissipation

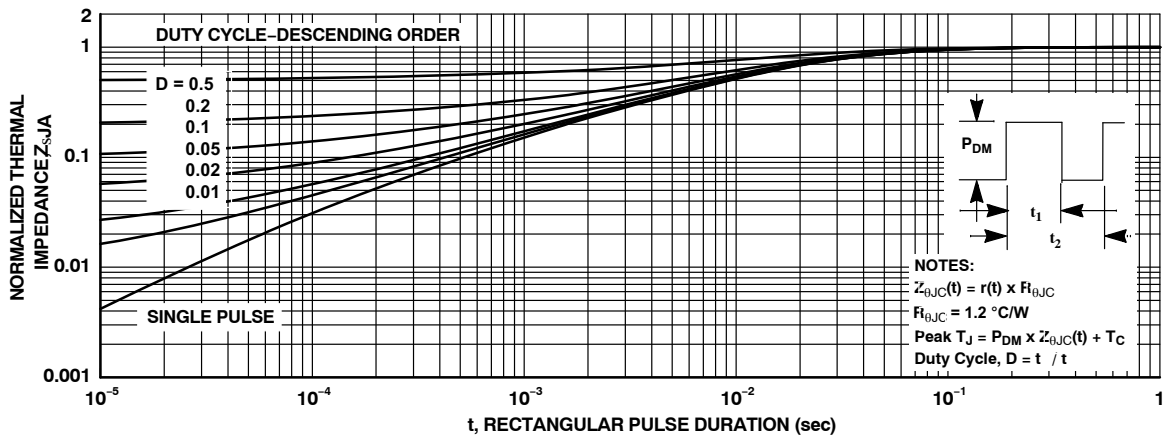


Figure 13. Transient Thermal Response Curve

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



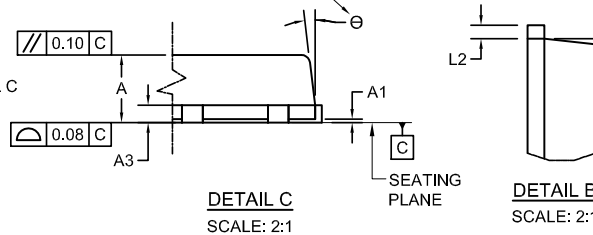
**PQFN8 5X6, 1.27P**  
CASE 483AE  
ISSUE C

DATE 21 JAN 2022

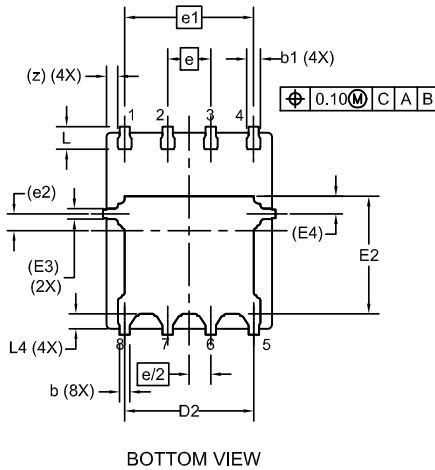


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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