

FDMS4D4N08C

MOSFET – POWERTRENCH[®], N-Channel Shielded Gate

80 V, 123 A, 4.3 mΩ

Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced POWERTRENCH[®] process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 4.3 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 44\text{ A}$
- Max $r_{DS(on)}$ = 10.4 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 22\text{ A}$
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

Typical Applications

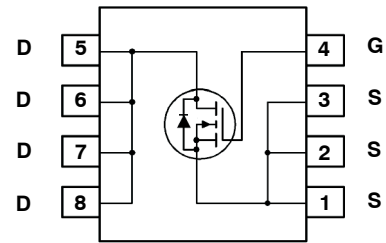
- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar



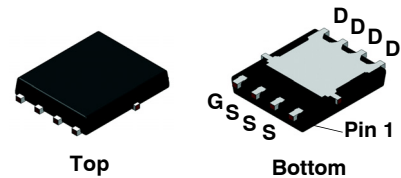
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ELECTRICAL CONNECTION

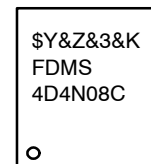


N-Channel MOSFET



**Power 56
(PQFN8 5x6)
CASE 483AE**

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMS4D4N08C	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V _{DS}	Drain to Source Voltage	80	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Drain Current –Continuous T _C = 25°C (Note 5)	123	A
	–Continuous T _C = 100°C (Note 5)	78	
	–Continuous T _A = 25°C (Note 1a)	17	
	–Pulsed (Note 4)	498	
E _{AS}	Single Pulse Avalanche Energy (Note 3)	486	mJ
P _D	Power Dissipation T _C = 25°C	125	W
	Power Dissipation T _A = 25°C (Note 1a)	2.5	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJC}	Thermal Resistance, Junction to Case	1.0	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	50	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
FDMS4D4N08C	FDMS4D4N08C	PQFN8 5×6 (Pb-Free/Halogen Free)	3000 Units/ Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		63		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			± 100	nA

ON CHARACTERISTICS (Note NO TAG)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		-8.2		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 44 \text{ A}$		3.7	4.3	m Ω
		$V_{GS} = 6 \text{ V}, I_D = 22 \text{ A}$		5.7	10.4	
		$V_{GS} = 10 \text{ V}, I_D = 44 \text{ A}, T_J = 125^\circ\text{C}$		5.9	7.2	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 44 \text{ A}$		98		S

DYNAMIC CHARACTERISTICS

C_{ISS}	Input Capacitance	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		2920	4090	pF
C_{OSS}	Output Capacitance			1045	1465	
C_{RSS}	Reverse Transfer Capacitance			35	50	
R_G	Gate Resistance		0.1	1.3	2.5	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn – On Delay Time	$V_{DD} = 40 \text{ V}, I_D = 44 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		17	31	ns
t_r	Rise Time			7	15	
$t_{d(off)}$	Turn – Off Delay Time			25	40	
t_f	Fall Time			5	10	
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$	$V_{DD} = 40 \text{ V}, I_D = 44 \text{ A}$	40	56	nC
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 6 \text{ V}$		25	35	
Q_{gs}	Gate to Source Charge			13		
Q_{gd}	Gate to Drain "Miller" Charge			8		
Q_{oss}	Output Charge	$V_{DD} = 40 \text{ V}, V_{GS} = 0 \text{ V}$		60		nC
Q_{sync}	Output Charge	$V_{DS} = 0 \text{ V}, I_D = 44 \text{ A}$		35		

DRAIN-SOURCE DIODE CHARACTERISTICS

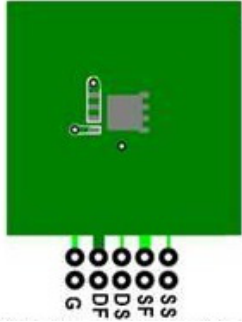
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0 \text{ V}, I_S = 44 \text{ A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 22 \text{ A}, di/dt = 300 \text{ A}/\mu\text{s}$		26	42	ns
Q_{rr}	Reverse Recovery Charge			44	71	
t_{rr}	Reverse Recovery Time	$I_F = 22 \text{ A}, di/dt = 1000 \text{ A}/\mu\text{s}$		20	32	ns
Q_{rr}	Reverse Recovery Charge			106	169	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

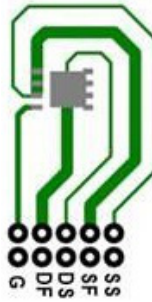
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NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 486 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 3\text{ mH}$, $I_{AS} = 18\text{ A}$, $V_{DD} = 80\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 51\text{ A}$.
4. Pulsed I_D please refer to Fig. 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

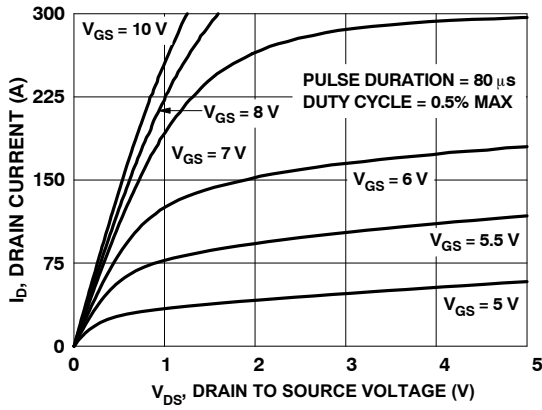


Figure 1. On Region Characteristics

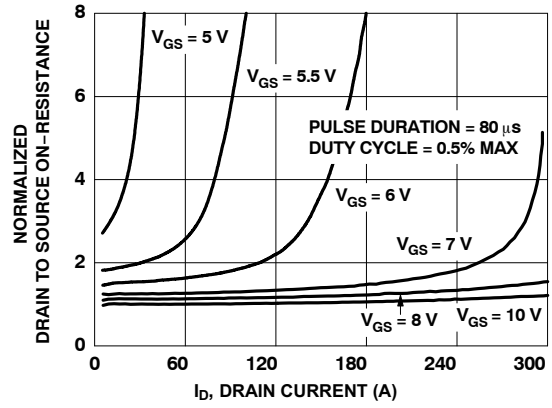


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

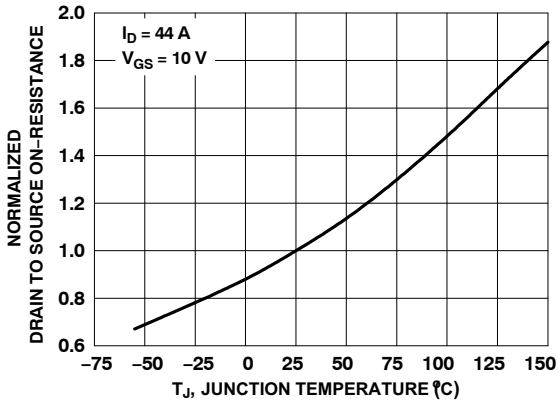


Figure 3. Normalized On Resistance vs. Junction Temperature

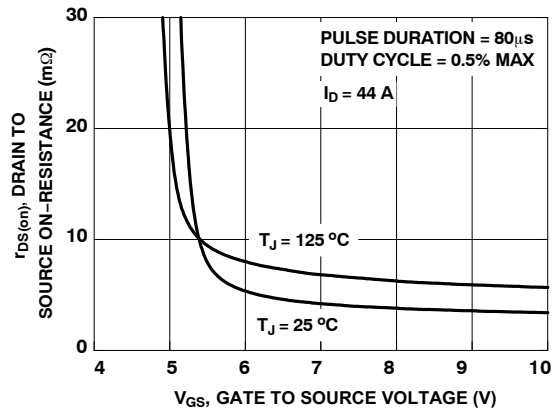


Figure 4. On-Resistance vs. Gate to Source Voltage

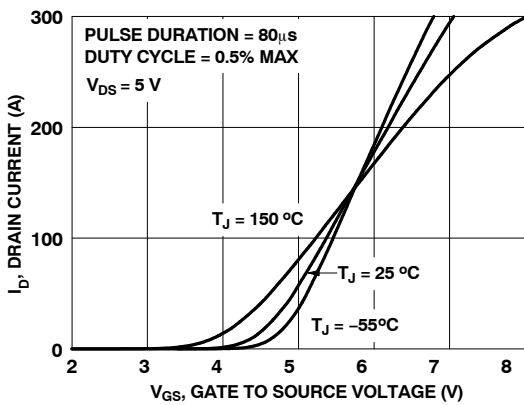


Figure 5. Transfer Characteristics

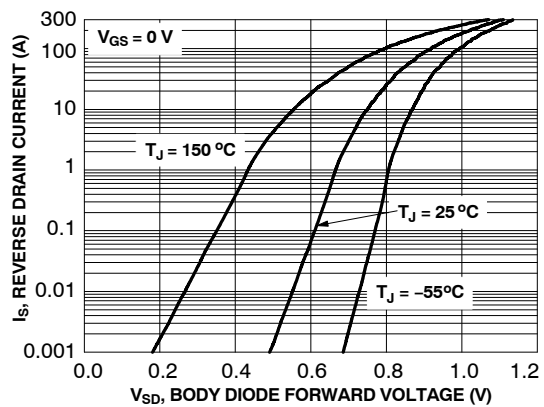


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS (continued)

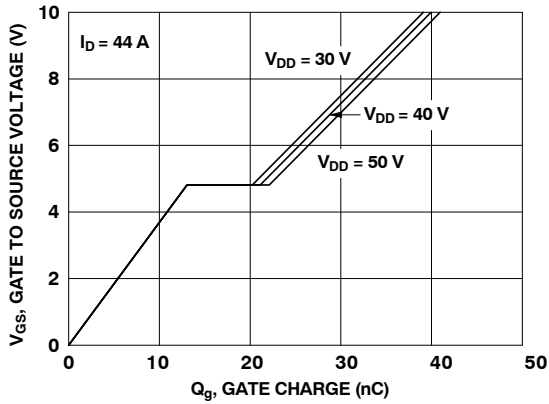


Figure 7. Gate Charge Characteristics

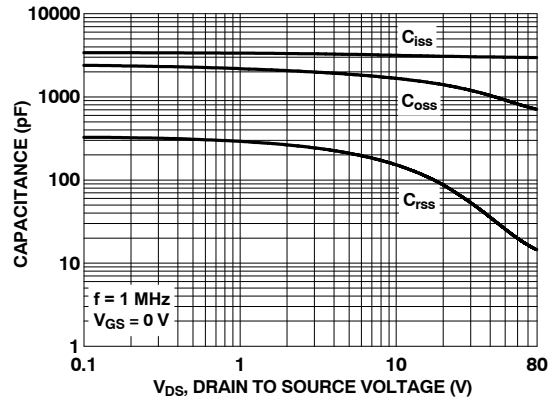


Figure 8. Capacitance vs. Drain to Source Voltage

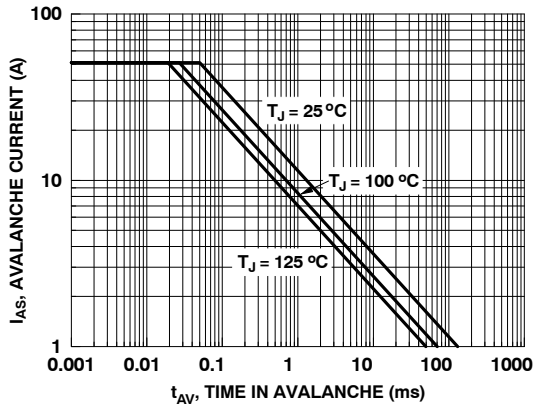


Figure 9. Unclamped Inductive Switching Capability

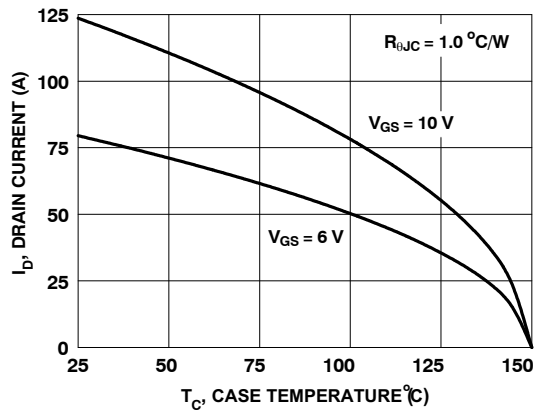


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

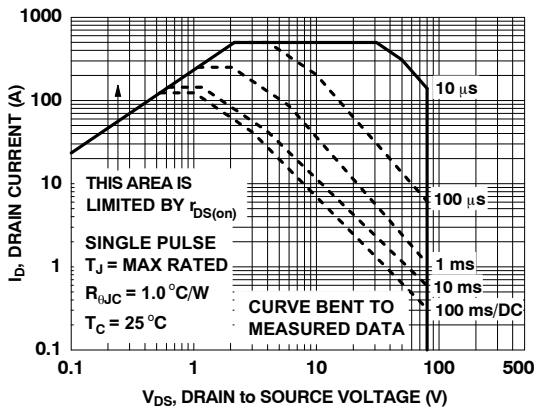


Figure 11. Forward Bias Safe Operating Area

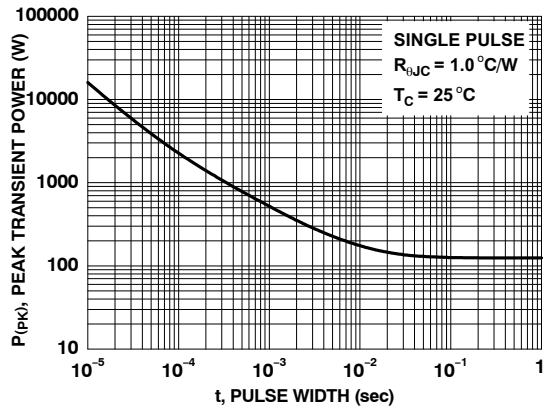


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (continued)

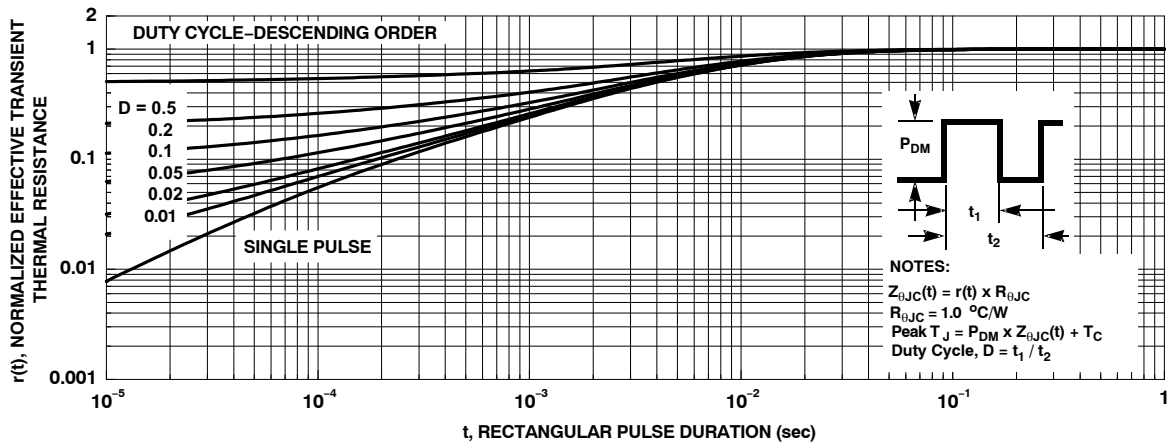
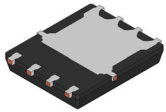


Figure 13. Junction-to-Case Transient Thermal Response Curve

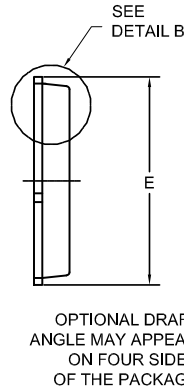
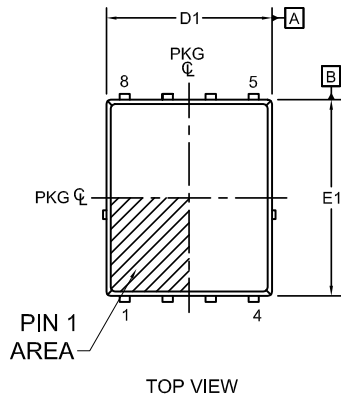
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



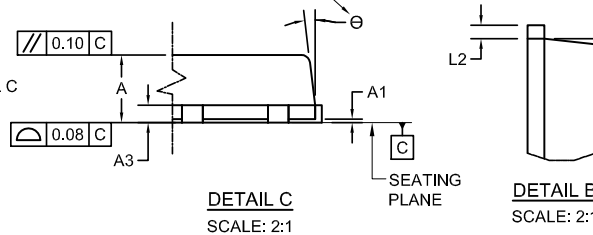
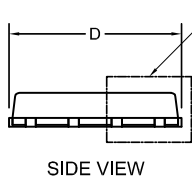
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CASE 483AE
ISSUE C

DATE 21 JAN 2022

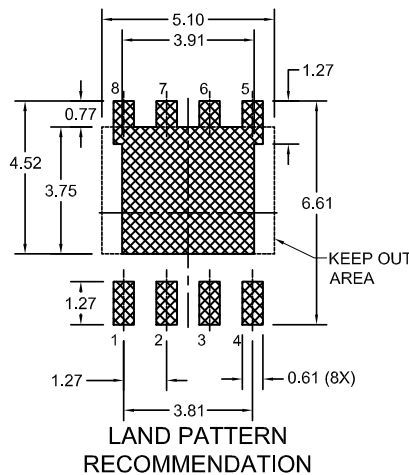
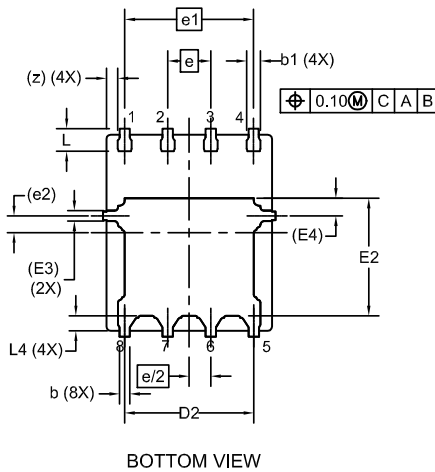


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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