FDMS1D2N03DSD

POWERTRENCH® Power Clip 30 V Asymmetric Dual N-Channel MOSFETs

ON Semiconductor®

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General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $R_{DS(on)}$ = 3.25 mΩ at V_{GS} = 10 V, I_D = 19 A
- Max $R_{DS(on)}$ = 4 mΩ at V_{GS} = 4.5 V, I_D = 17 A

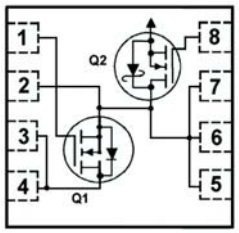
Q2: N-Channel

- Max $R_{DS(on)}$ = 0.97 mΩ at V_{GS} = 10 V, I_D = 37 A
- Max $R_{DS(on)}$ = 1.25 mΩ at V_{GS} = 4.5 V, I_D = 34 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses.
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing.
- RoHS Compliant

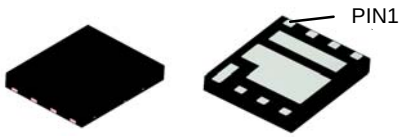
Applications

- Computing
- Communications
- General Purpose Point of Load

ELECTRICAL CONNECTION



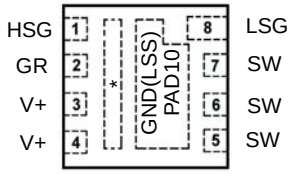
N-Channel MOSFET



Top View Bottom View

Power Clip 56
(PQFN8 5x6)
CASE 483AR

PIN ASSIGNMENT



*PAD9 V+(HSD)

MARKING DIAGRAM

$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMS1D2N03DSD	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Q1	Q2	Unit
V_{DS}	Drain to Source Voltage	30	30	V
V_{GS}	Gate to Source Voltage	+16/−12	+16/−12	V
I_D	Drain Current − Continuous (T_C = 25°C) (Note 5)	70	164	A
	− Continuous (T_C = 85°C) (Note 5)	54	126	
	− Continuous (T_A = 25°C)	19 (Note 1a)	37 (Note 1b)	
	− Continuous (T_A = 85°C)	15 (Note 1a)	29 (Note 1b)	
	− Pulsed (T_A = 25°C) (Note 4)	362	1199	
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	121	337	mJ
P_D	Power Dissipation for Single Operation (T_C = 25°C) (T_A = 25°C)	26 2.1 (Note 1a)	42 2.3 (Note 1b)	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.8	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 (Note 1a)	55 (Note 1b)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 (Note 1c)	120 (Note 1d)	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Device	Top Marking	Package	Reel Size	Tape Width	Quantity
FDMS1D2N03DSD	FDMS1D2N03DSD	Power Clip 56 (PGFN8) (Pb-Free / Halogen Free)	13″	12 mm	3,000 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30	− −	− −	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C	Q1 Q2	− −	15 21	− −	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2	− −	− −	1 500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = +16 V/−12 V, V_{DS}= 0 V	Q1 Q2	− −	− −	±100 ±100	nA nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 320 μA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	0.8 1.0	1.3 1.5	2.5 3.0	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 1 mA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2	− −	−3 −3	− −	mV/°C

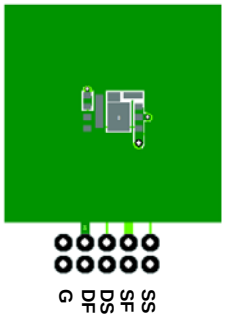
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
ON CHARACTERISTICS							
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 19 A V_{GS} = 4.5 V, I_D = 17 A V_{GS} = 10 V, I_D = 19 A, T_J =125°C	Q1	– – –	2.5 3.0 3.6	3.25 4.0 4.9	mΩ
		V_{GS} = 10 V, I_D = 37 A V_{GS} = 4.5 V, I_D = 34 A V_{GS} = 10 V, I_D = 37 A, T_J =125°C	Q2	– – –	0.73 0.93 1.1	0.97 1.25 1.6	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 19 A V_{DS} = 5 V, I_D = 37 A	Q1 Q2	– –	95 247	– –	S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2	– –	1410 4860	– –	pF
C_{oss}	Output Capacitance		Q1 Q2	– –	564 1845	– –	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	40 123	– –	pF
R_g	Gate Resistance		Q1 Q2	– –	0.3 0.3	– –	Ω
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 15 V, I_D = 19 A, R_{GEN} = 6 Ω Q2: V_{DD} = 15 V, I_D = 37 A, R_{GEN} = 6 Ω	Q1 Q2	– –	8 13	– –	ns
t_r	Rise Time		Q1 Q2	– –	2 5	– –	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2	– –	22 37	– –	ns
t_f	Fall Time		Q1 Q2	– –	2 4	– –	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V Q1: V_{DD} = 15 V, I_D = 19 A Q2: V_{DD} = 15 V, I_D = 37 A	Q1 Q2	– –	23 84	33 117	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V Q1: V_{DD} = 15 V, I_D = 19 A Q2: V_{DD} = 15 V, I_D = 37 A	Q1 Q2	– –	11 39	15 54	nC
Q_{gs}	Gate to Source Gate Charge	Q1: V_{DD} = 15 V, I_D = 19 A Q2: V_{DD} = 15 V, I_D = 37 A	Q1 Q2	– –	3.1 13	– –	nC
Q_{gd}	Gate to Drain “Miller” Charge	Q1: V_{DD} = 15 V, I_D = 19 A Q2: V_{DD} = 15 V, I_D = 37 A	Q1 Q2	– –	2.5 9	– –	nC
SOURCE-DRAIN DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 19 A (Note 2) V_{GS} = 0 V, I_S = 37 A (Note 2)	Q1 Q2	– –	0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1: I_F = 19 A, di/dt = 100 A/μs Q2: I_F = 37 A, di/dt = 300 A/μs	Q1 Q2	– –	28 43	– –	ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2	– –	12 63	– –	nC

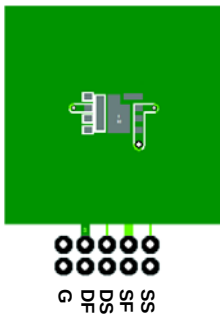
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

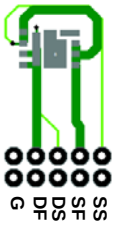
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



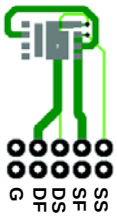
a) 60°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 55°C/W when mounted on a 1 in^2 pad of 2 oz copper.



c) 130°C/W when mounted on a minimum pad of 2 oz copper.



d) 120°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1: E_{AS} of 121 mJ is based on starting T_J = 25°C; N-ch: L = 3 mH, I_{AS} = 9 A, V_{DD} = 30 V. 100% tested at L = 0.1 mH, I_{AS} = 29 A.
   Q2: E_{AS} of 337 mJ is based on starting T_J = 25°C; N-ch: L = 3 mH, I_{AS} = 15 A, V_{DD} = 30 V. 100% tested at L = 0.1 mH, I_{AS} = 47 A.
4. Pulsed Id please refer to Figure 11 and Figure 24 SOA graphs for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS (Q1 N-Channel)

(T_J = 25°C unless otherwise noted)

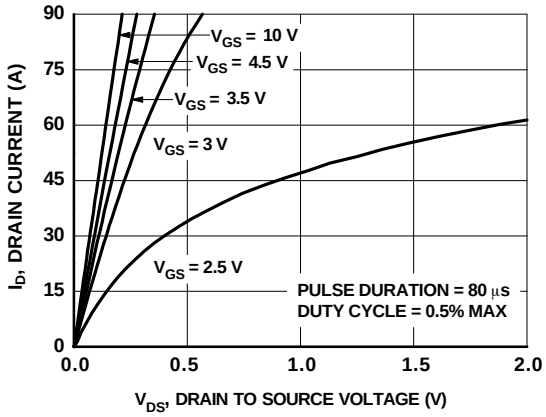


Figure 1. On-Region Characteristics

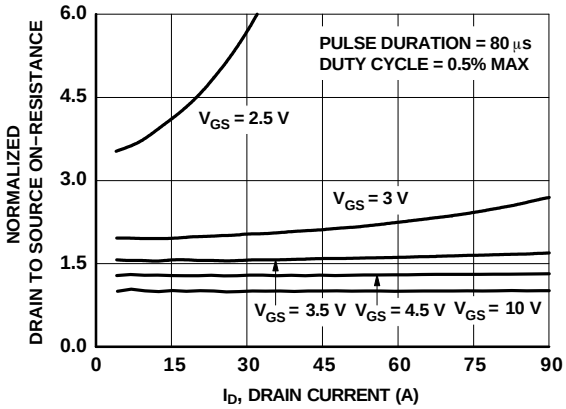


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

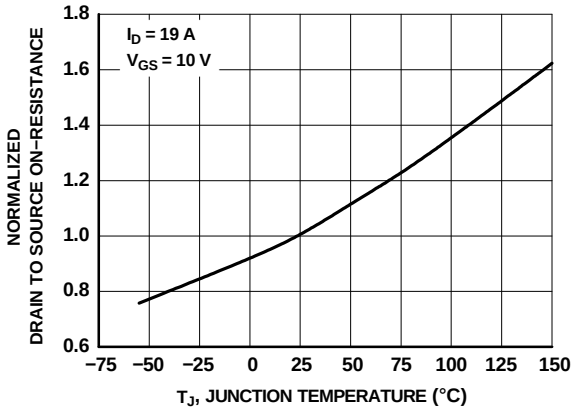


Figure 3. Normalized On-Resistance vs. Junction Temperature

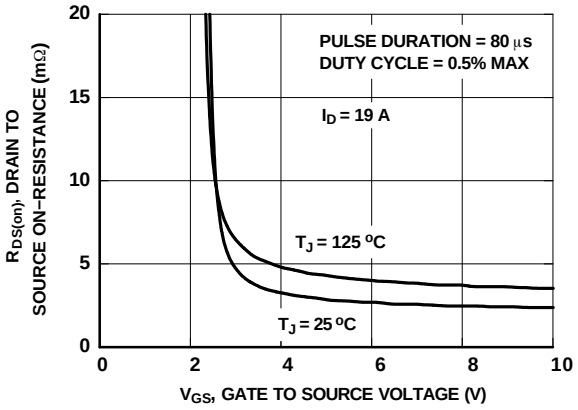


Figure 4. On-Resistance vs. Gate to Source Voltage

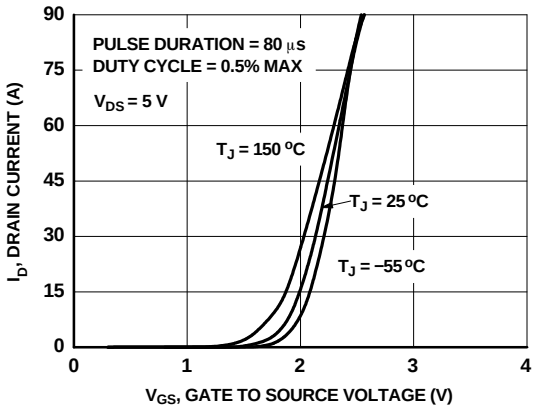


Figure 5. Transfer Characteristics

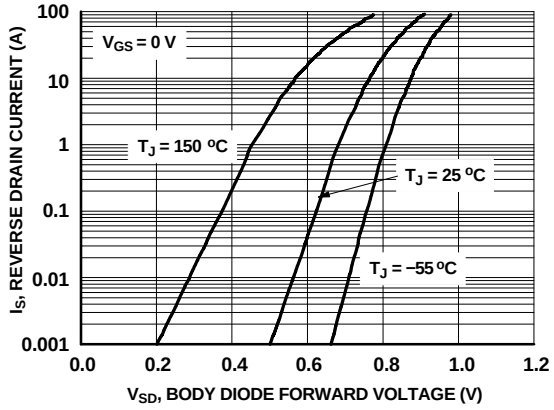


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-Channel)

(T_J = 25°C unless otherwise noted)

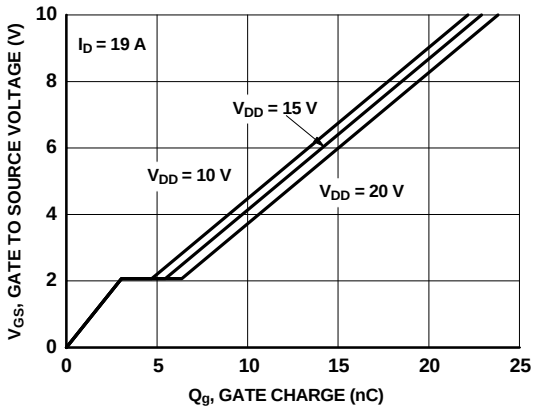


Figure 7. Gate Charge Characteristics

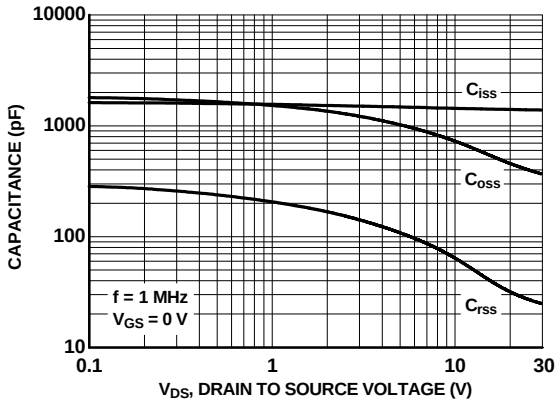


Figure 8. Capacitance vs. Drain to Source Voltage

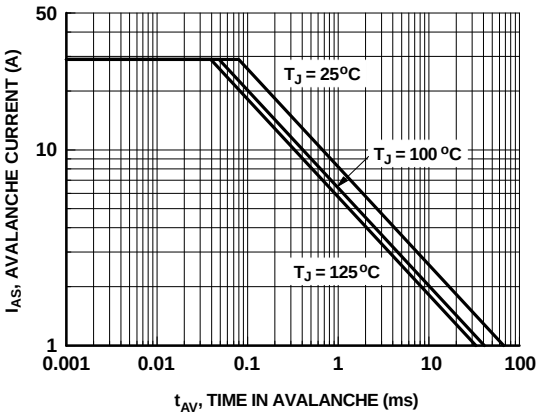


Figure 9. Unclamped Inductive Switching Capability

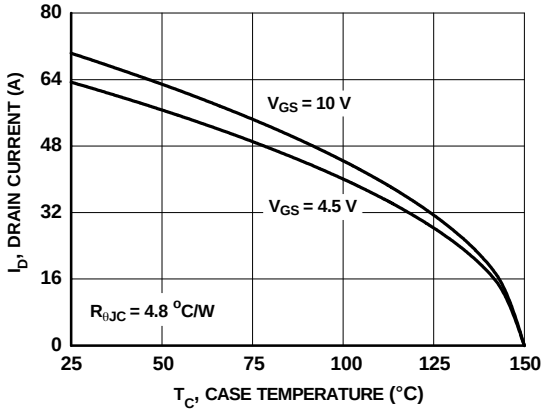


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

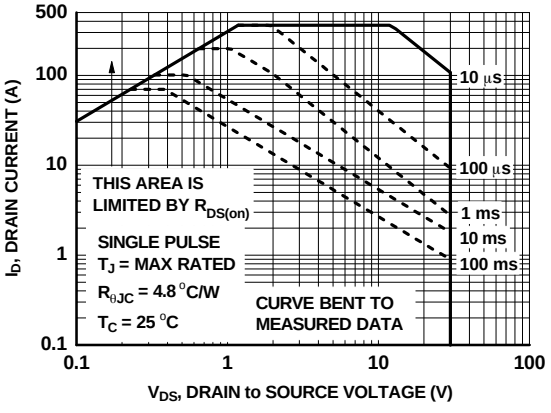


Figure 11. Forward Bias Safe Operating Area

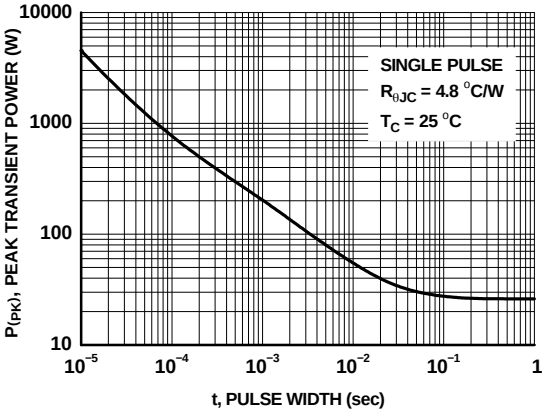


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N-Channel)

(T_J = 25°C unless otherwise noted)

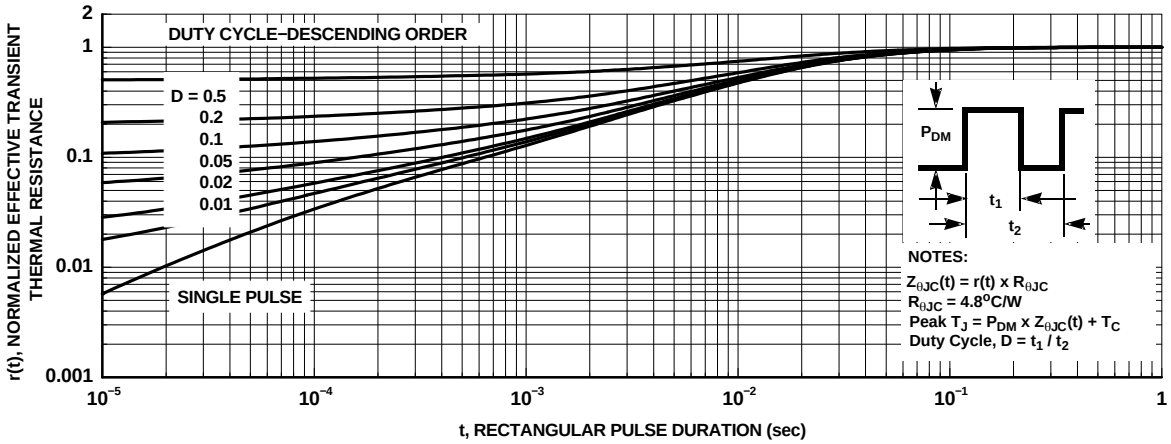


Figure 13. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-Channel)

(T_J = 25°C unless otherwise noted)

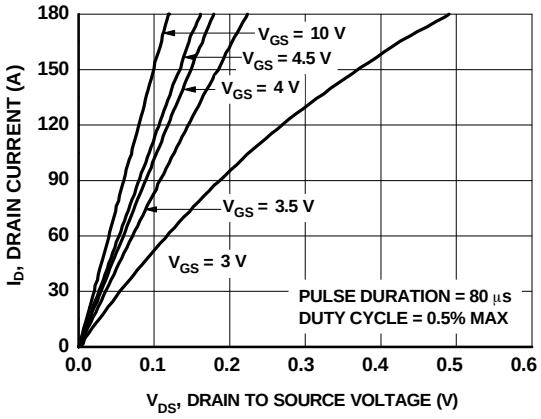


Figure 14. On-Region Characteristics

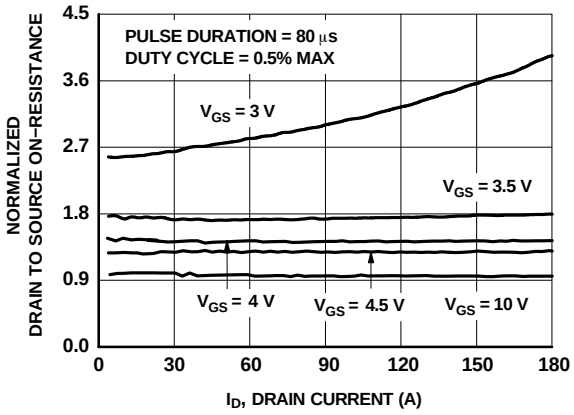


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

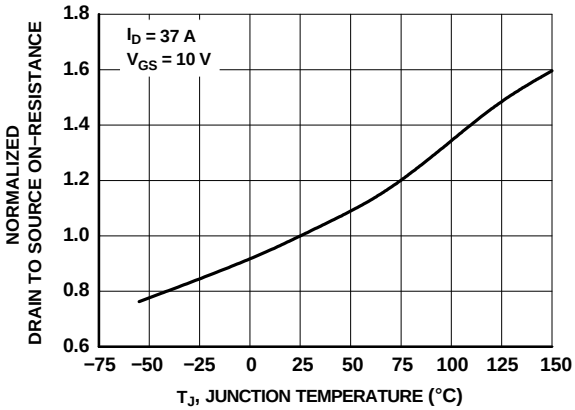


Figure 16. Normalized On-Resistance vs. Junction Temperature

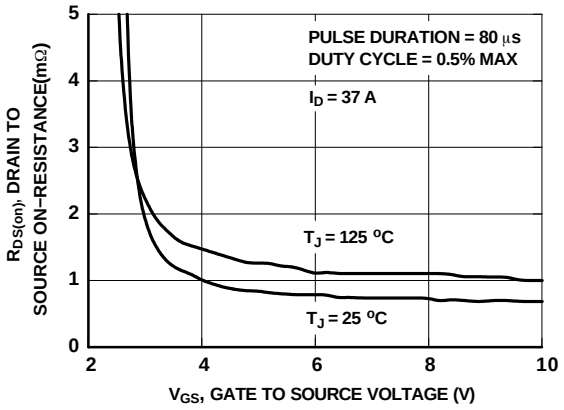


Figure 17. On-Resistance vs. Gate to Source Voltage

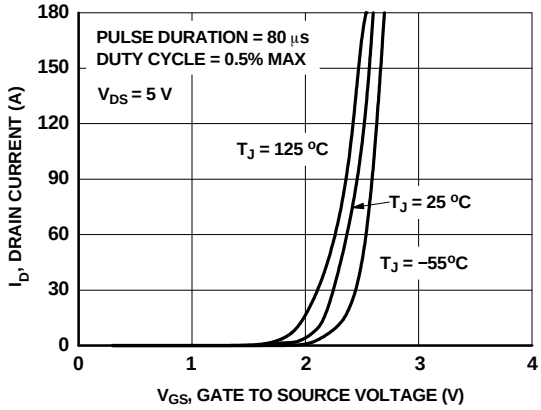


Figure 18. Transfer Characteristics

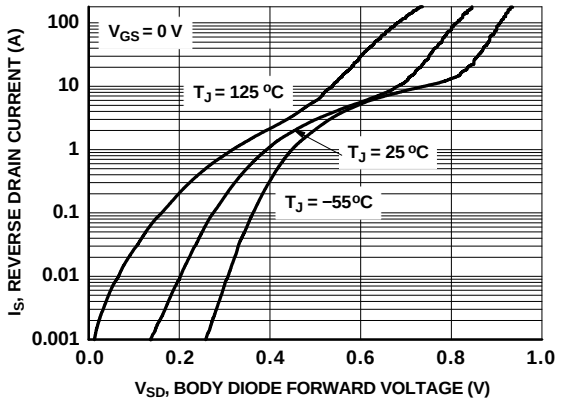


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-Channel)

(T_J = 25°C unless otherwise noted)

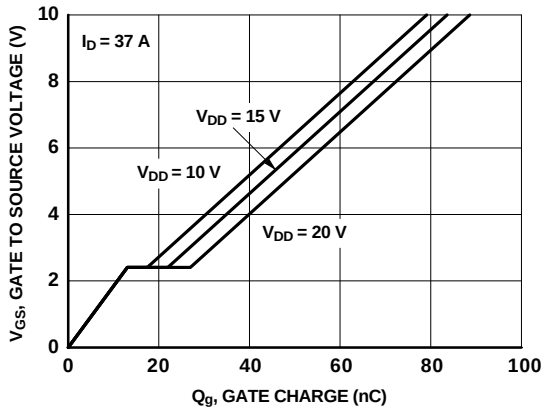


Figure 20. Gate Charge Characteristics

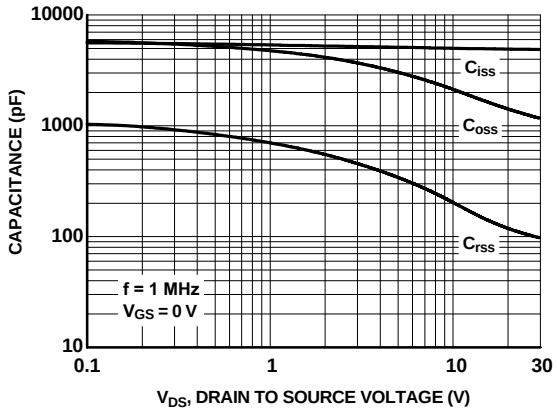


Figure 21. Capacitance vs. Drain to Source Voltage

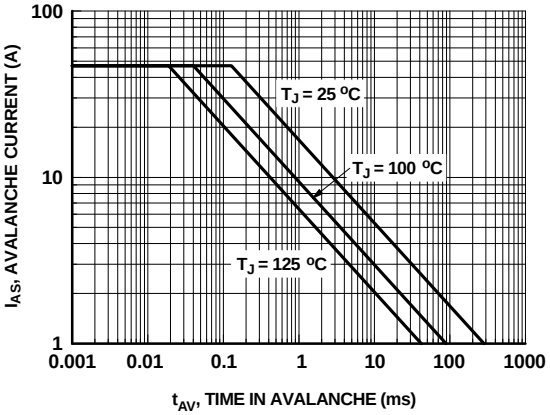


Figure 22. Unclamped Inductive Switching Capability

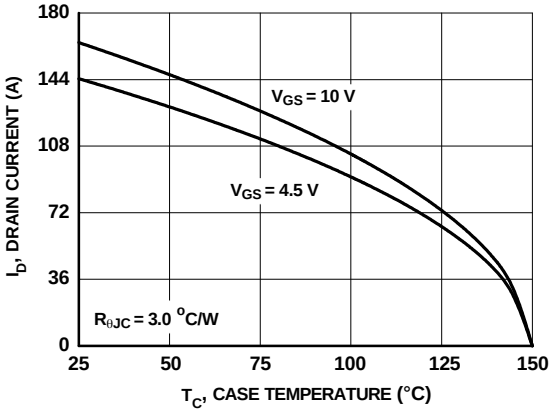


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

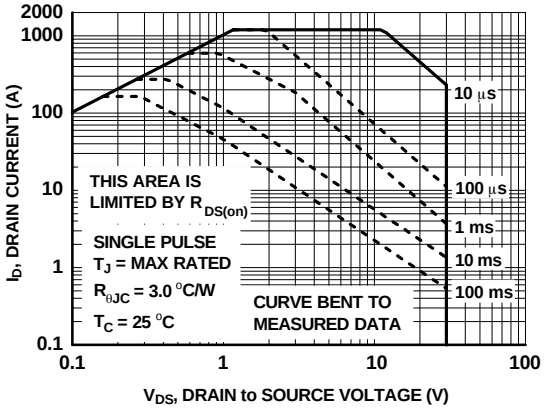


Figure 24. Forward Bias Safe Operating Area

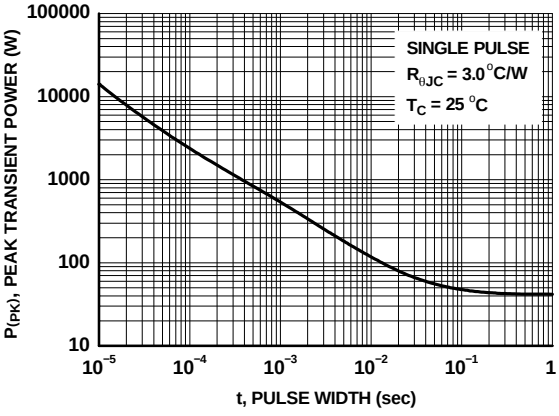


Figure 25. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N-Channel)

(T_J = 25°C unless otherwise noted)

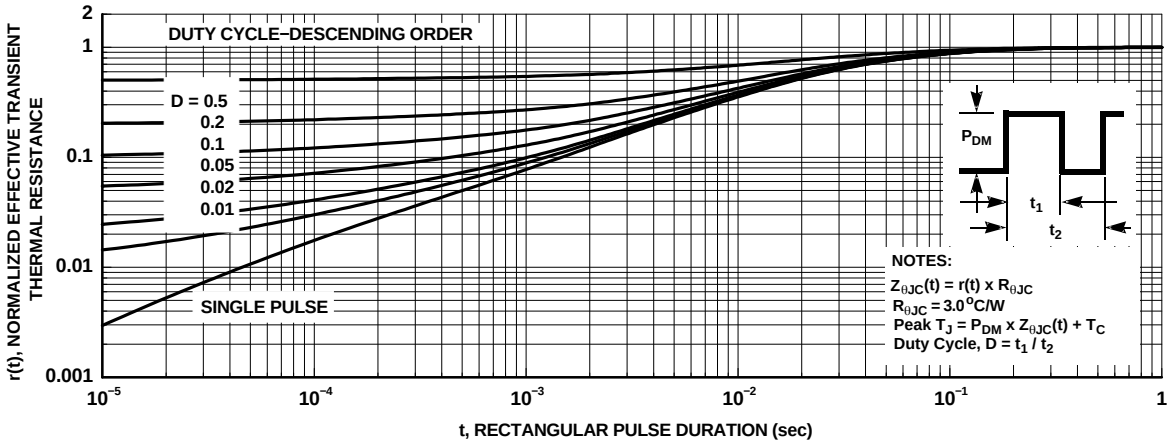


Figure 26. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

ON's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS1D2N03DSD.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

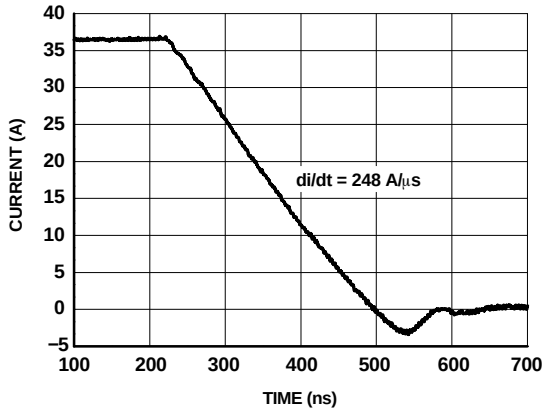


Figure 27. FDMS1D2N03DSD SyncFET Body Diode Reverse Recovery Characteristic

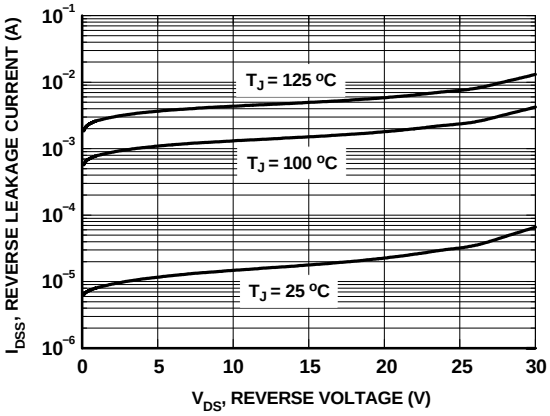
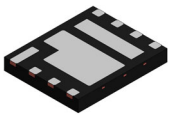


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



PQFN8 5.00x6.00x0.75, 1.27P
CASE 483AR
ISSUE D

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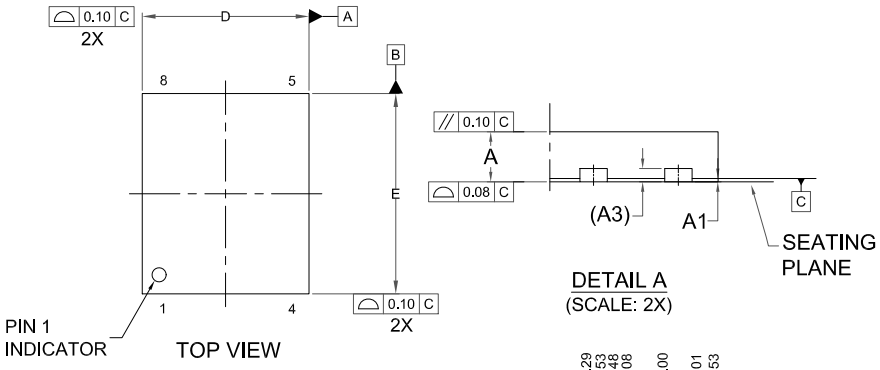

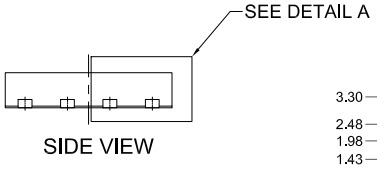

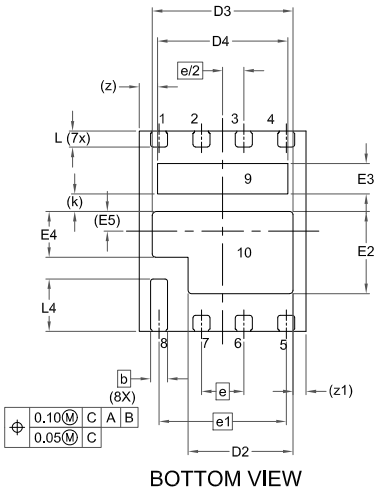

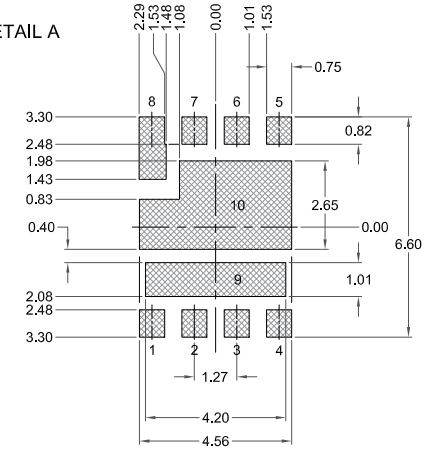

RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20 REF	
b		0.51 BSC	
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
D3	4.12	4.22	4.32
D4	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	2.36	2.46	2.56
E3	0.81	0.91	1.01
E4	1.27	1.37	1.47
E5		0.59 REF	
e		1.27 BSC	
e/2		0.635 BSC	
e1		3.81 BSC	
k		0.52 REF	
L	0.38	0.48	0.58
L4	1.47	1.57	1.67
z		0.55 REF	
z1		0.39 REF	

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