

SyncFET™ – N-Channel, POWERTRENCH®

30 V, 42 A, 4.9 mΩ

FDMS0312S

General Description

The FDMS0312S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Features

- Max $r_{DS(on)}$ = 4.9 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 18\text{ A}$
- Max $r_{DS(on)}$ = 5.8 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 14\text{ A}$
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$ and High Efficiency
- SyncFET Schottky Body Diode
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

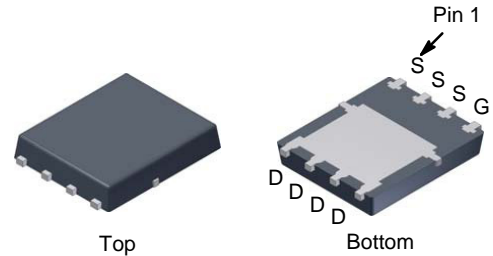
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	± 20	V
I_D	Drain Current		A
	– Continuous (Package Limited) $T_C = 25^\circ\text{C}$	42	
	– Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	83	
	– Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	19	
	– Pulsed	90	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	60	mJ
P_D	Power Dissipation		W
	$T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	46 2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

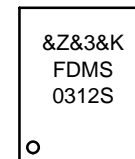
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

V_{DS} MAX	$r_{DS(on)}$ MAX	I_D MAX
30 V	4.9 mΩ @ 10 V	42 A
	5.8 mΩ @ 4.5 V	



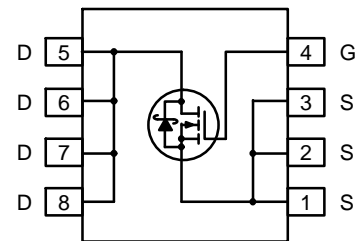
PQFN8 5X6, 1.27P
(Power 56)
CASE 483AE

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code
- &K = 2-Digits Lot Run Code
- FDMS0312S = Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMS0312S

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, referenced to 25°C	–	18	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	500	μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 1 mA	1.2	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 10 mA, referenced to 25°C	–	–5	–	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 18 A	–	3.6	4.9	mΩ
		V _{GS} = 4.5 V, I _D = 14 A	–	4.7	5.8	
		V _{GS} = 10 V, I _D = 18 A, T _J = 125°C	–	5	6.2	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 18 A	–	97	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	–	2120	2820	pF
C _{oss}	Output Capacitance		–	735	975	pF
C _{rss}	Reverse Transfer Capacitance		–	90	135	pF
R _g	Gate Resistance		–	1.1	2.2	Ω

SWITCHING CHARACTERISTICS

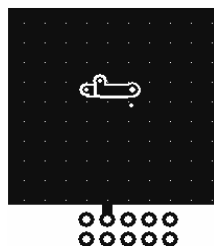
t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 18 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	12	21	ns
t _r	Rise Time		–	5	10	ns
t _{d(off)}	Turn-Off Delay Time		–	28	44	ns
t _f	Fall Time		–	4	10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 15 V, I _D = 18 A	–	33	46	nC
Q _g	Total Gate Charge	V _{GS} = 0 V to 4.5 V, V _{DD} = 15 V, I _D = 18 A	–	15	22	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 15 V, I _D = 18 A	–	6.5	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	4.0	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

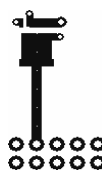
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2 A (Note 2)	–	0.48	0.7	V
		V _{GS} = 0 V, I _S = 18 A (Note 2)	–	0.80	1.2	
t _{rr}	Reverse Recovery Time	I _F = 18 A, di/dt = 300 A/μs	–	26	42	ns
Q _{rr}	Reverse Recovery Charge		–	26	42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R_{θJA} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 50°C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- E_{AS} of 60 mJ is based on starting T_J = 25°C, L = 1 mH, I_{AS} = 11 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 0.3 mH, I_{AS} = 16 A.
- As an N-ch device, the negative V_{gs} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS
($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

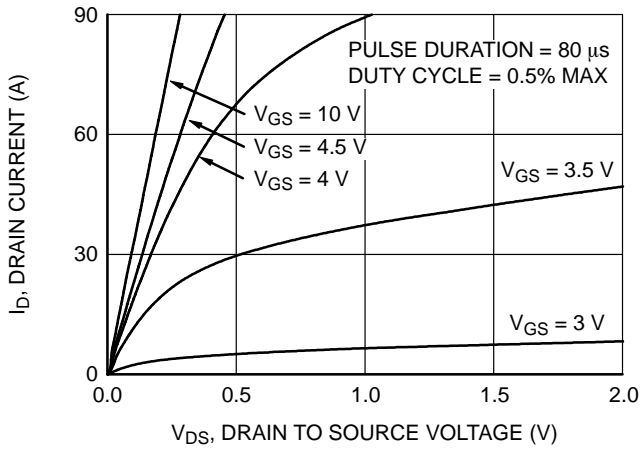


Figure 1. On-Region Characteristics

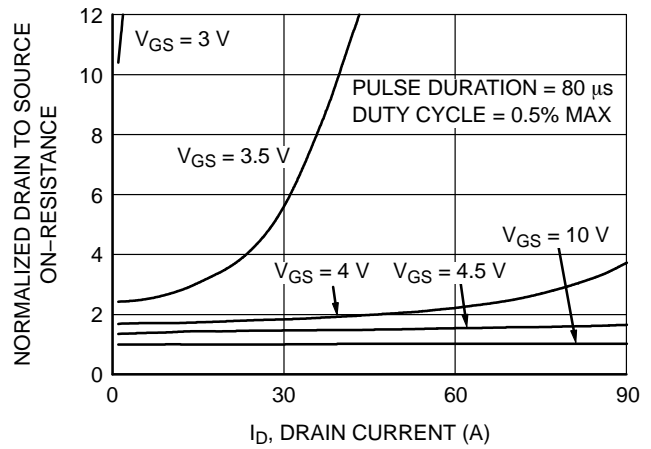


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

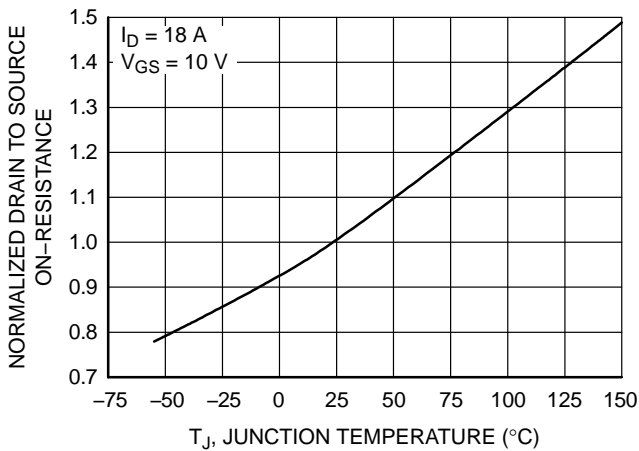


Figure 3. Normalized On-Resistance vs. Junction Temperature

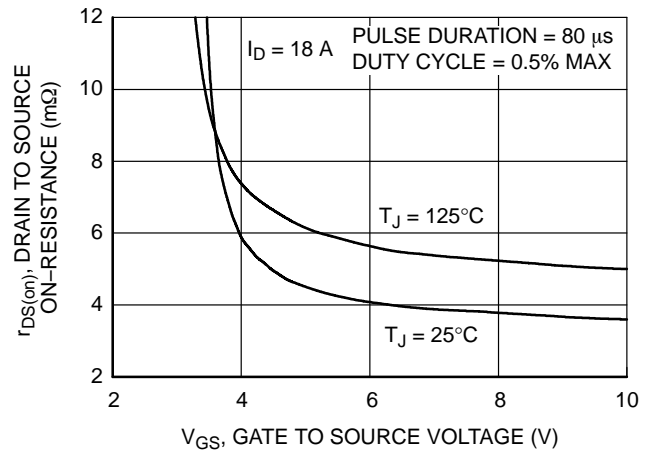


Figure 4. On-Resistance vs. Gate to Source Voltage

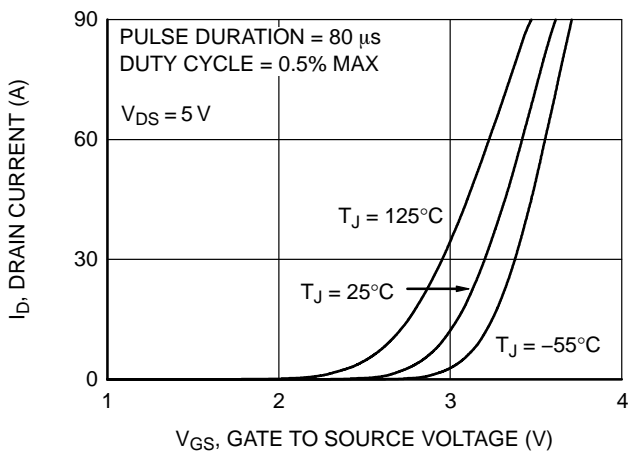


Figure 5. Transfer Characteristics

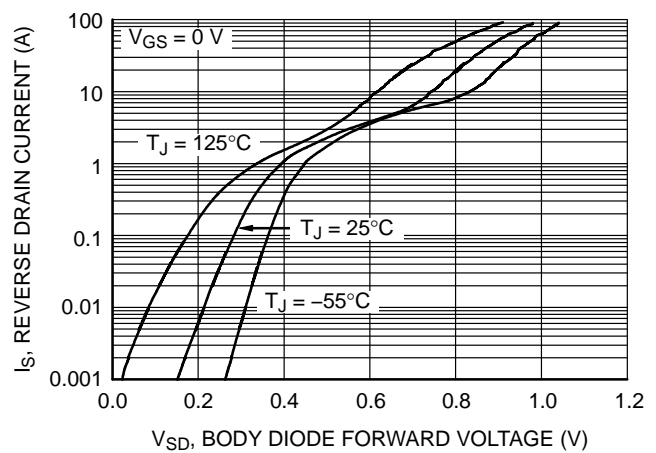


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS
($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) (CONTINUED)

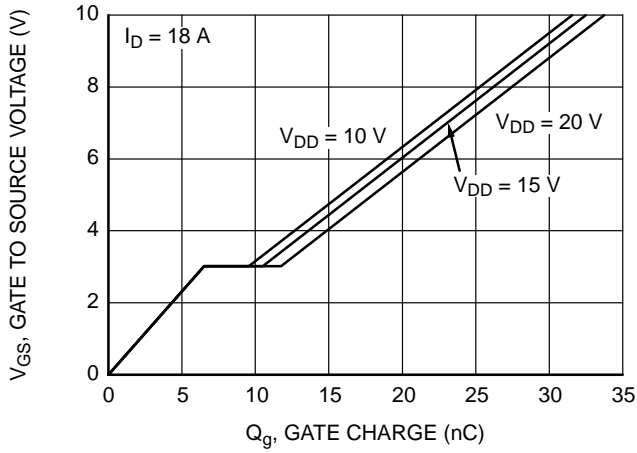


Figure 7. Gate Charge Characteristics

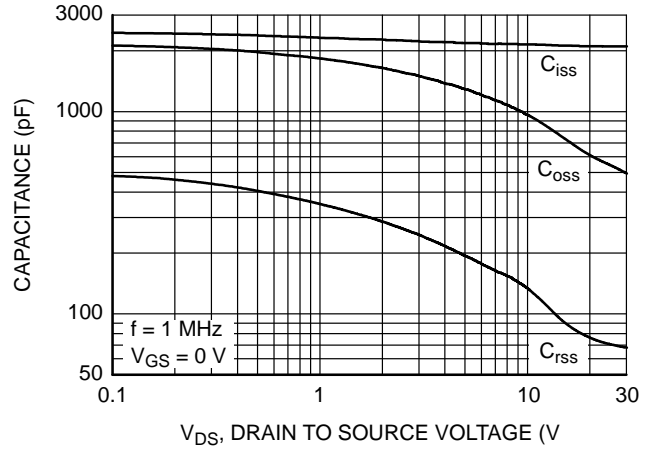


Figure 8. Capacitance vs. Drain to Source Voltage

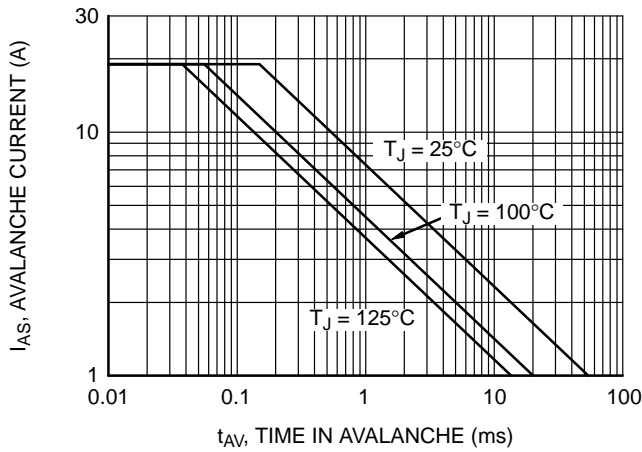


Figure 9. Unclamped Inductive Switching Capability

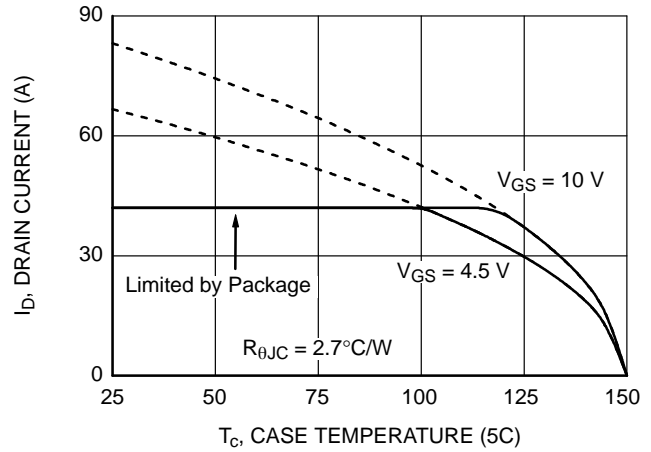


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

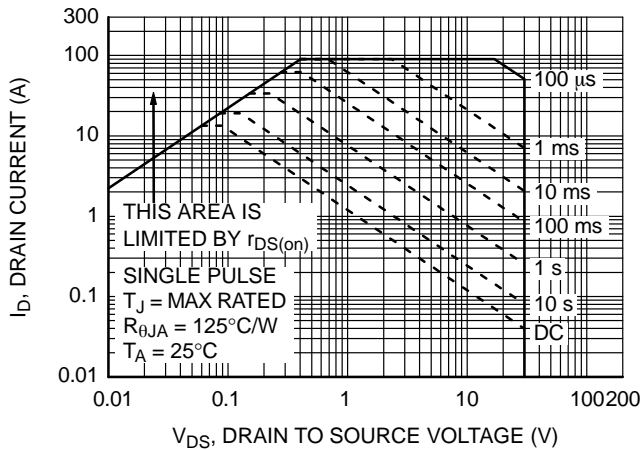


Figure 11. Forward Bias Safe Operating Area

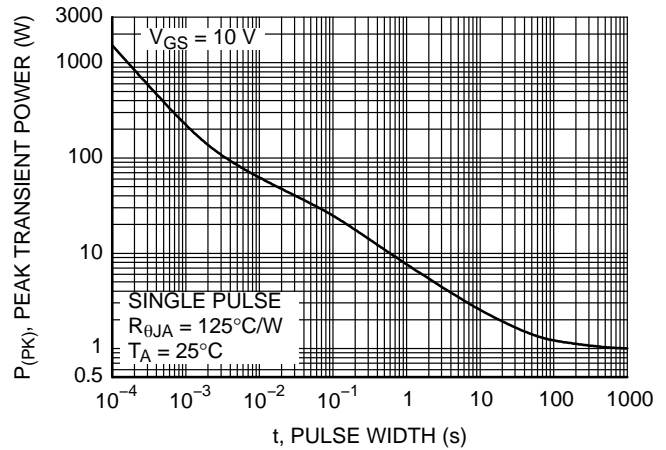


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS
 (T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

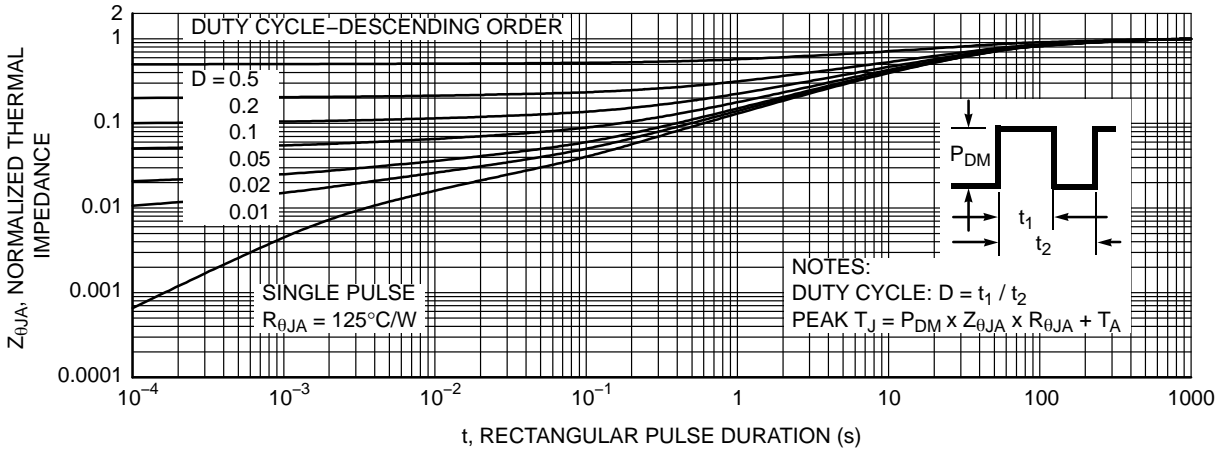


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

FDMS0312S

TYPICAL CHARACTERISTICS (CONTINUED)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS0312S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

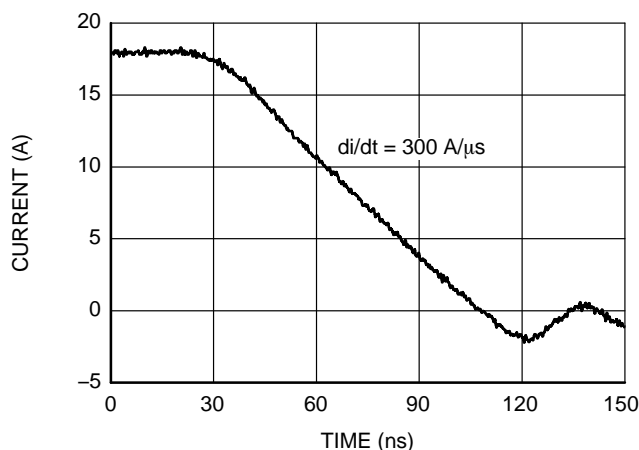


Figure 14. FDMS0312S SyncFET Body Diode Reverse Recovery Characteristic

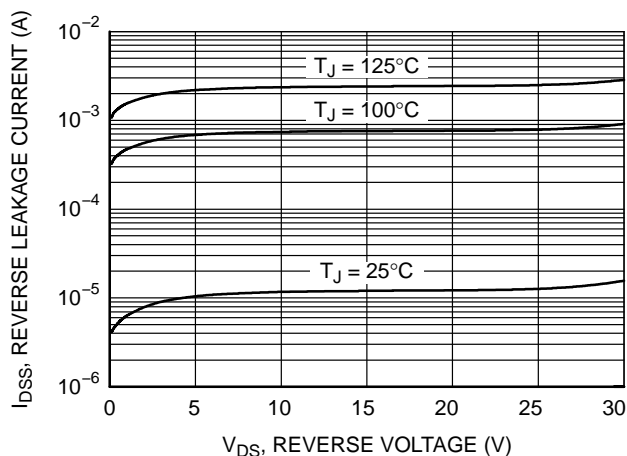


Figure 15. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMS0312S	FDMS0312S	PQFN8 5X6, 1.27P (Power 56) (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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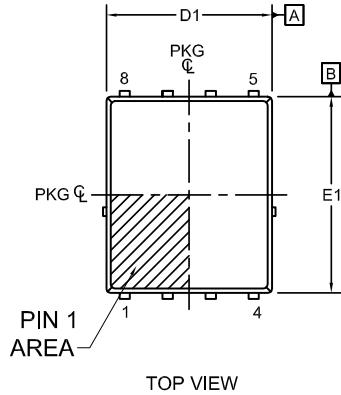
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



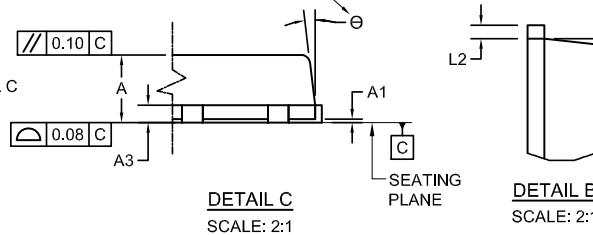
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

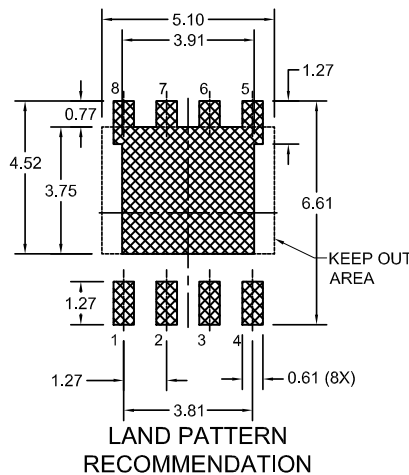
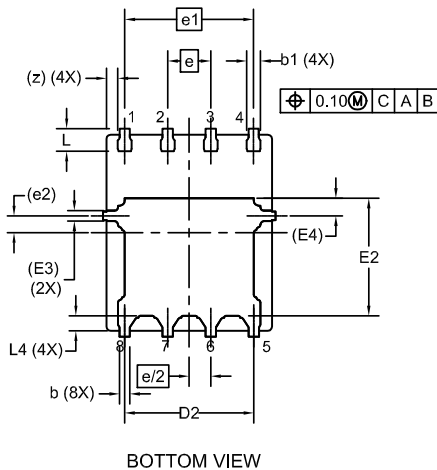


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	PQFN8 5X6, 1.27P	PAGE 1 OF 1

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