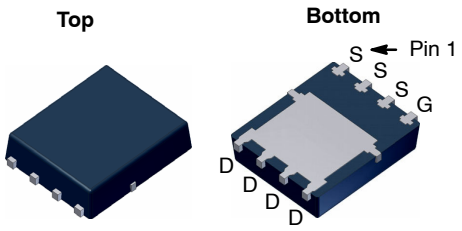
MOSFET – N-Channel, POWERTRENCH®

60 V, 100 A, 3 Ω

FDMS030N06B



PQFN8 5 × 6, 1.27P
(Power 56)
CASE 483AE

Description

This N−Channel MOSFET is produced using **onsemi**'s advance POWERTRENCH process that has been tailored to minimize the on−state resistance while maintaining superior switching performance.

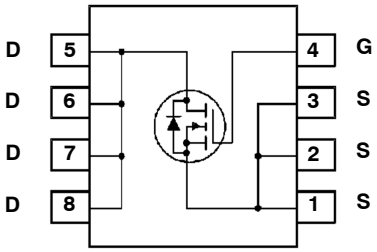
Features

- $R_{DS(on)}$ = 2.4 m (Typ) at V_{GS} = 10 V, I_D = 50 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies
- Renewable system

PIN CONNECTIONS



MARKING DIAGRAM

&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digit Lot Run Traceability Code
FDMS030N06B	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMS030N06B	PQFN8 (Pb−Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter			FDMS030N06B	Unit
V_{DSS}	Drain to Source Voltage			60	V
V_{GSS}	Gate to Source Voltage			±20	V
I_D	Drain Current	Continuous (Note 1)	T_C = 25°C	100	A
		Continuous (Note 2a)	T_A = 25°C	22.1	
I_{DM}	Drain Current	Pulsed (Note 3)		400	
E_{AS}	Single Pulse Avalanche Energy (Note 4)			248	mJ
P_D	Power Dissipation		T_C = 25°C	104	W
			T_A = 25°C (Note 2a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDMS030N06B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max (Note 2a)	50	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

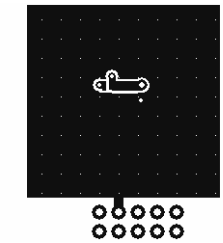
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.03	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	3.3	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 50 A	–	2.4	3.0	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 50 A	–	119	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	–	5685	7560	pF
C_{oss}	Output Capacitance		–	1720	2290	pF
C_{rss}	Reverse Transfer Capacitance		–	59	–	pF
C_{oss}(er)	Engry Releted Output Capacitance	V_{DS} = 30 V, V_{GS} = 0 V	–	2504	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 30 V, I_D = 50 A V_{GS} = 0 V to 10 V (Note 5)	–	75	–	nC
Q_{gs}	Gate to Source Gate Charge		–	30	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	14	–	nC
$V_{plateau}$	Gate Plateau Voltage		–	5.4	–	V
Q_{sync}	Total Gate Charge Sync	V_{DS} = 0 V, I_D = 50 A	–	66.2		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V	–	174	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.05	–	Ω

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 50 A, V_{GS} = 10 V, R_{GEN} = 4.7 Ω (Note 5)	–	39	88	ns
t_r	Turn-On Rise Time		–	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		–	52	114	ns
t_f	Turn-Off Fall Time		–	16	42	ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	100	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	400	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 50 A	–	–	1.25	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 50 A, dI_F/dt = 100 A/μs	–	71	–	ns
Q_{rr}	Reverse Recovery Charge		–	85	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Silicon limited I_D rating = 147 A.
2. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.

b) 125°C/W when mounted on a minimum pad of 2 oz copper.

3. Repetitive rating: pulse−width limited by maximum junction temperature.
4. L = 0.3 mH, I_{AS} = 40 A, V_{DD} = 50 V, V_{GS} = 10 V, starting T_J = 25°C.
5. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

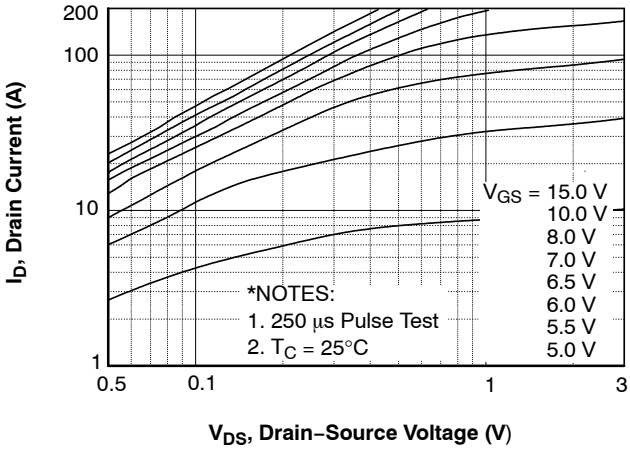


Figure 1. On−Region Characteristics

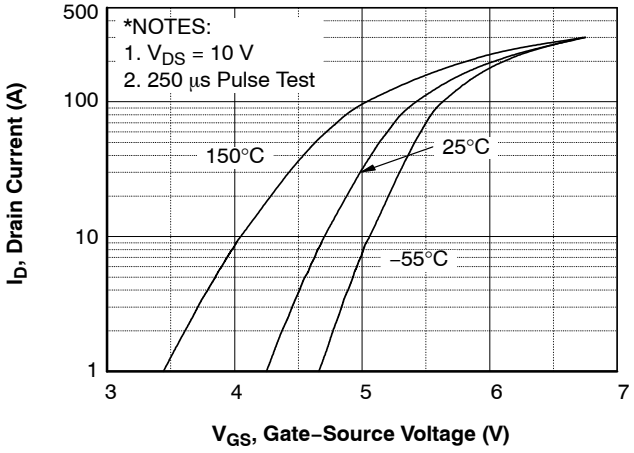


Figure 2. Transfer Characteristics

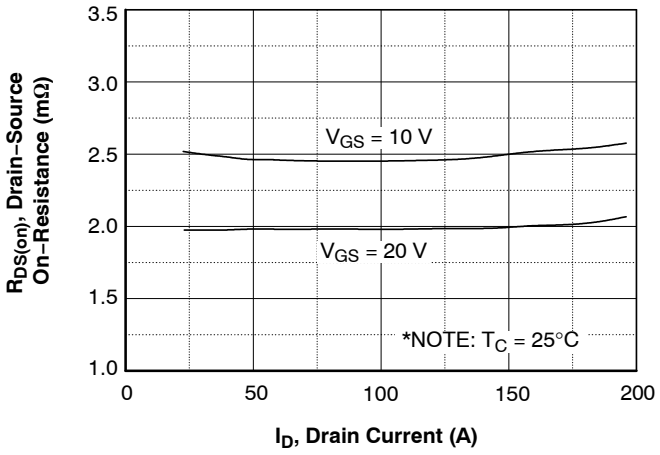


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

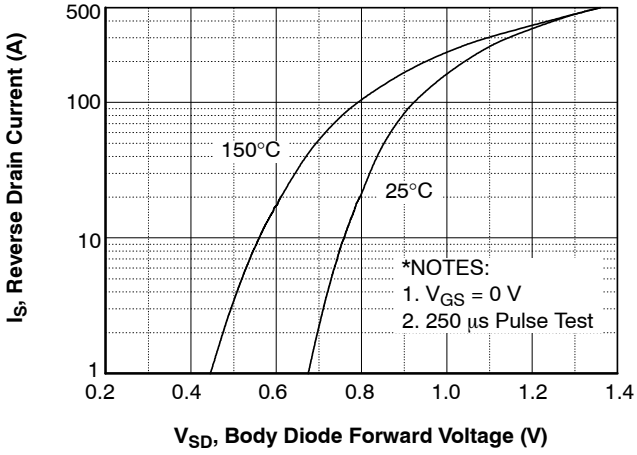


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

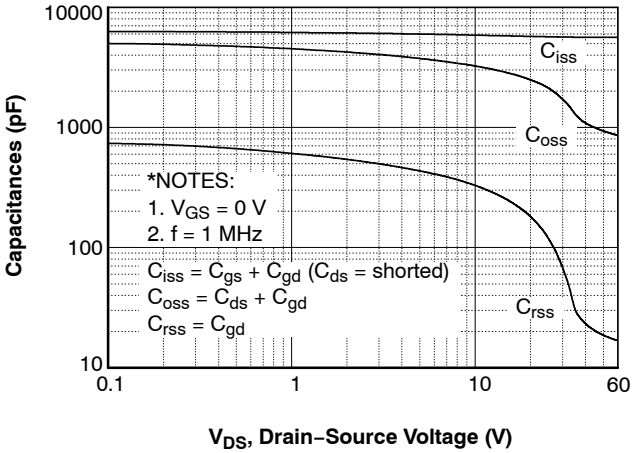


Figure 5. Capacitance Characteristics

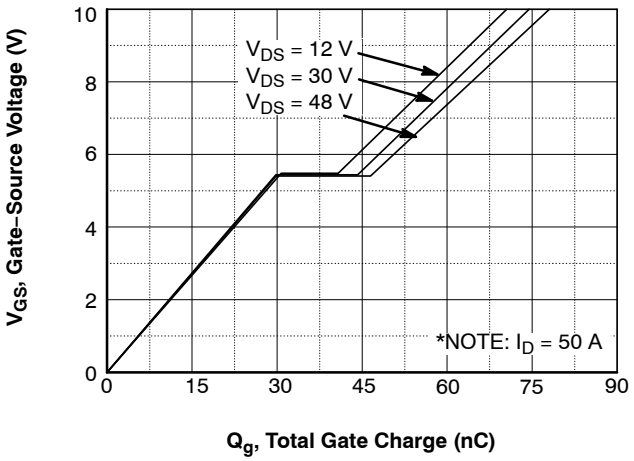


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

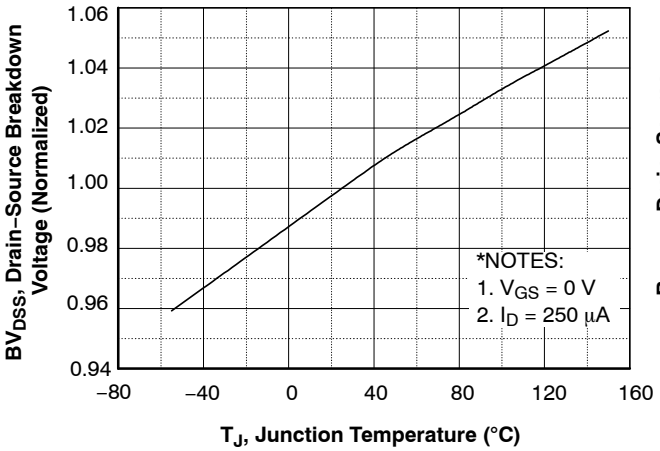


Figure 7. Breakdown Voltage Variation vs. Temperature

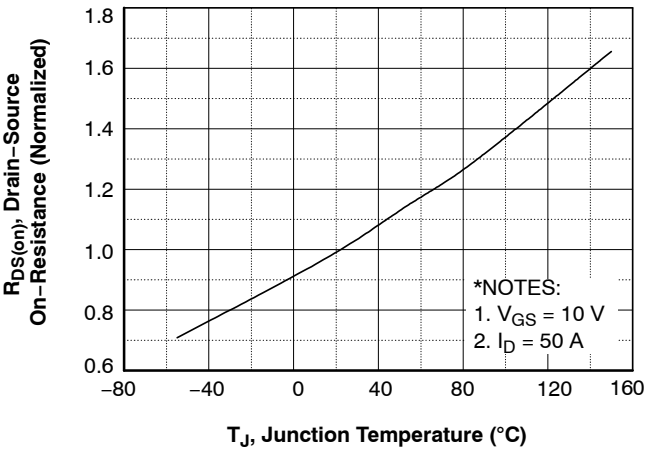


Figure 8. On−Resistance Variation vs. Temperature

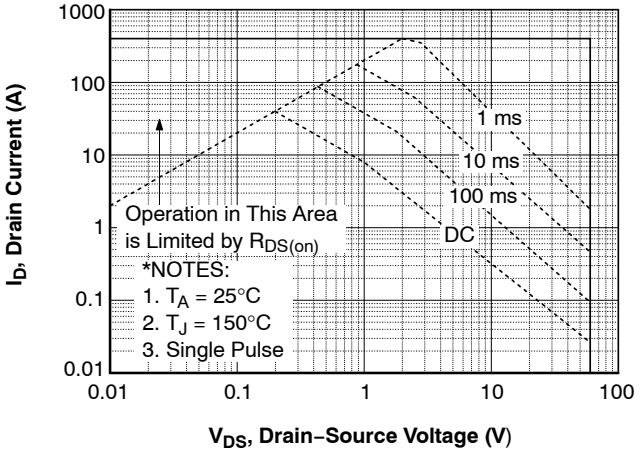


Figure 9. Maximum Safe Operating Area

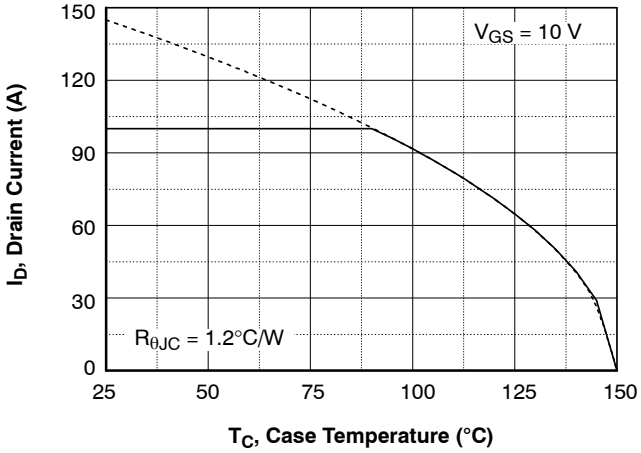


Figure 10. Maximum Drain Current vs. Case Temperature

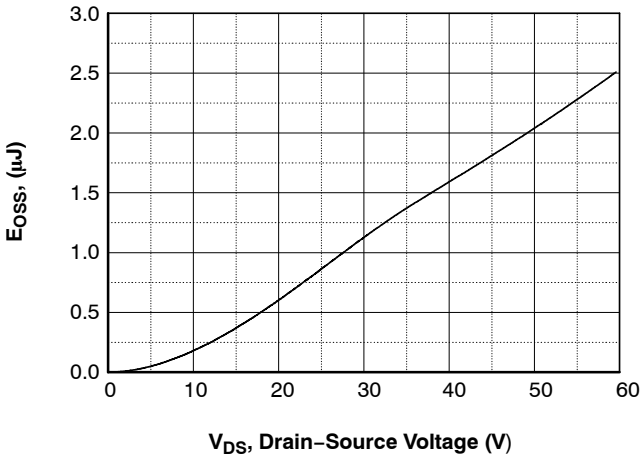


Figure 11. Eoss vs. Drain to Source Voltage

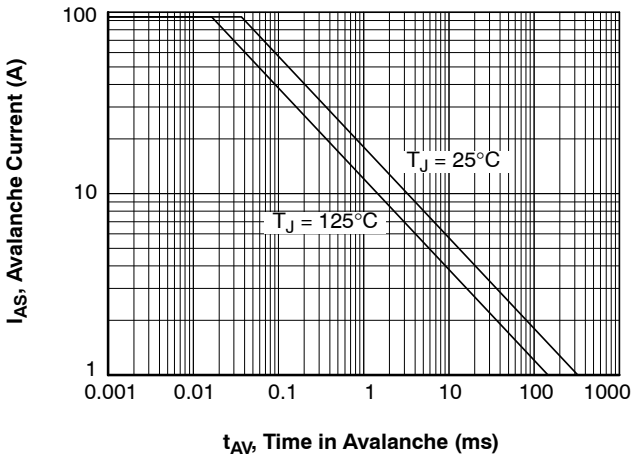


Figure 12. Unclamped Inductive Switching Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

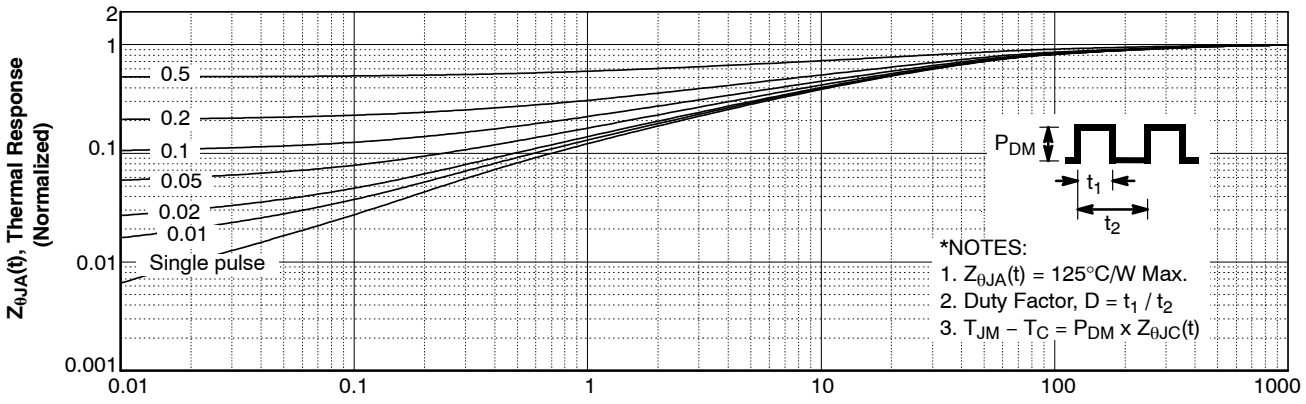


Figure 13. Transient Thermal Response Curve

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

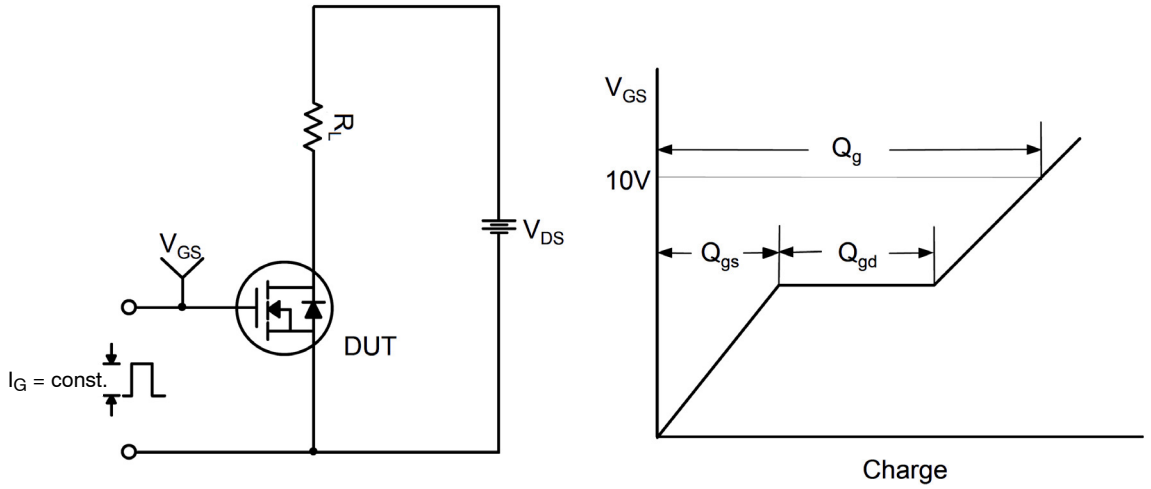


Figure 14. Gate Charge Test Circuit & Waveform

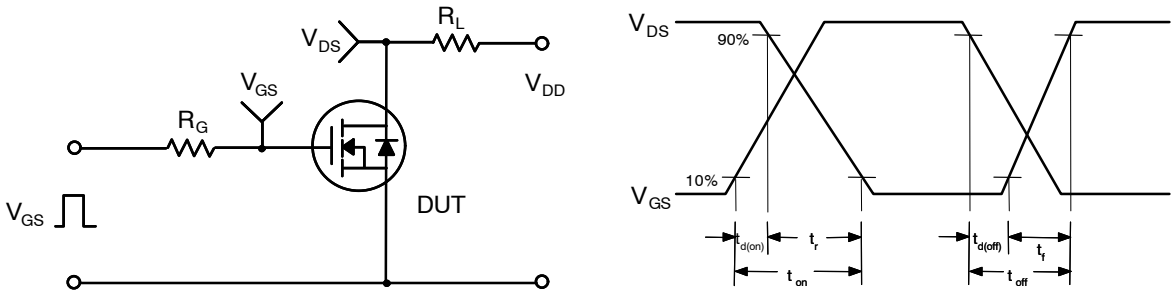


Figure 15. Resistive Switching Test Circuit & Waveforms

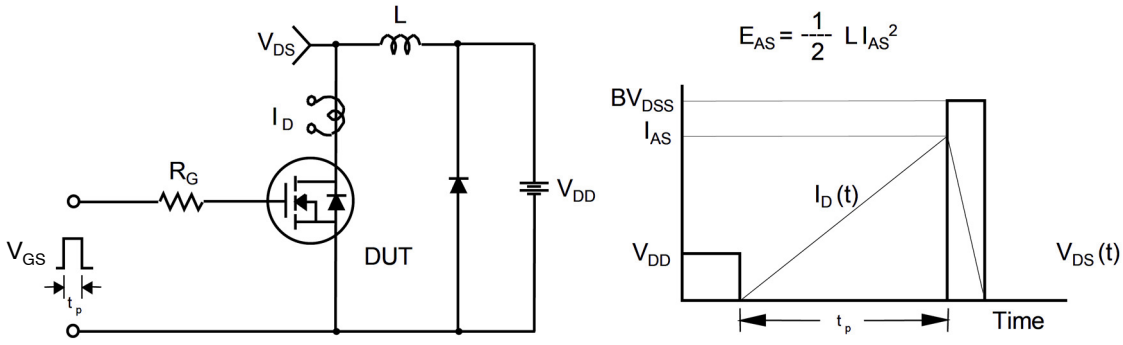


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

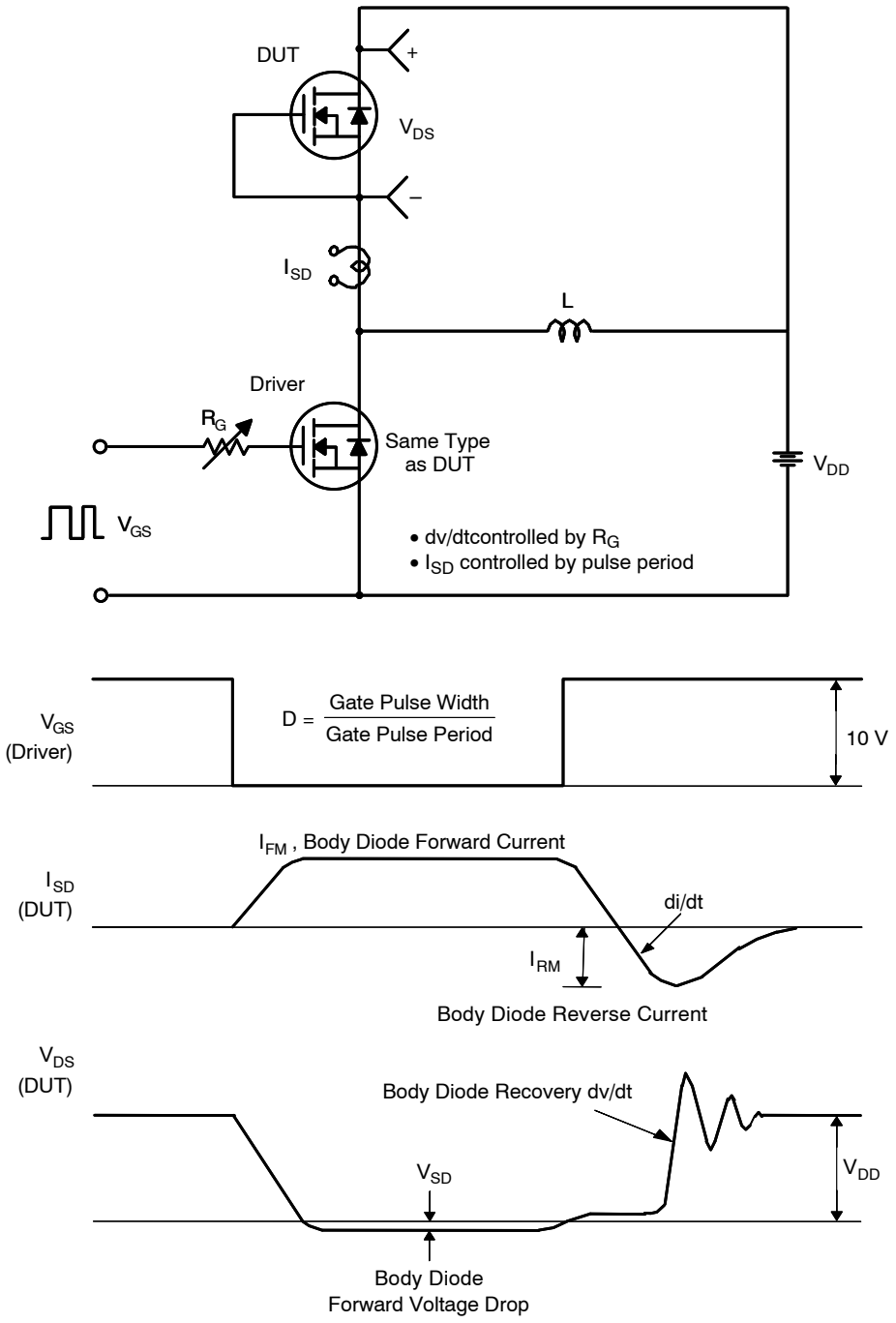


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

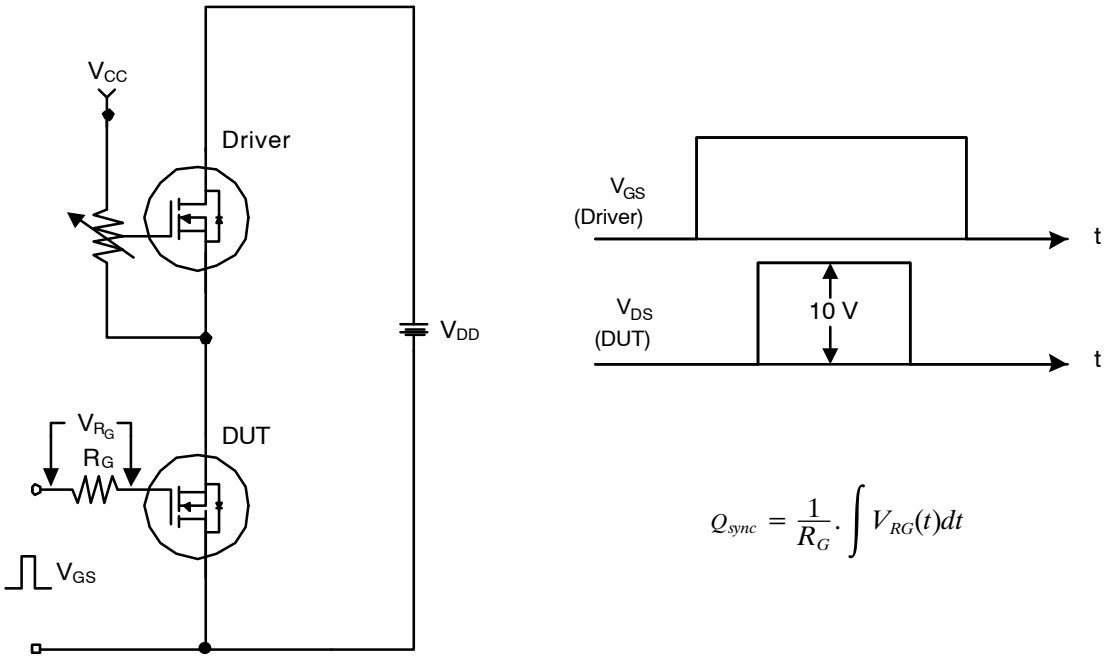


Figure 18. Total Gate Charge Qsync. Test Circuit & Waveforms

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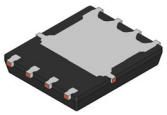

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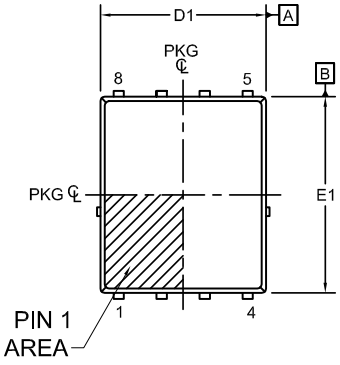
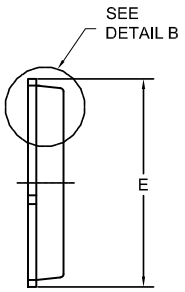
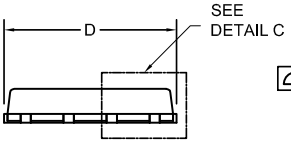
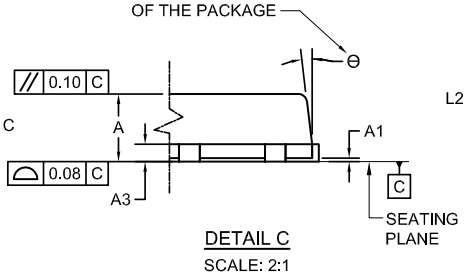


TOP VIEW

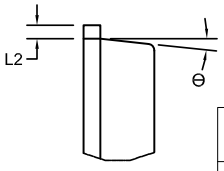




SIDE VIEW



DETAIL C
SCALE: 2:1

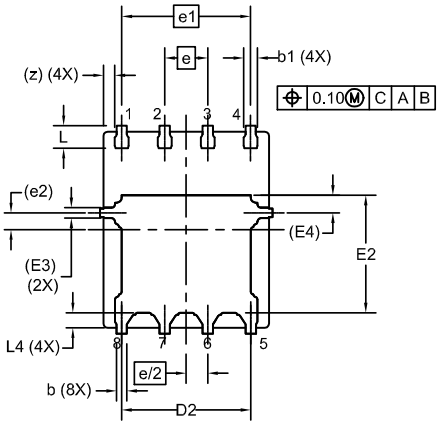


DETAIL B
SCALE: 2:1

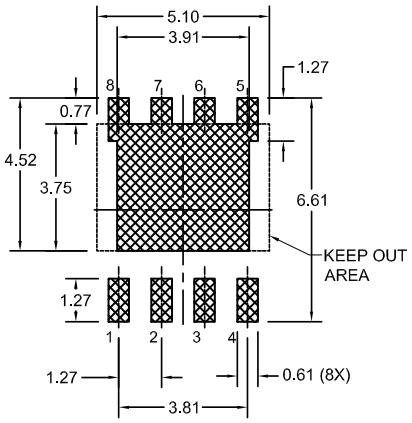
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



BOTTOM VIEW



LAND PATTERN
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DESCRIPTION:	**PQFN8 5X6, 1.27P**		**PAGE 1 OF 1**

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