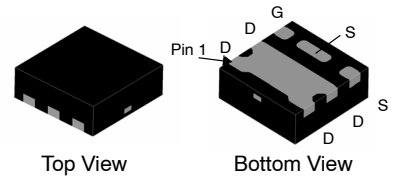
MOSFET – N-Channel, POWERTRENCH®

20 V, 9 A, 18 mohm

FDME820NZT



MicroFET
(UDFN6)
CASE 517DV

General Description

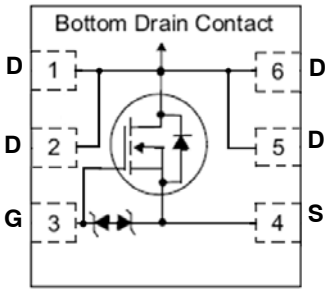
This Single N−Channel MOSFET has been designed using **onsemi**'s advanced Power Trench process to optimize the $R_{DS(ON)}$ @ V_{GS} = 1.8 V on special MicroFET™ leadframe.

Features

- Max $R_{DS(ON)}$ = 18 mΩ at V_{GS} = 4.5 V, I_D = 9 A
- Max $R_{DS(ON)}$ = 24 mΩ at V_{GS} = 2.5 V, I_D = 7.5 A
- Max $R_{DS(ON)}$ = 32 mΩ at V_{GS} = 1.8 V, I_D = 7 A
- Low Profile – 0.55 mm maximum – in the New Package MicroFET 1.6x1.6 Thin
- HBM ESD Protection Level > 2.5 kV (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- RoHS Compliant

Applications

- Li−Ion Battery Pack
- Baseband Switch
- Load Switch
- DC−DC Conversion



MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

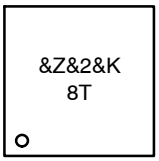
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±12	V
I_D	Drain Current – Continuous T_A = 25°C (Note 1a) – Pulsed	 9 40	A
P_D	Power Dissipation for Single Operation T_A = 25°C (Note 1a) T_A = 25°C (Note 1b)	 2.1 0.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	70	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	190	

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
8T = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDME820NZT	UDFN6 (Pb−Free)	5000 / Tape & Reel

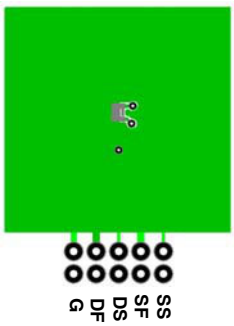
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	20	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS} , I_D = 250 μA	0.5	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	–3	–	mV/°C
$R_{DS(on)}$	Drain to Source On–Resistance	V_{GS} = 4.5 V, I_D = 9 A V_{GS} = 2.5 V, I_D = 7.5 A V_{GS}= 1.8 V, I_D = 7 A, V_{GS} = 4.5 V, I_D = 9 A, T_J = 125°C	– – –	14 17 26 19	18 24 32 24	mΩ
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	–	865	–	pF
C_{oss}	Output Capacitance		–	203	–	pF
C_{rss}	Reverse Transfer Capacitance		–	190	–	pF
R_g	Gate Resistance	f = 1 MHz	–	1.0	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 4 A, V_{GS} = 4.5 V, R_{GEN} = 2 Ω	–	9	–	ns
t_r	Turn–On Rise Time		–	5	–	ns
$t_{d(off)}$	Turn–Off Delay Time		–	19	–	ns
t_f	Turn–Off Fall Time		–	5	–	ns
Q_g	Total Gate Charge	V_{DD} = 4.2 V, I_D = 3 A, V_{GS} = 4.3 V	–	8.0	–	nC
Q_g	Total Gate Charge	V_{DD} = 4.2 V, I_D = 3 A, V_{GS} = 4.5 V	–	8.5	–	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 10 V, I_D = 9 A	–	1.4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	3.2	–	nC
DRAIN–SOURCE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.6 A (Note 2) V_{GS} = 0 V, I_S = 9 A (Note 2)	–	0.7 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	I_F = 9 A, di/dt = 100 A/μs	–	18	–	ns
Q_{rr}	Reverse Recovery Charge		–	4	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR–4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user’s board design.



a. 70°C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 190°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

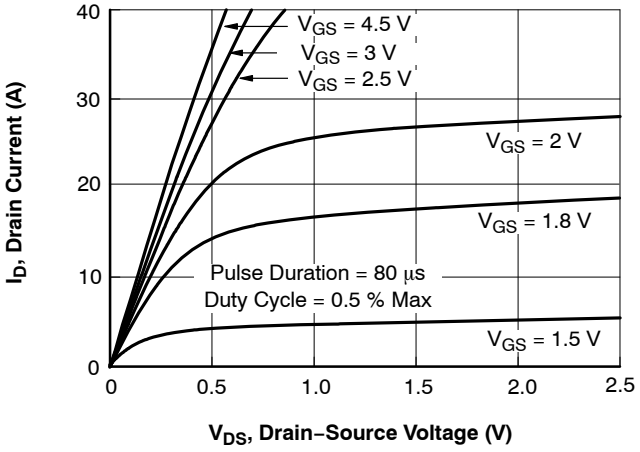


Figure 1. On−Region Characteristics

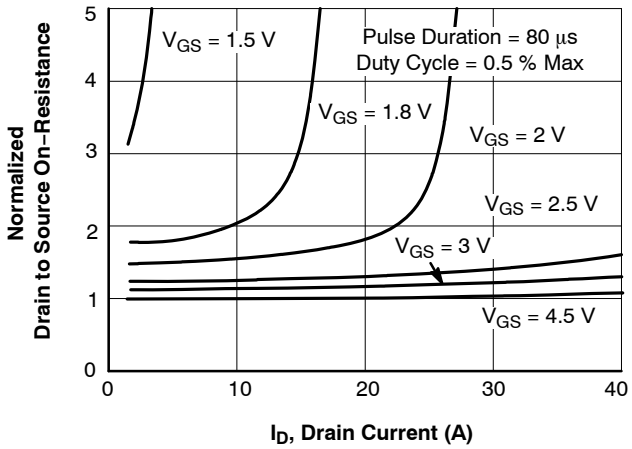


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

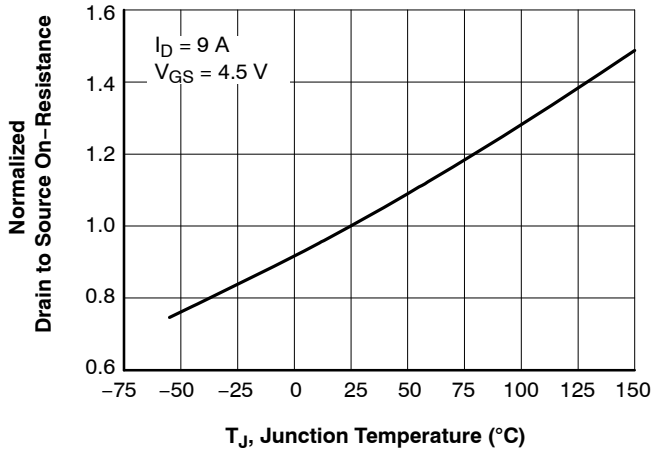


Figure 3. Normalized On−Resistance vs. Junction Temperature

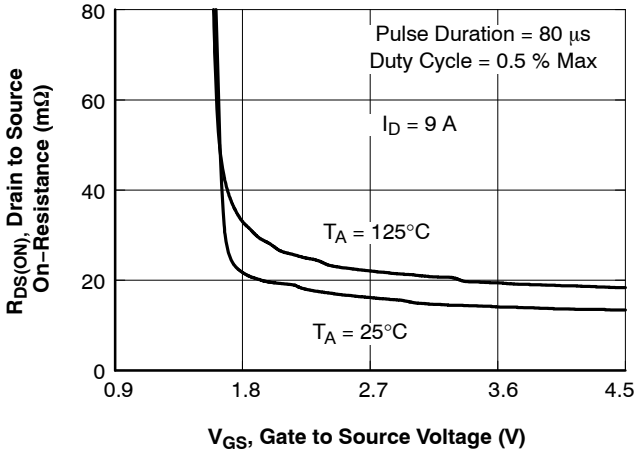


Figure 4. On−Resistance vs Gate−to−Source Voltage

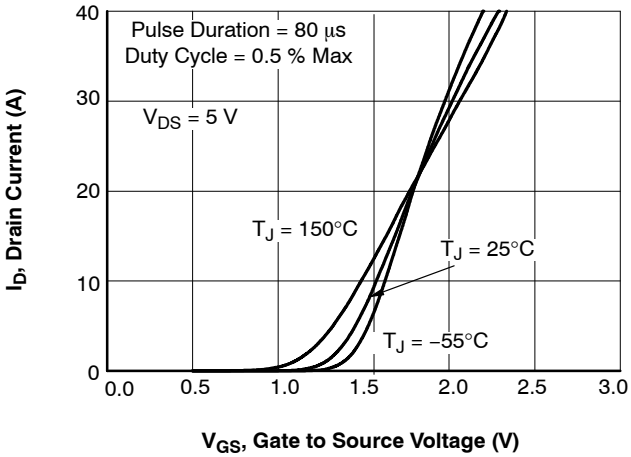


Figure 5. Transfer Characteristics

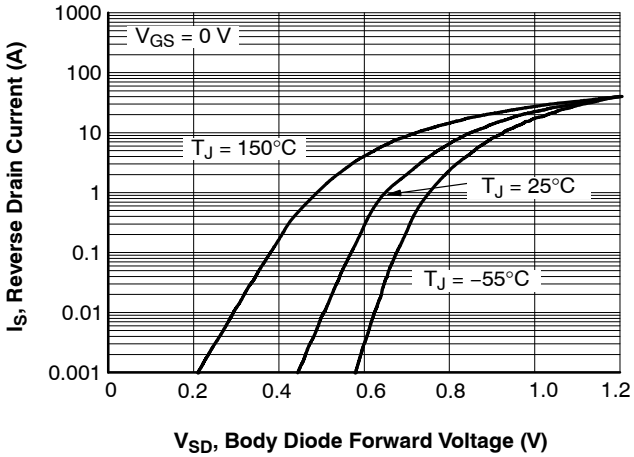


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C, UNLESS OTHERWISE NOTED) (CONTINUED)

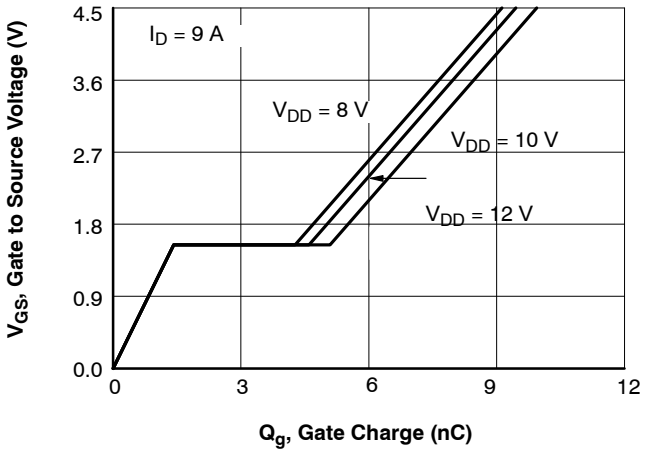


Figure 7. Gate Charge Characteristics

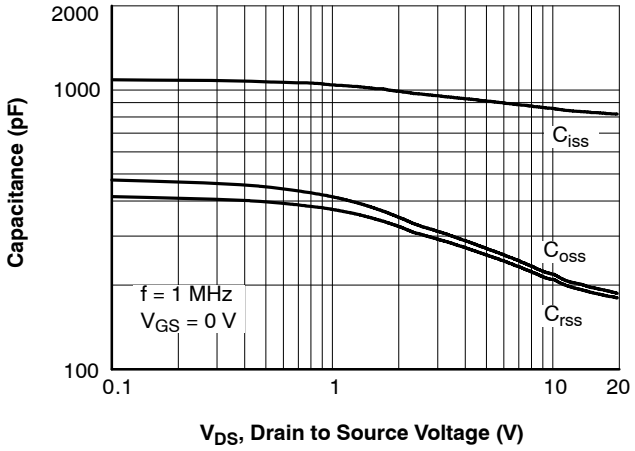


Figure 8. Capacitance vs Drain to Source Voltage

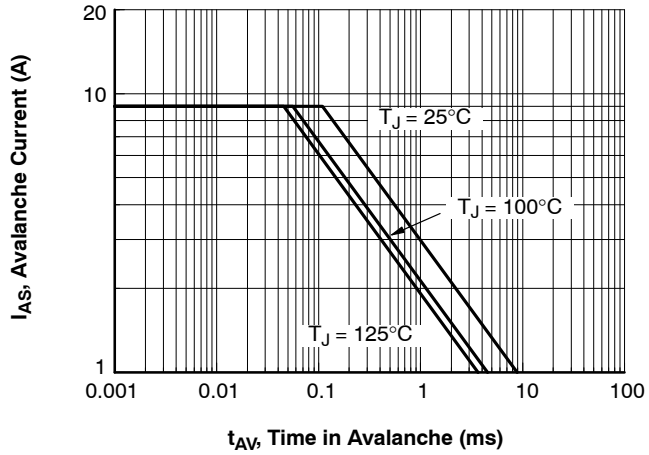


Figure 9. Unclamped Inductive Switching Capability

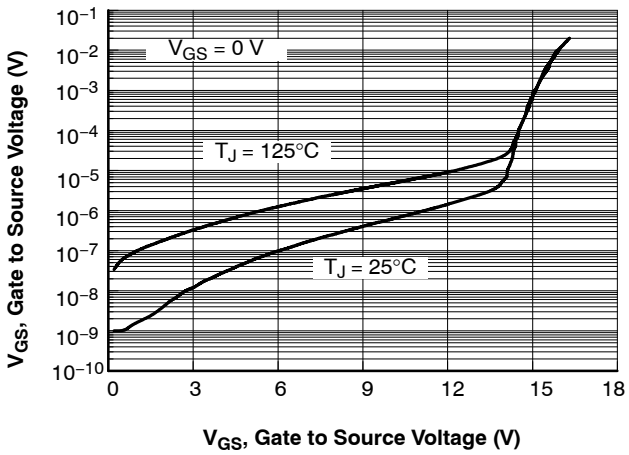


Figure 10. Gate Leakage Current vs Gate to Source Voltage

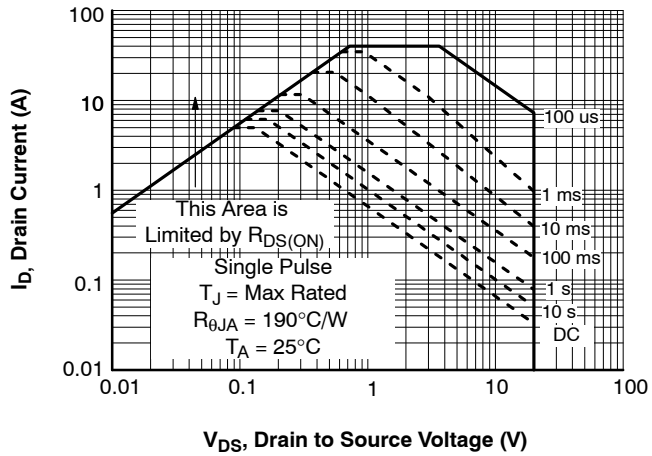


Figure 11. Forward Bias Safe Operating Area

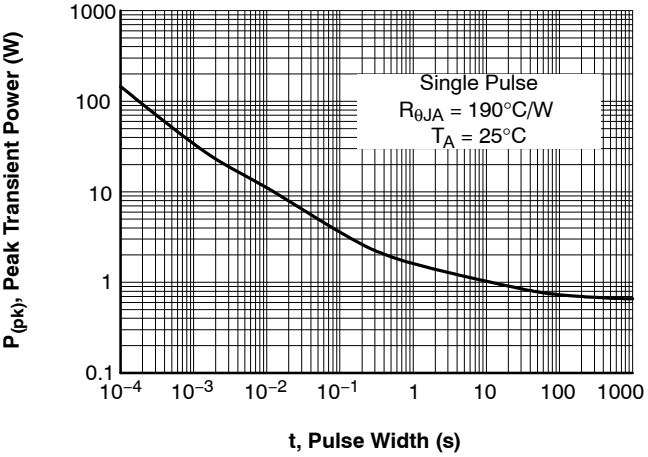


Figure 12. Single Pulse Maximum Power Dissipation

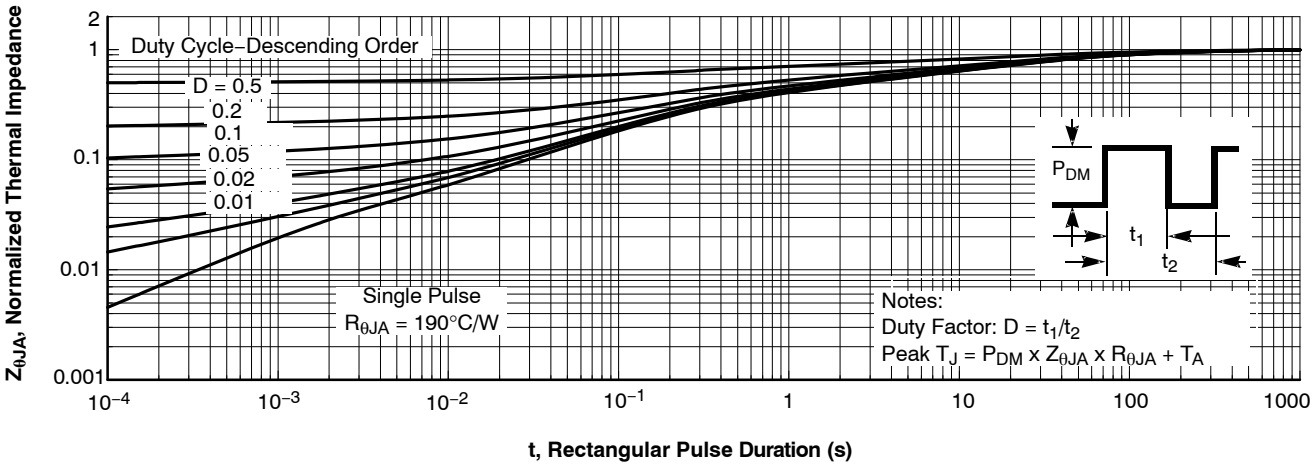
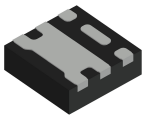
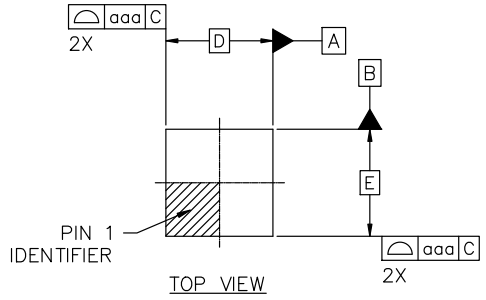


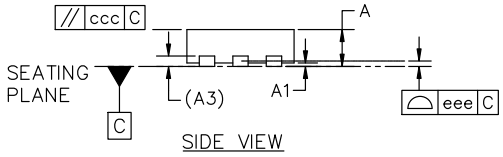
Figure 13. Junction−to−Ambient Transient Thermal Response Curve

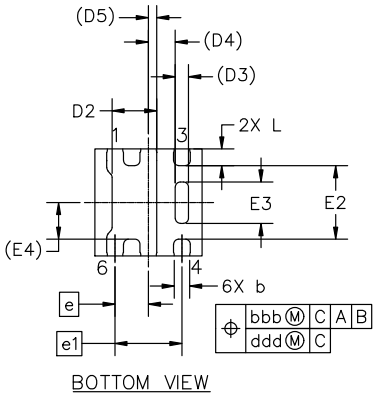


UDFN6 1.60x1.60x0.50, 0.50P
CASE 517DV
ISSUE A

DATE 31 OCT 2024

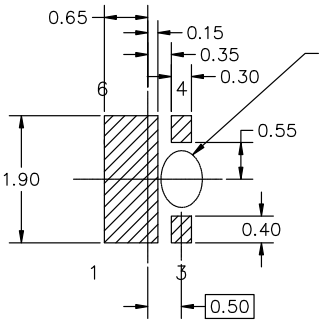




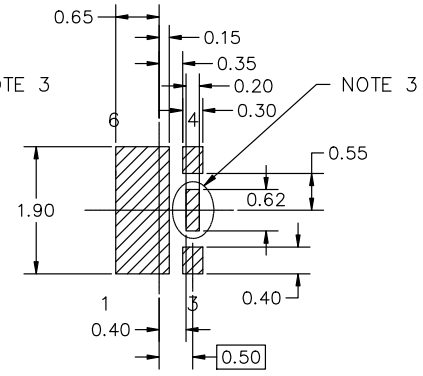


MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3		0.15 REF	
D		1.60 BSC	
D2	0.62	0.67	0.72
D3		0.20 REF	
D4		0.40 REF	
D5		0.125 REF	
E		1.60 BSC	
E2	1.05	1.10	1.15
E3	0.57	0.62	0.67
E4		0.55 REF	
b	0.20	0.25	0.30
e		0.50 BSC	
e1		1.00 BSC	
L	0.20	0.25	0.30

TOLERANCE FORM AND POSITION	
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08



Option 1



Option 2

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASMEY14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NO VIAS OR TRACES ALLOWED IN THE AREA

RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference manual. SOLDERRM/D.

DOCUMENT NUMBER:	**98AON13700G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**UDFN6 1.60x1.60x0.50, 0.50P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales