

# MOSFET – Dual P-Channel POWERTRENCH®

**-20 V, -2.6 A, 142 mΩ**

## FDME1023PZT

### Description

This device is designed specifically as a single package solution for the battery charges switch in cellular handset and other ultra-portable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

The MicroFET 1.6x1.6 **Thin** package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

### Features

- Max  $R_{DS(on)}$  = 142 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -2.3$  A
- Max  $R_{DS(on)}$  = 213 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -1.8$  A
- Max  $R_{DS(on)}$  = 331 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -1.5$  A
- Max  $R_{DS(on)}$  = 530 mΩ at  $V_{GS} = -1.5$  V,  $I_D = -1.2$  A
- Low Profile: 0.55 mm Maximum in the New Package MicroFET 1.6x1.6 **Thin**
- HBM ESD Protection Level > 1600 V (Note 3)
- This Device is Pb-Free, Halide Free and RoHS Compliant

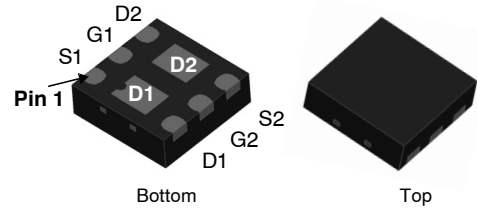
### Typical Applications

- Load Switch
- Battery Charging
- Battery Disconnect Switch

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

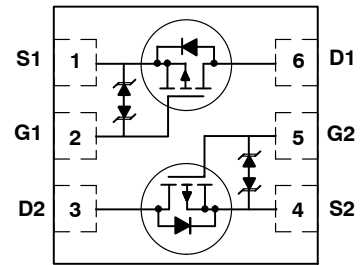
Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	$T_A = 25^\circ\text{C}$ -2.6 -6	A
$P_D$	Power Dissipation for Single Operation – (Note 1a) – (Note 1b)	$T_A = 25^\circ\text{C}$ 1.4 $T_A = 25^\circ\text{C}$ 0.6	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



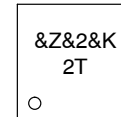
UDFN6 1.6 x 1.6 0.5P  
(MicroFET™ 1.6 x 1.6 Thin)  
CASE 517DW

### ELECTRICAL CONNECTION



Dual P-Channel MOSFET  
(Top View)

### MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code (Year and Week)
- &K = 2-Digit Lot Run Code
- 2T = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDME1023PZT

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation) (Note 1a)	90	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation) (Note 1b)	195	

## ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

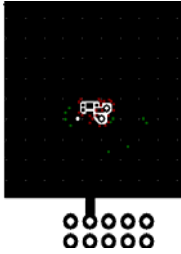
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$	-20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	-	-12	-	mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}$ , $V_{GS} = 0 \text{ V}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}$ , $V_{DS} = 0 \text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250 \mu\text{A}$	-0.4	-0.6	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	-	2	-	mV/°C
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}$ , $I_D = -2.3 \text{ A}$	-	95	142	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ , $I_D = -1.8 \text{ A}$	-	120	213	
		$V_{GS} = -1.8 \text{ V}$ , $I_D = -1.5 \text{ A}$	-	150	331	
		$V_{GS} = -1.5 \text{ V}$ , $I_D = -1.2 \text{ A}$	-	190	530	m $\Omega$
		$V_{GS} = -4.5 \text{ V}$ , $I_D = -2.3 \text{ A}$ , $T_J = 125^\circ\text{C}$	-	128	190	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -4.5 \text{ V}$ , $I_D = -2.3 \text{ A}$	-	7	-	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -10 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$	-	305	405	pF
$C_{oss}$	Output Capacitance		-	55	75	pF
$C_{rss}$	Reverse Transfer Capacitance		-	50	75	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10 \text{ V}$ , $I_D = -1 \text{ A}$ , $V_{GS} = -4.5 \text{ V}$ , $R_{GEN} = 6 \Omega$	-	4.7	10	ns
$t_r$	Rise Time		-	4.8	10	ns
$t_{d(off)}$	Turn-Off Delay Time		-	33	53	ns
$t_f$	Fall Time		-	16	29	ns
$Q_g$	Total Gate Charge	$V_{DD} = -10 \text{ V}$ , $I_D = -2.3 \text{ A}$ , $V_{GS} = -4.5 \text{ V}$	-	5.5	7.7	nC
$Q_{gs}$	Gate to Source Gate Charge		-	0.6	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	1.4	-	nC
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = -0.9 \text{ A}$ (Note 2)	-	-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -2.3 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$	-	16	29	ns
$Q_{rr}$	Reverse Recovery Charge		-	4.4	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

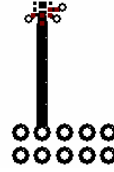
# FDME1023PZT

## NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a. 90°C/W when mounted on  
a 1 in<sup>2</sup> pad of 2 oz copper



b. 195°C/W when mounted on  
a minimum pad of 2 oz copper

2. Pulse Test : Pulse Width < 300  $\mu$ s, Duty Cycle < 2.0%
3. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

# FDME1023PZT

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

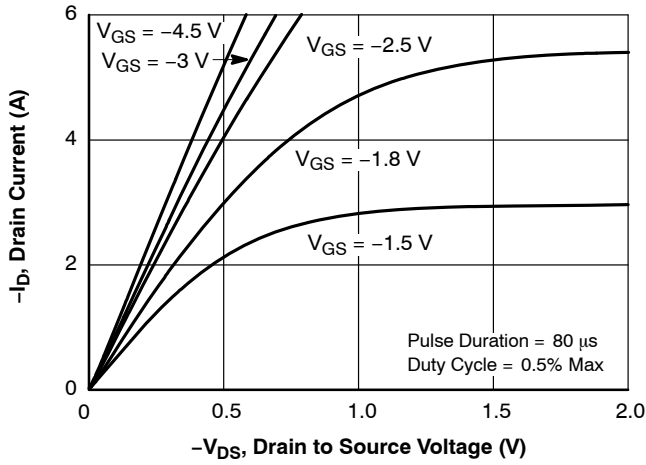


Figure 1. On Region Characteristics

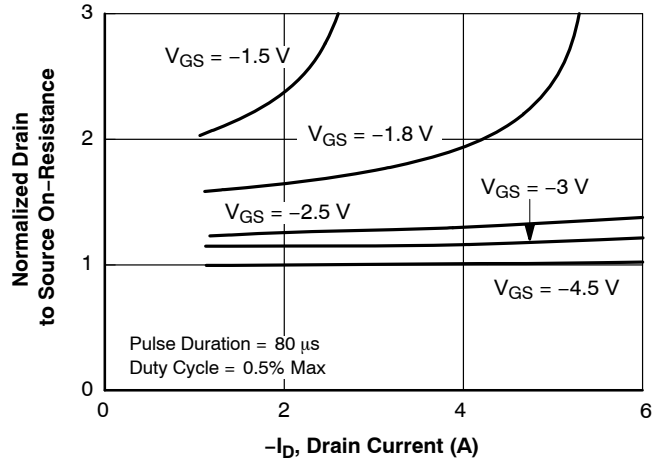


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

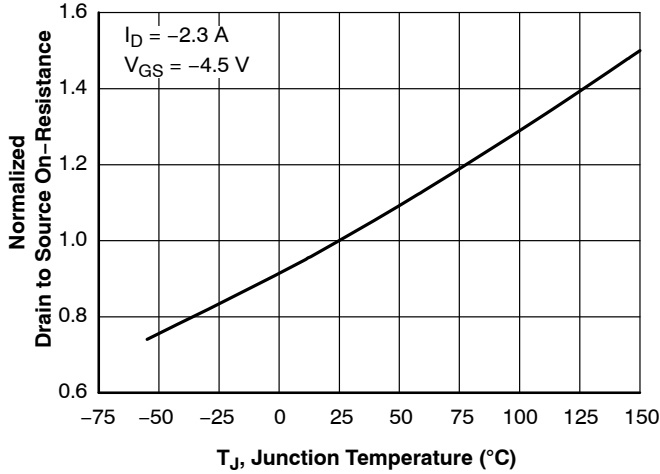


Figure 3. Normalized On Resistance vs. Junction Temperature

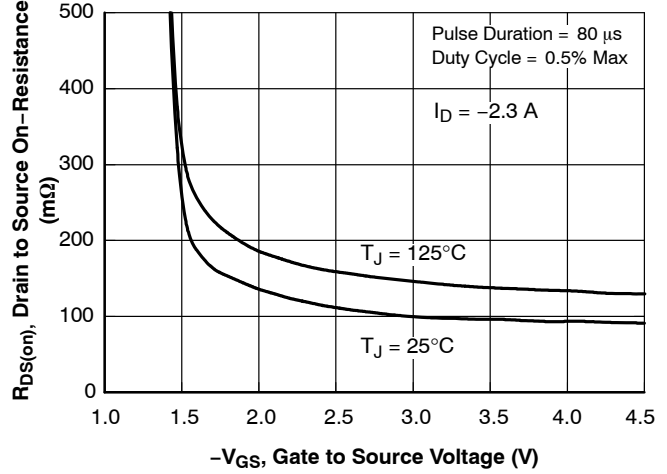


Figure 4. On-Resistance vs. Gate to Source Voltage

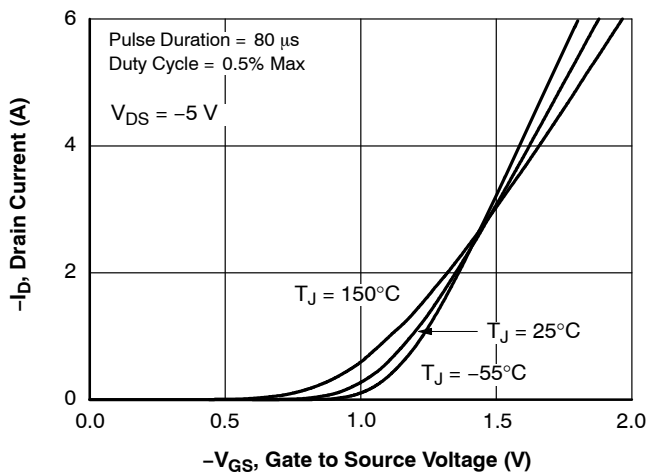


Figure 5. Transfer Characteristics

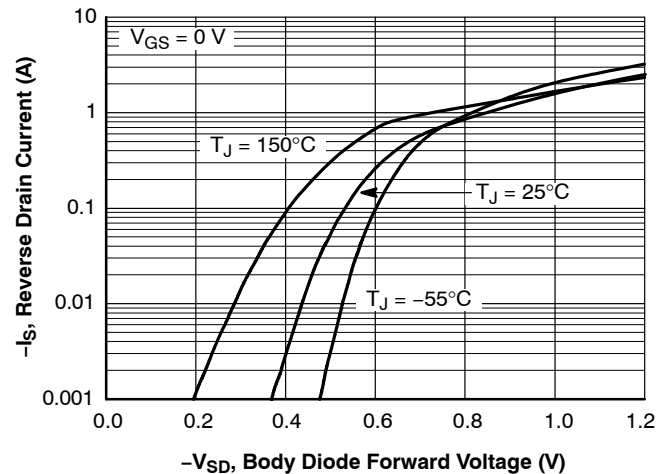


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# FDME1023PZT

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

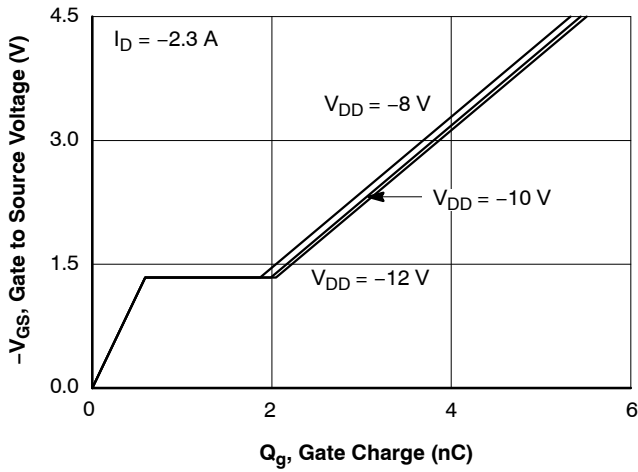


Figure 8. Gate Charge Characteristics

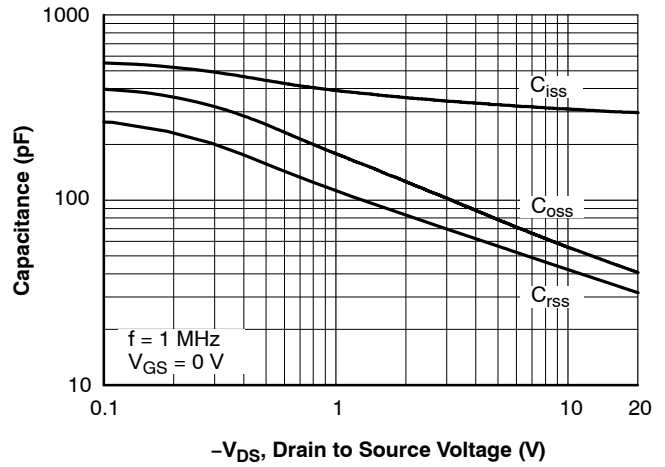


Figure 9. Capacitance vs. Drain to Source Voltage

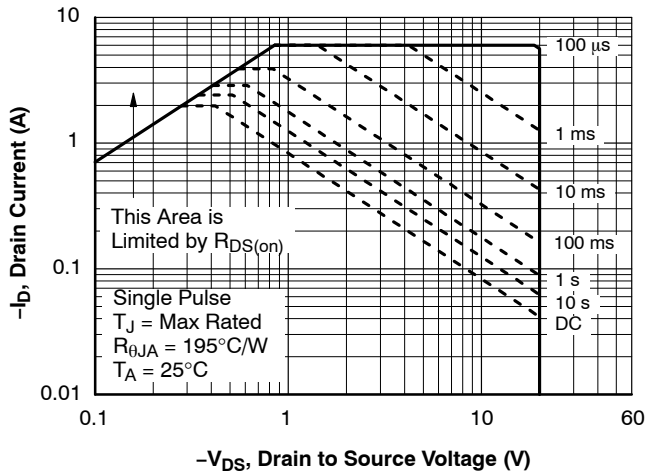


Figure 7. Forward Bias Safe Operating Area

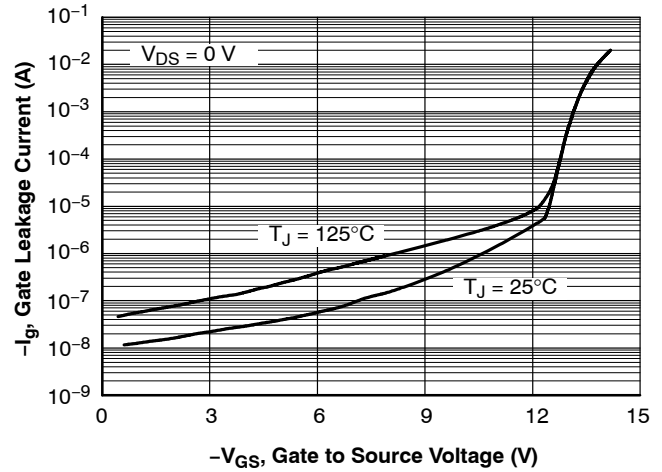


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

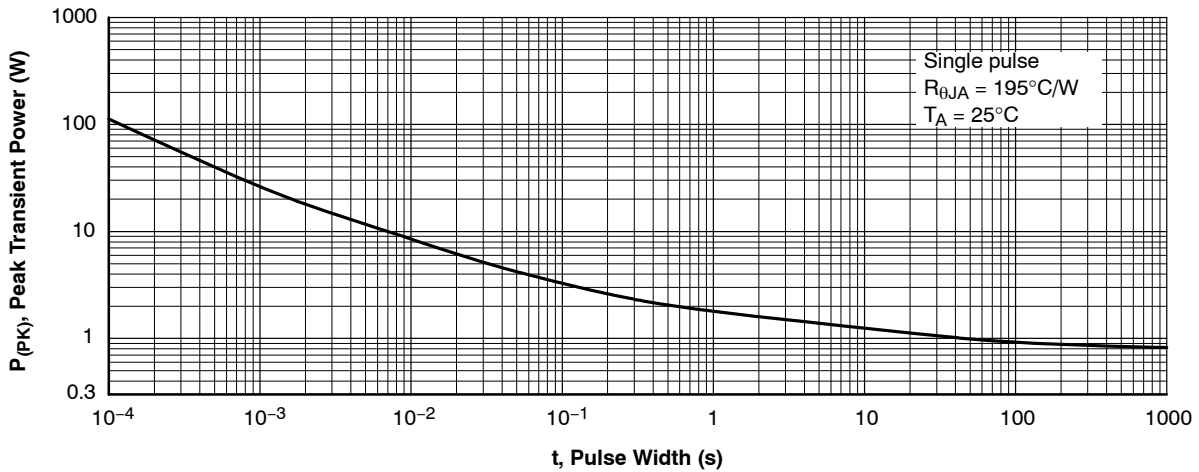


Figure 11. Single Pulse Maximum Power Dissipation

# FDME1023PZT

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

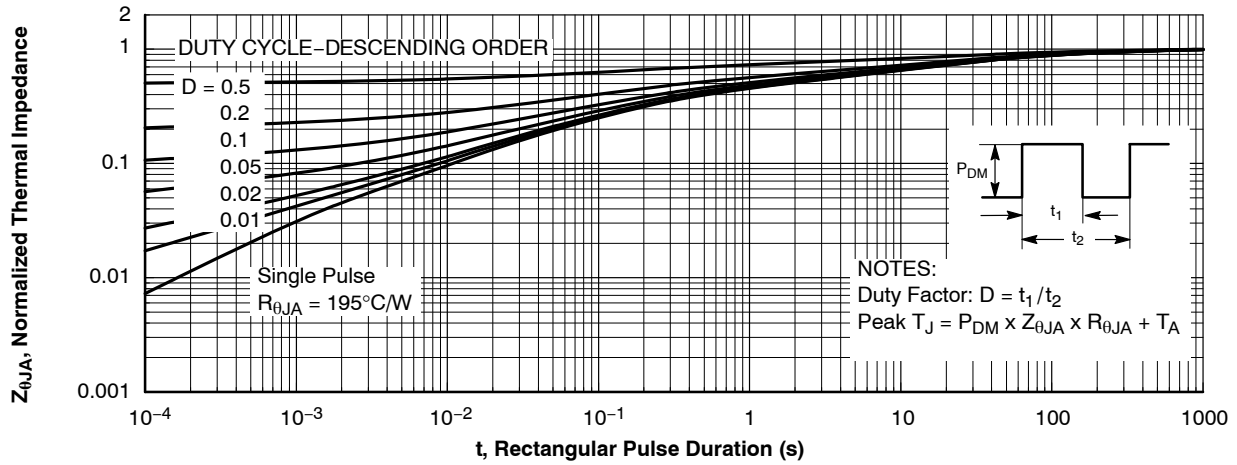


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping <sup>†</sup>
FDME1023PZT	2T	UDFN6 1.6×1.6 0.5P (MicroFET 1.6×1.6 Thin) (Pb-Free/Halide Free)	7"	8 mm	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

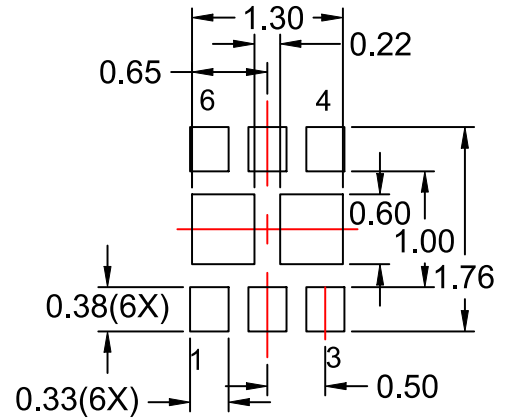
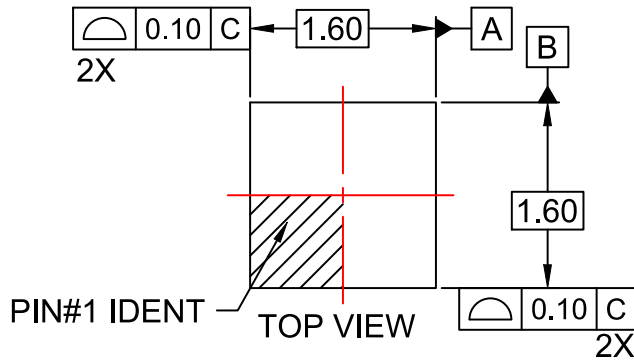
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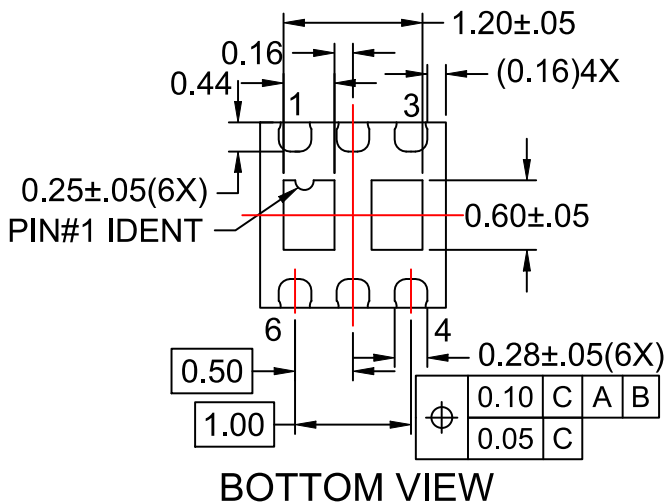
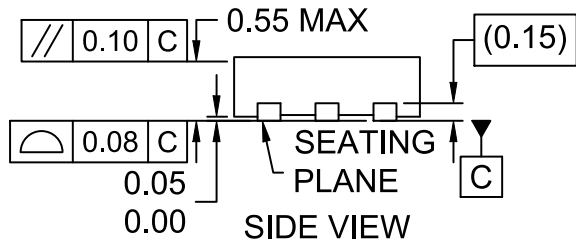


**UDFN6 1.6x1.6, 0.5P**  
CASE 517DW  
ISSUE O

DATE 31 OCT 2016



**RECOMMENDED  
LAND PATTERN**



**NOTES:**

- A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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