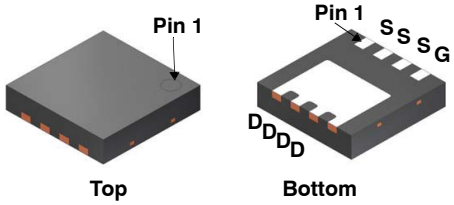
# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

## 80 V, 6.5 mΩ , 48 A

# FDMC86340




**WDFN8**
**CASE 483AW**

### Description

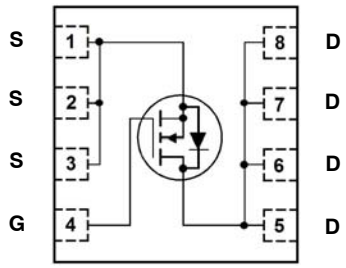
This N−Channel MOSFET is produced using **onsemi**'s advanced POWETRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on−state resistance and yet maintain superior switching performance.

### Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 6.5 mΩ at $V_{GS}$ = 10 V, $I_D$ = 14 A
- Max $R_{DS(on)}$ = 8.5 mΩ at $V_{GS}$ = 8 V, $I_D$ = 12 A
- High Performance Technology for Extremely Low $R_{DS(on)}$
- Termination is Lead−Free
- RoHS Compliant

### Applications

- DC−DC Conversion




### MARKING DIAGRAM


| | | |
|---|---|---|
| $Y | = | **onsemi** Logo |
| Z | = | Assembly Plant Code |
| XYY | = | Date Code (Year &Week) |
| KK | = | Lot Traceability Code |
| FDMC86340 | = | Specific Device Code |

### MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain−to−Source Voltage | 80 | V |
| $V_{GS}$ | Gate−to−Source Voltage | ±20 | V |
| $I_D$ | Drain Current − Continuous<br>$T_C$ = 25°C<br>$T_A$ = 25°C (Note 1a) | <br>48<br>14 | A |
| | − Pulsed (Note 4) | 200 | |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | 216 | mJ |
| $P_D$ | Power Dissipation<br>$T_C$ = 25°C<br>$T_A$ = 25°C (Note 1a) | <br>54<br>2.3 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDMC86340 | WDFN8<br>(Pb-Free,<br>Halide Free) | 3000 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case (Note 1) | 2.3 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1a) | 53 | |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain−to−Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 80 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | 46 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 64 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate−to−Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate−to−Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.0 | 3.4 | 4.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate−to−Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | −10 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain−to−Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 14 A | – | 5.0 | 6.5 | mΩ |
| | | $V_{GS}$ = 8 V, $I_D$ = 12 A | – | 6.0 | 8.5 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 14 A, $T_J$ = 125°C | – | 8.5 | 11 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 14 A | – | 36 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 2775 | 3885 | pF |
| $C_{oss}$ | Output Capacitance | | – | 468 | 655 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 15 | 25 | pF |
| $R_g$ | Gate Resistance | | 0.1 | 0.7 | 2.1 | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = 40 V, $I_D$ = 14 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 20 | 32 | ns |
| $t_r$ | Rise Time | | – | 7.9 | 16 | |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 23 | 37 | |
| $t_f$ | Fall Time | | – | 5.1 | 10 | |
| $Q_{g(tot)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 40 V, $I_D$ = 14 A | – | 38 | 53 | nC |
| $Q_{g(tot)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 8 V, $V_{DD}$ = 40 V, $I_D$ = 14 A | – | 31 | 44 | |
| $Q_{gs}$ | Gate−to−Source Charge | $V_{DD}$ = 40 V, $I_D$ = 14 A | – | 14 | – | |
| $Q_{gd}$ | Gate−to−Drain “Miller” Charge | $V_{DD}$ = 40 V, $I_D$ = 14 A | – | 8.0 | – | |
| $Q_{oss}$ | Output Charge | $V_{DD}$ = 40 V, $I_D$ = 0 V | – | 42 | – | |

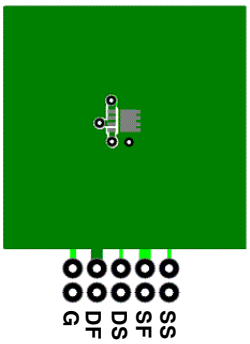
**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source−to−Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 14 A (Note 2) | – | 0.80 | 1.3 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 1.9 A (Note 2) | – | 0.7 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 14 A, di/dt = 100 A/μs | – | 41 | 66 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 25 | 40 | nC |

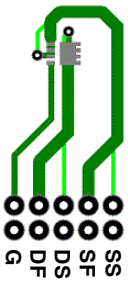
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.




a) 53°C/W when mounted on a 1 $in^2$ pad of 2 oz copper




b) 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. $E_{AS}$ of 216 mJ is based on starting $T_J$ = 25 °C, L = 3 mH, $I_{AS}$ = 12 A, $V_{DD}$ = 80 V, $V_{GS}$ = 10 V. 100% test at L = 0.1 mH, $I_{AS}$ = 37 A.
4. Pulsed Id limited by junction temperature, td ≤ 100 μS, please refer to SOA curve for more details.

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise noted)

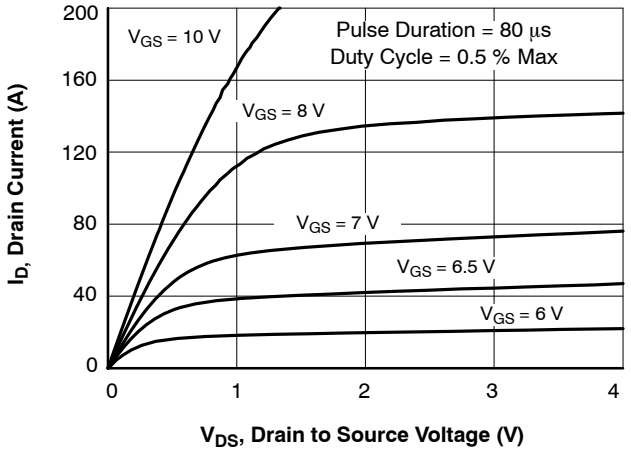



**Figure 1. On−Region Characteristics**

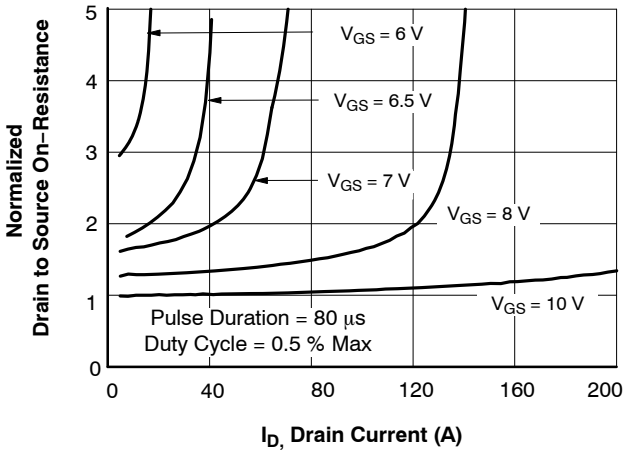



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

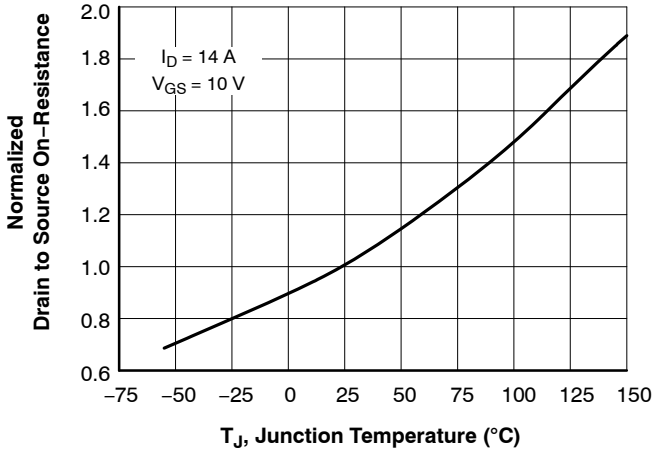



**Figure 3. Normalized On−Resistance vs. Junction Temperature**

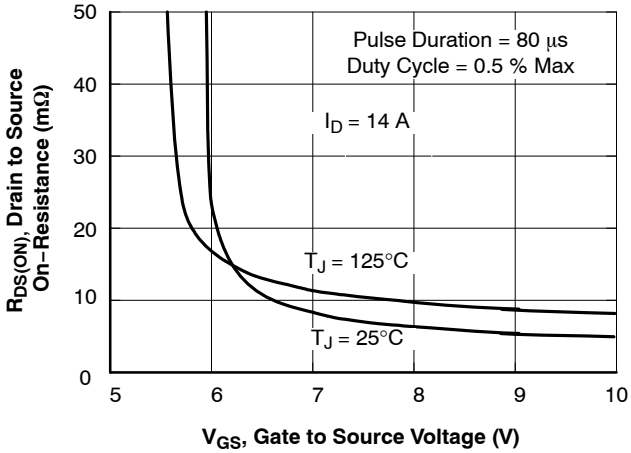



**Figure 4. On−Resistance vs. Gate to Source Voltage**

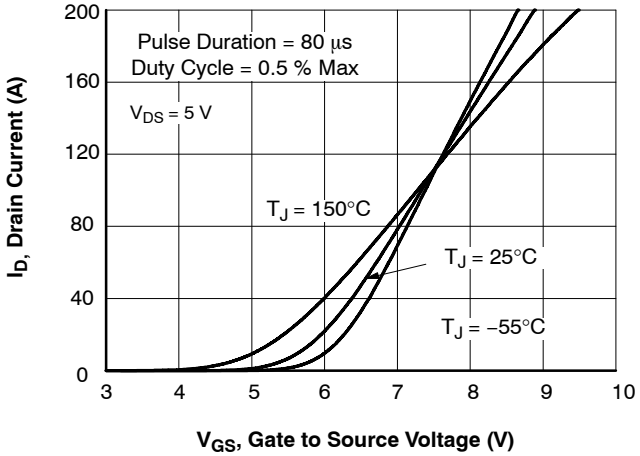



**Figure 5. Transfer Characteristics**

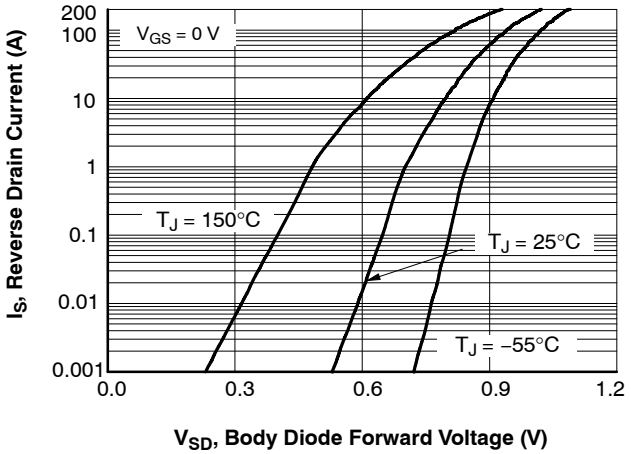



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS (continued)

($T_J$ = 25°C unless otherwise noted)

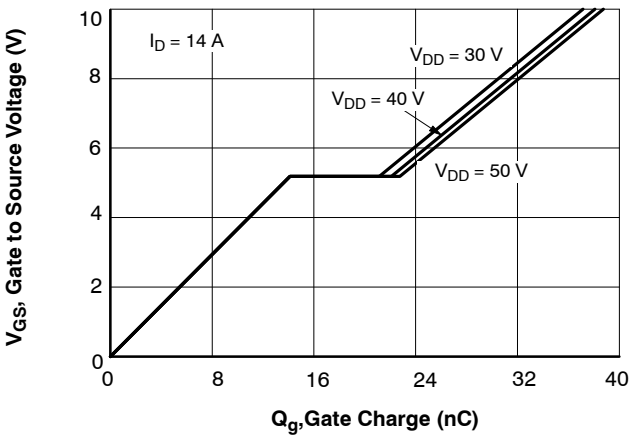



**Figure 7. Gate Charge Characteristics**

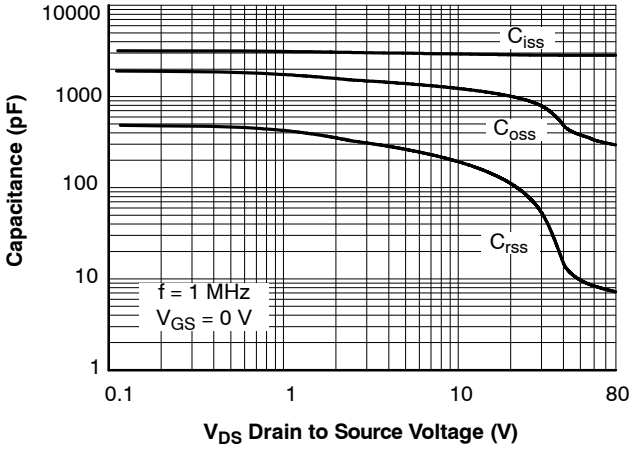



**Figure 8. Capacitance vs Drain to Source Voltage**

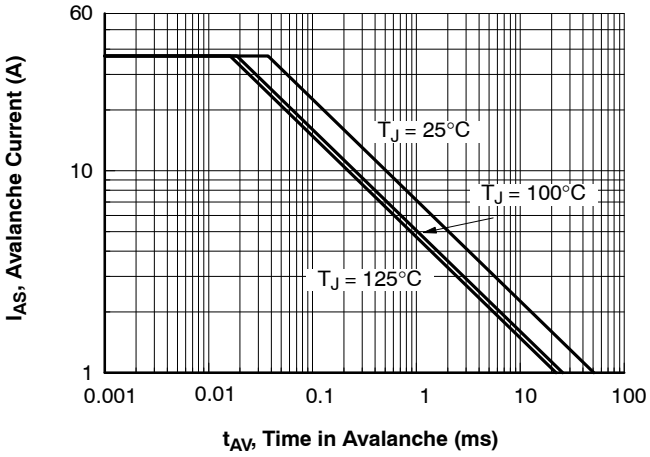



**Figure 9. Unclamped Inductive Switching Capability**

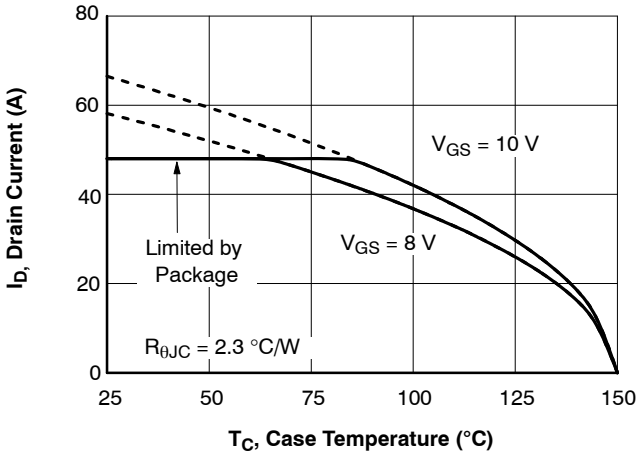



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

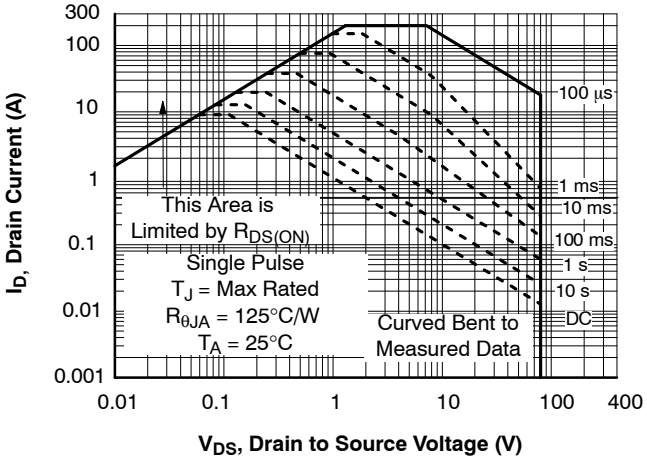



**Figure 11. Forward Bias Safe Operating Area**

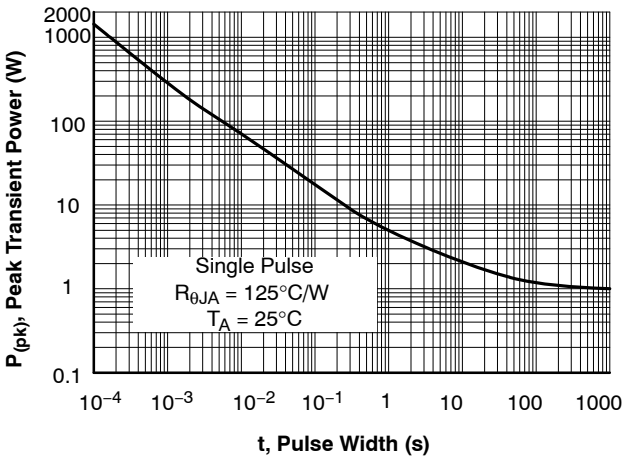



**Figure 12. Single Pulse Maximum Power Dissipation**

## TYPICAL CHARACTERISTICS (continued)

($T_J$ = 25°C unless otherwise noted)

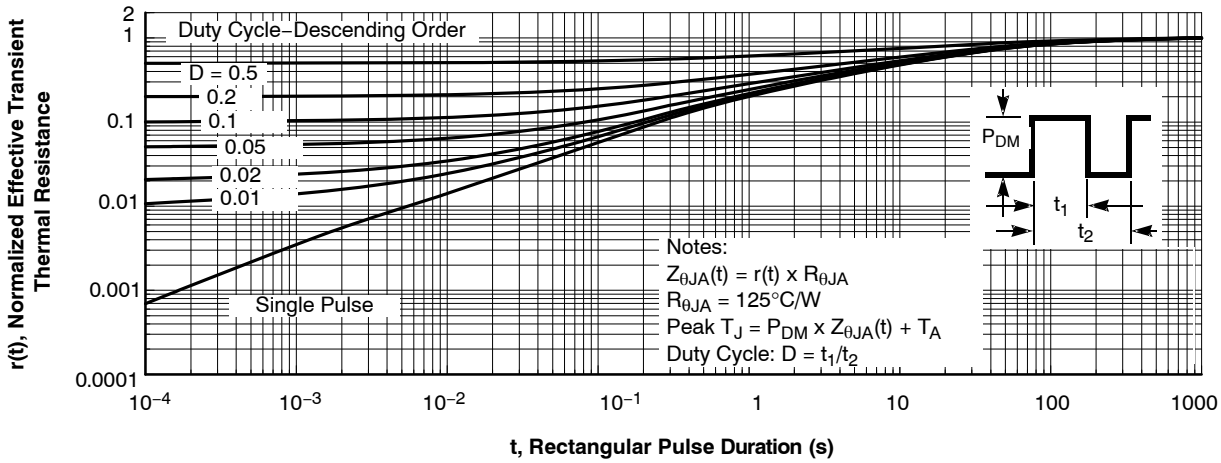
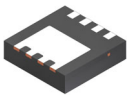
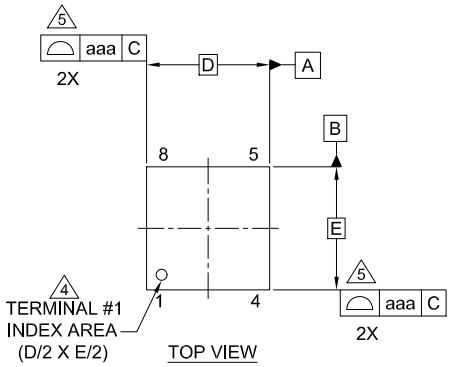


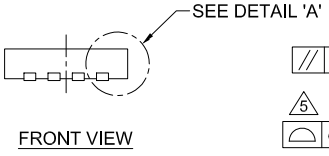

**Figure 13. Junction−to−Ambient Transient Thermal Response Curve**

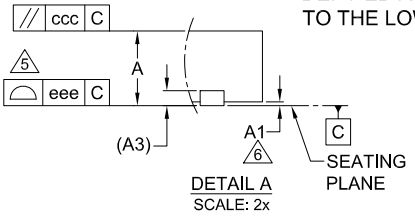


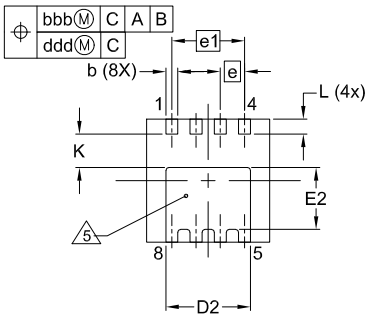
**WDFN8 3.30x3.30x0.75, 0.65P**
CASE 483AW
ISSUE B

DATE 22 MAR 2024



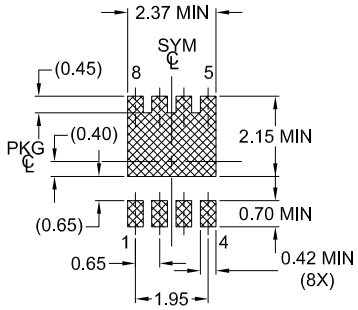




NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | -- | -- | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.27 | 0.32 | 0.37 |
| D | | 3.30 BSC | |
| D2 | 2.17 | 2.27 | 2.37 |
| E | | 3.30 BSC | |
| E2 | 1.56 | 1.66 | 1.76 |
| e | | 0.65 BSC | |
| e1 | | 1.95 BSC | |
| K | 0.90 | -- | -- |
| L | 0.30 | 0.40 | 0.50 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.05 | |

## LAND PATTERN RECOMMENDATION




*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON13672G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **WDFN8 3.30x3.30x0.75, 0.65P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales