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# FDMC8097AC

**Dual N & P-Channel PowerTrench<sup>®</sup> MOSFET**  
**N-Channel: 150 V, 2.4 A, 155 mΩ P-Channel: -150 V, -0.9 A, 1200 mΩ**

## Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 155 mΩ at  $V_{GS} = 10$  V,  $I_D = 2.4$  A
- Max  $r_{DS(on)}$  = 212 mΩ at  $V_{GS} = 6$  V,  $I_D = 2$  A

Q2: P-Channel

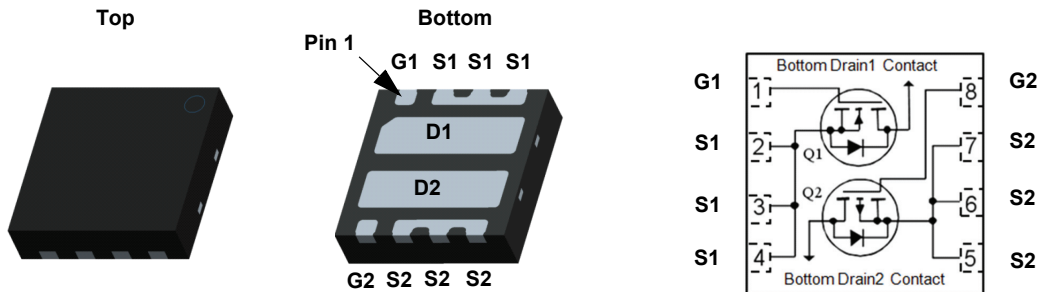
- Max  $r_{DS(on)}$  = 1200 mΩ at  $V_{GS} = -10$  V,  $I_D = -0.9$  A
- Max  $r_{DS(on)}$  = 1400 mΩ at  $V_{GS} = -6$  V,  $I_D = -0.8$  A
- Optimised for active clamp forward converters
- RoHS Compliant

## General Description

These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance. Shrinking the area needed for implementation of active clamp topology; enabling best in class power density.

## Applications

- DC-DC Converter
- Active Clamp



Power 33

## MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Q1	Q2	Units	
$V_{DS}$	Drain to Source Voltage	150	-150	V	
$V_{GS}$	Gate to Source Voltage	±20	±25	V	
$I_D$	Drain Current -Continuous	$T_C = 25$ °C (Note 5)	6.3	-2.0	A
	-Continuous	$T_C = 100$ °C (Note 5)	3.9	-1.2	
	-Continuous	$T_A = 25$ °C	2.4 <sup>1a</sup>	-0.9 <sup>1b</sup>	
	-Pulsed	(Note 4)	33	-8.8	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	24	6	mJ
$P_D$	Power Dissipation for Single Operation	$T_A = 25$ °C	1.9 <sup>1a</sup>	1.9 <sup>1b</sup>	W
	Power Dissipation for Single Operation	$T_A = 25$ °C	0.8 <sup>1c</sup>	0.8 <sup>1d</sup>	
	Power Dissipation for Single Operation	$T_C = 25$ °C	14	10	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		°C	

## Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	65 <sup>1a</sup>	65 <sup>1b</sup>	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	155 <sup>1c</sup>	155 <sup>1d</sup>	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	8.9	12.5	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8097AC	FDMC8097AC	Power 33	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$ $I_D = -250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	Q1 Q2	150 -150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		98 122		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -120\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	Q1 Q2	2.0 -2.0	3.1 -3.0	4.0 -4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-9 -6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 2.4\text{ A}$ $V_{GS} = 6\text{ V}, I_D = 2\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 2.4\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q1		124 155 245	155 212 306	m $\Omega$
		$V_{GS} = -10\text{ V}, I_D = -0.9\text{ A}$ $V_{GS} = -6\text{ V}, I_D = -0.8\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -0.9\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q2		930 1030 1682	1200 1400 2171	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\text{ V}, I_D = 2.4\text{ A}$ $V_{DD} = -10\text{ V}, I_D = -0.9\text{ A}$	Q1 Q2		6.4 0.75		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		279 162	395 230	pF
$C_{oss}$	Output Capacitance	Q2	Q1 Q2		26 13	40 25	pF
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS} = -75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		1.4 0.6	5 5	pF
$R_g$	Gate Resistance		Q1 Q2	0.1 0.1	0.6 3.3	1.5 8.3	$\Omega$

**Switching Characteristics**

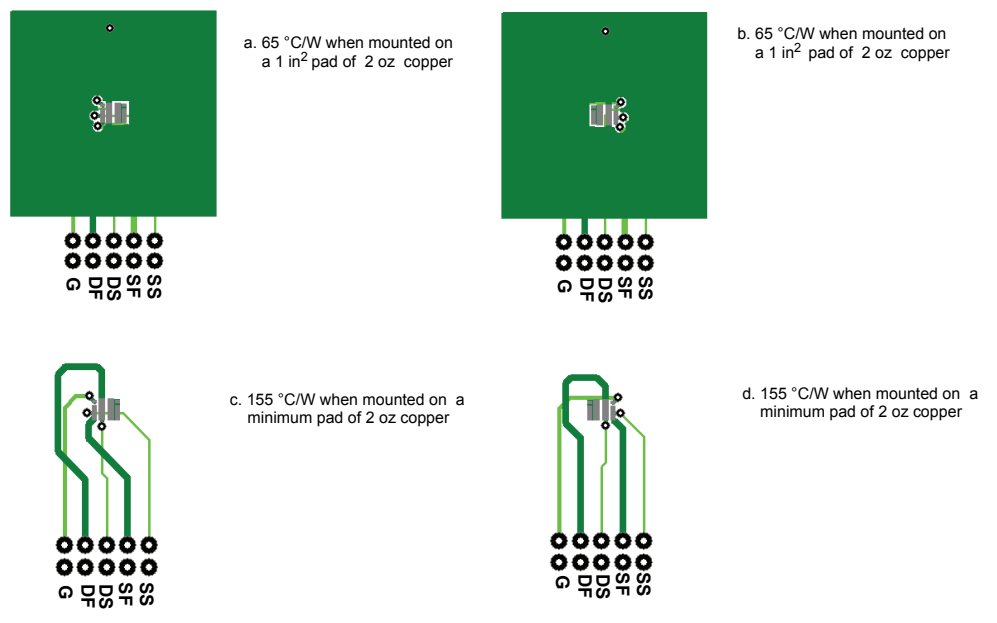
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 75\text{ V}, I_D = 2.4\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		5.4 5.2	11 11	ns
$t_r$	Rise Time		Q1 Q2		1.3 1.6	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -75\text{ V}, I_D = -0.9\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		9.1 7.4	18 15	ns
$t_f$	Fall Time		Q1 Q2		2.2 6.3	10 13	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$ $V_{GS} = 0\text{ V to } -10\text{ V}$	Q1 Q2		4.4 2.8	6.2 4.0	nC
		$V_{GS} = 0\text{ V to } 6\text{ V}$ $V_{GS} = 0\text{ V to } -6\text{ V}$	Q1 Q2		2.9 1.8	4.1 2.6	
$Q_{gs}$	Gate to Source Charge		Q1 Q2		1.3 0.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1 Q2		1.0 0.7		nC

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
<b>Drain-Source Diode Characteristics</b>							
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.4\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -0.9\text{ A}$ (Note 2)	Q1 Q2		0.8 -0.9	1.3 -1.3	V
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 2.4\text{ A}, di/dt = 100\text{ A/s}$	Q1 Q2		50 44	80 71	ns
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = -0.9\text{ A}, di/dt = 100\text{ A/s}$	Q1 Q2		43 68	69 109	nC

**Notes:**

1.  $R_{\theta JA}$  is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- 2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- 3. Q1:  $E_{AS}$  of 24 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 4\text{ A}$ ,  $V_{DD} = 150\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 14\text{ A}$ .  
Q2:  $E_{AS}$  of 6 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = -2\text{ A}$ ,  $V_{DD} = -150\text{ V}$ ,  $V_{GS} = -10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = -8\text{ A}$ .
- 4. Q1: Pulsed  $I_d$  please refer to Fig 11 SOA graph for more details.  
Q2: Pulsed  $I_d$  please refer to Fig 24 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

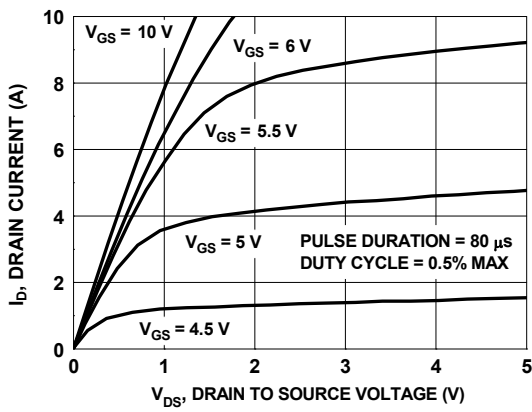


Figure 1. On Region Characteristics

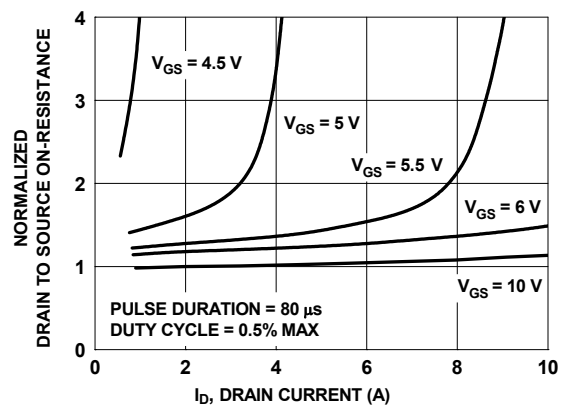


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

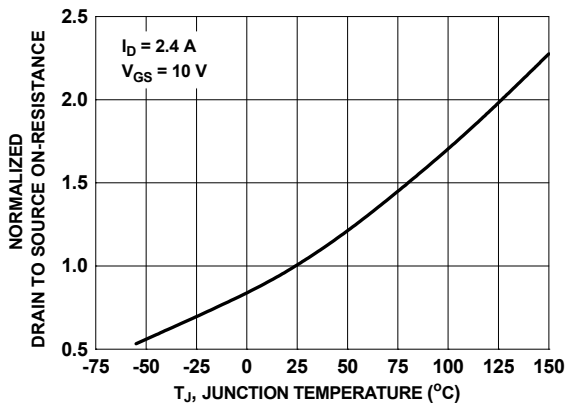


Figure 3. Normalized On Resistance vs. Junction Temperature

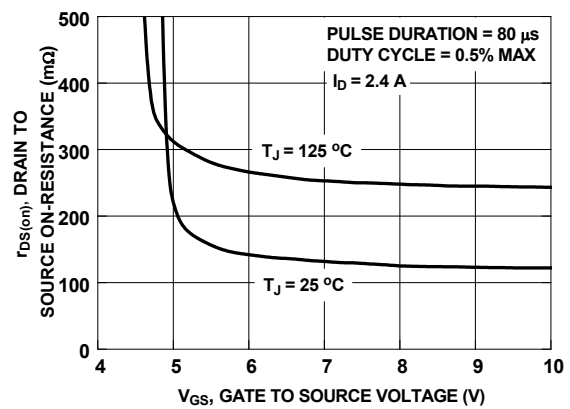


Figure 4. On-Resistance vs. Gate to Source Voltage

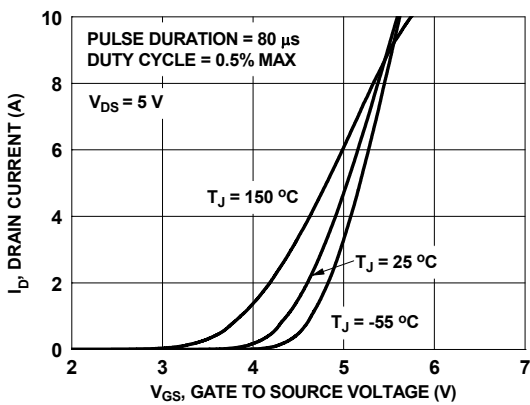


Figure 5. Transfer Characteristics

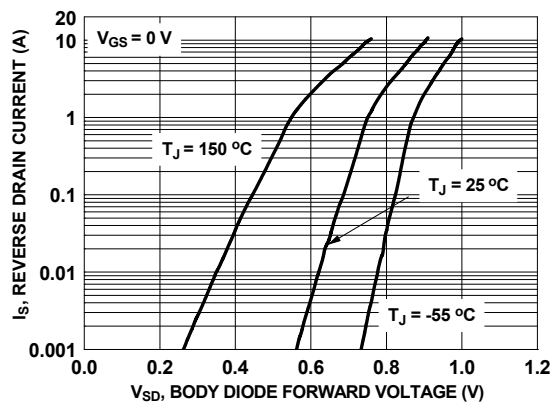
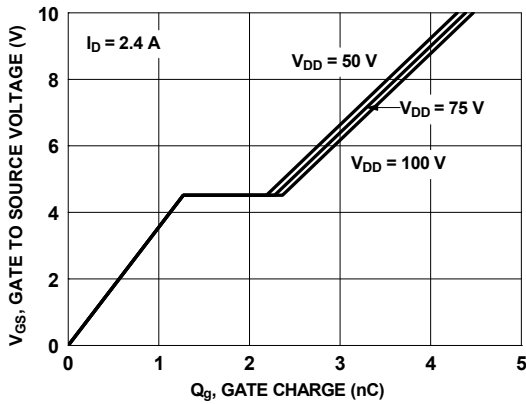
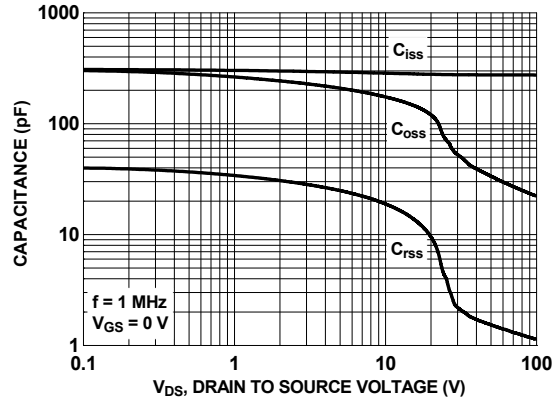


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

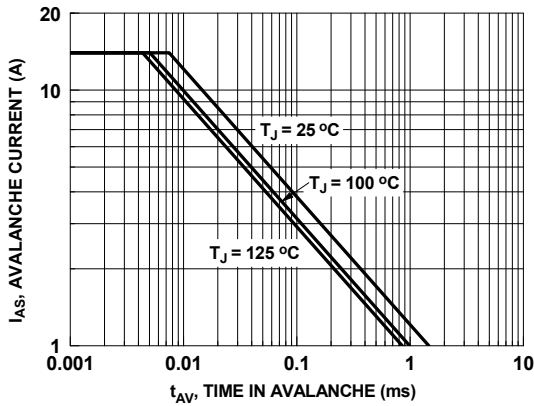
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



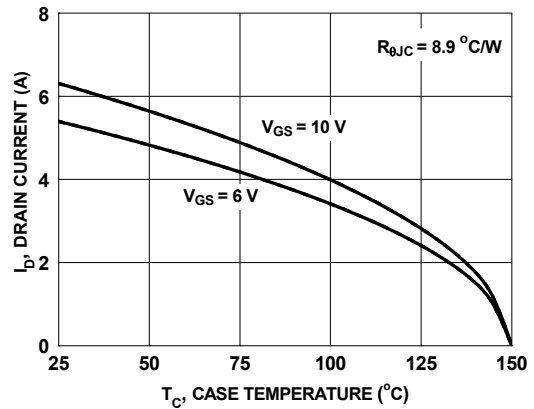
**Figure 7. Gate Charge Characteristics**



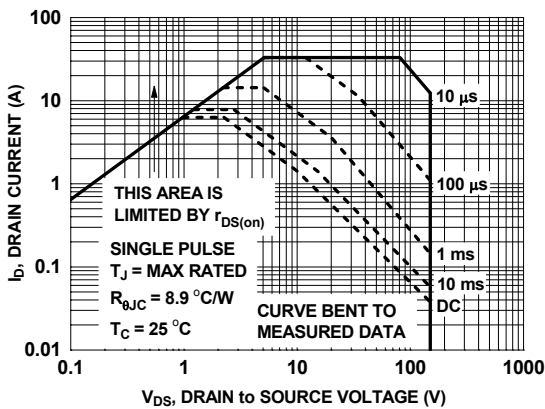
**Figure 8. Capacitance vs. Drain to Source Voltage**



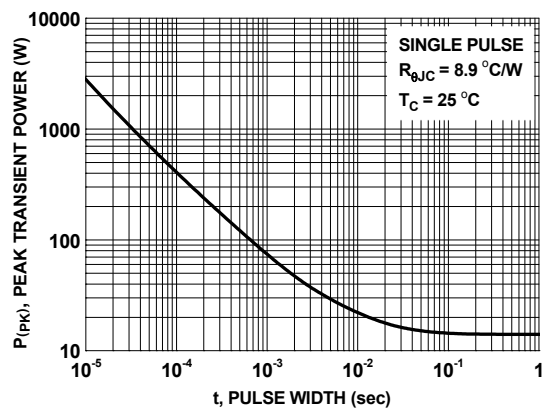
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

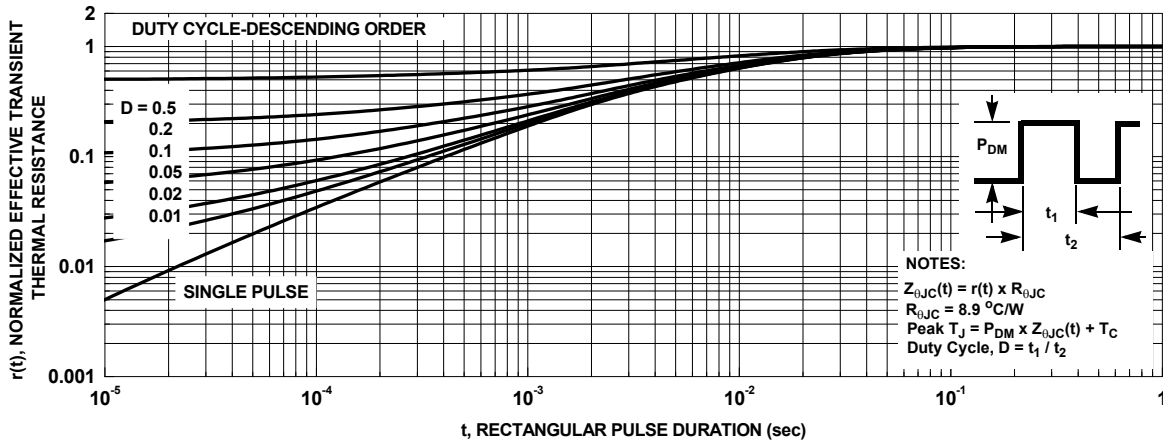


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

**Typical Characteristics (Q2 P-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

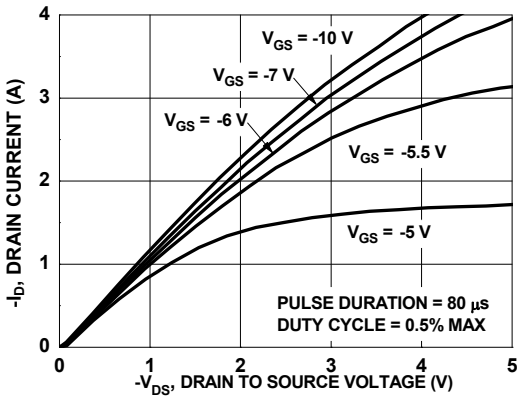


Figure 14. On-Region Characteristics

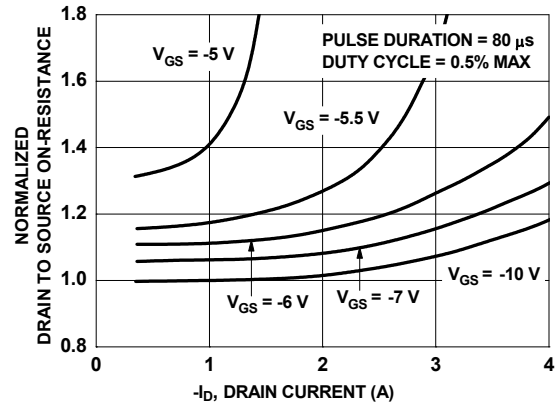


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

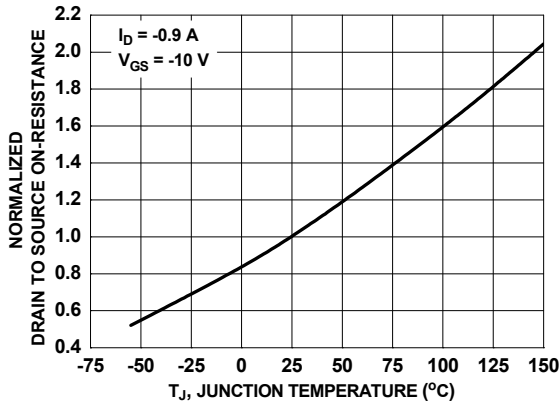


Figure 16. Normalized On-Resistance vs. Junction Temperature

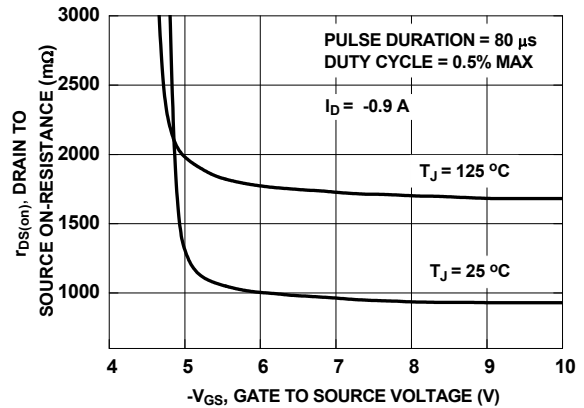


Figure 17. On-Resistance vs. Gate to Source Voltage

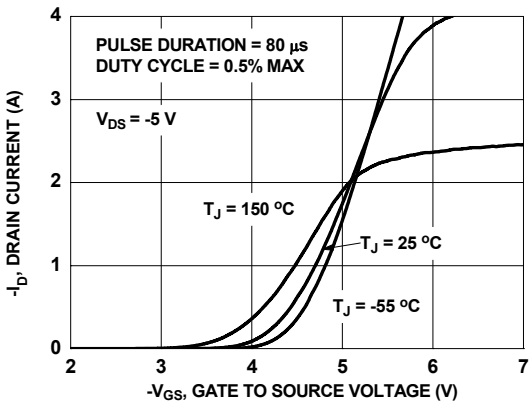


Figure 18. Transfer Characteristics

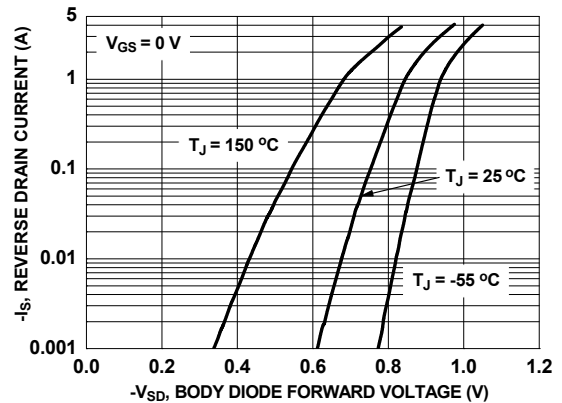
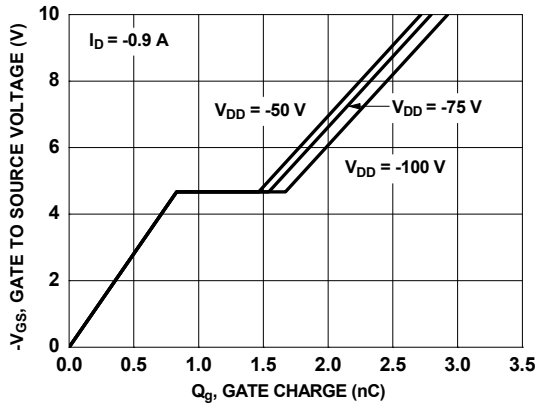


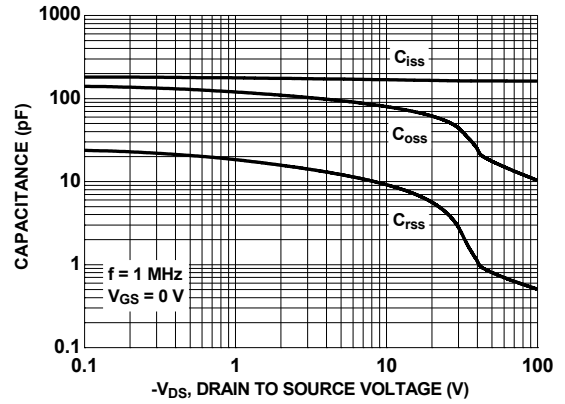
Figure 19. Source to Drain Diode Forward Voltage vs. Source Current



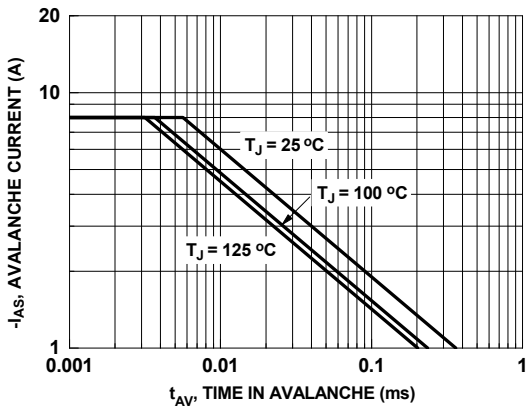
**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



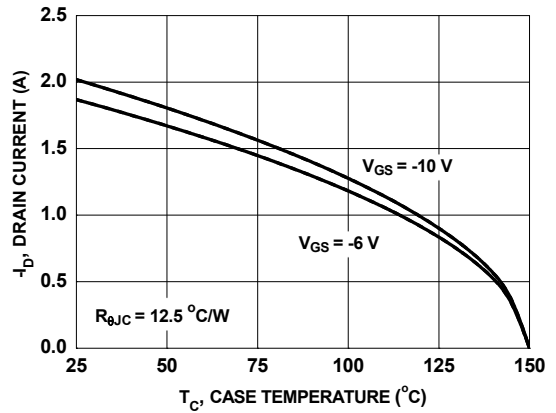
**Figure 20. Gate Charge Characteristics**



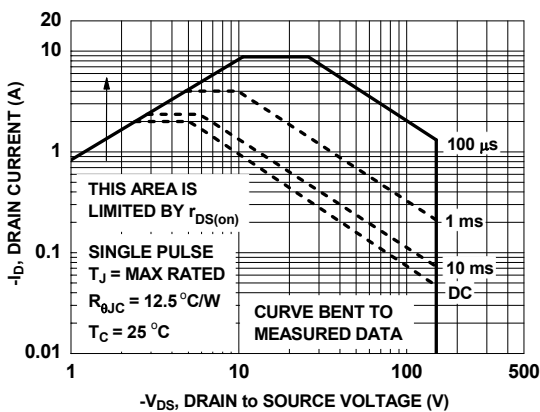
**Figure 21. Capacitance vs. Drain to Source Voltage**



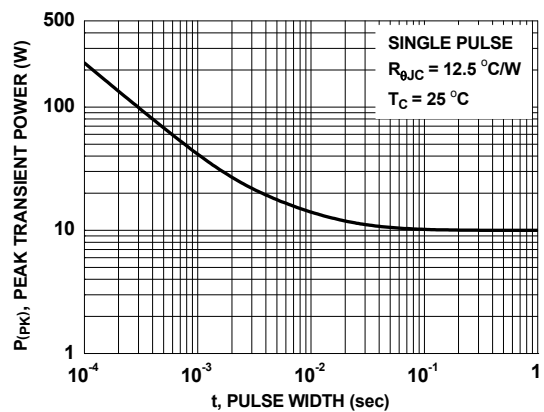
**Figure 22. Unclamped Inductive Switching Capability**



**Figure 23. Maximum Continuous Drain Current vs. Case Temperature**

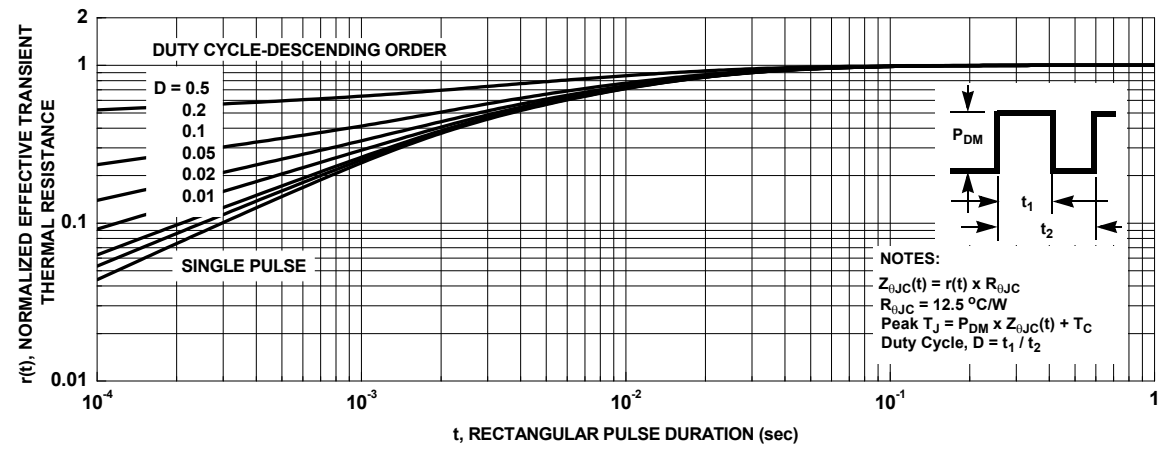


**Figure 24. Forward Bias Safe Operating Area**

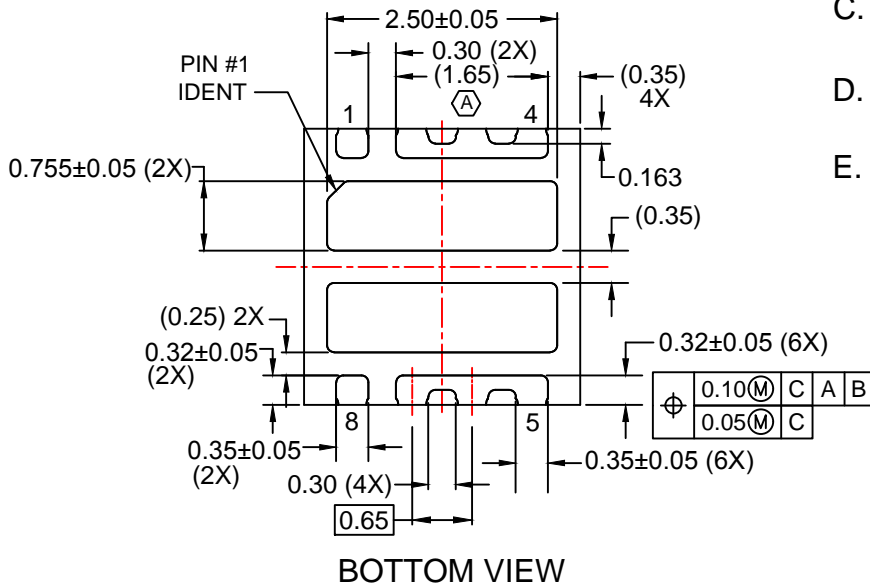
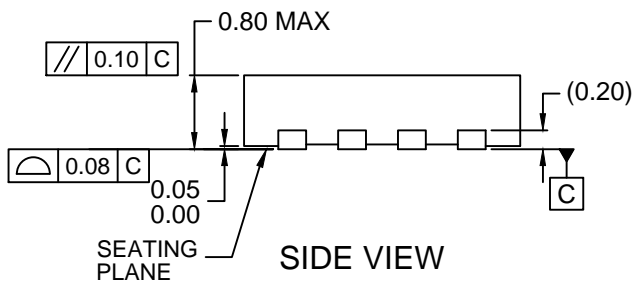
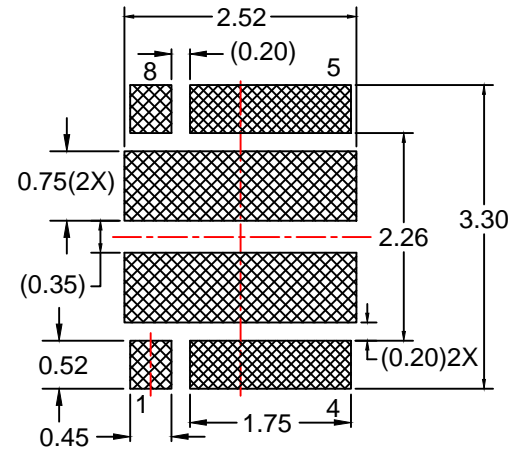
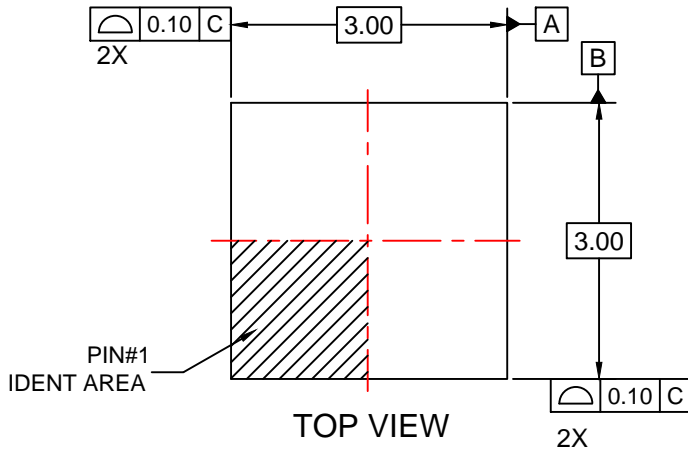


**Figure 25. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q2 P-Channel)  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted**



**Figure 26. Junction-to-Case Transient Thermal Response Curve**



### RECOMMENDED LAND PATTERN

#### NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
- E. DRAWING FILE NAME: MKT-MLP08Xrev2.

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