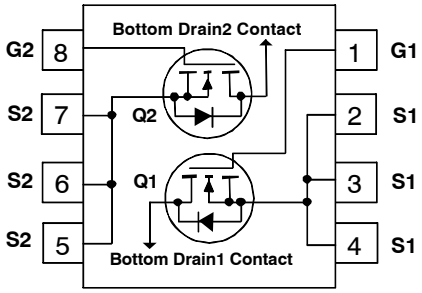
MOSFET – Dual N-Channel, POWERTRENCH®

40 V, 12 A, 10 mΩ

FDMC8030



General Description

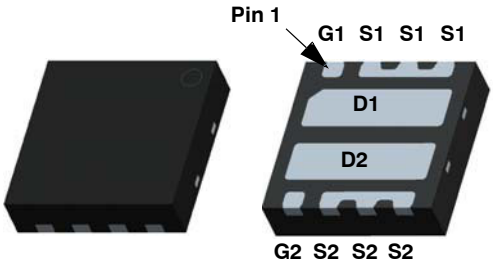
This device includes two 40 V N−Channel MOSFETs in a dual Power 33 (3 mm x 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

Features

- Max $r_{DS(on)}$ = 10 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 14 mΩ at V_{GS} = 4.5 V, I_D = 10 A
- Max $r_{DS(on)}$ = 28 mΩ at V_{GS} = 3.2 V, I_D = 4 A
- This Device is Pb−Free and is RoHS Compliant

Applications

- Battery Protection
- Load Switching
- Point of Load



Power 33

WDFN8 3x3, 0.65P
CASE 511DG

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		40	V
V_{GS}	Gate to Source Voltage	(Note 4)	±12	V
I_D	Drain Current – Continuous T_A = 25°C – Pulsed	(Note 1a)	 12 50	A
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	21	mJ
P_D	Power Dissipation T_C = 25°C		14	W
	Power Dissipation T_A = 25°C	(Note 1a)	1.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM

$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
FDMC8030	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	9.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	65	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	155	

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FDMC8030	FDMC8030	WDFN8 3x3, 0.65P, Power 33 (Pb−Free)	3000 units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.5	2.8	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		−5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A		8	10	mΩ
		V_{GS} = 4.5 V, I_D = 10 A		10	14	
		V_{GS} = 3.2 V, I_D = 4 A		19	28	
		V_{GS} = 10 V, I_D = 12 A, T_J = 125°C		13	16	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 12 A		57		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V f = 1 MHz		1462	1975	pF
C_{oss}	Output Capacitance			321	430	pF
C_{rss}	Reverse Transfer Capacitance			20	30	pF
R_g	Gate Resistance			0.9	2.5	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 20 V, I_D = 12 A V_{GS} = 10 V, R_{GEN} = 6 Ω		7	13	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn−Off Delay Time			19	33	ns
t_f	Fall Time			3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 20 V, I_D = 12 A		21	30	nC
	Total Gate Charge	V_{GS} = 0 V to 5 V, V_{DD} = 20 V, I_D = 12 A		12	17	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V I_D = 12 A		2.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.5		nC

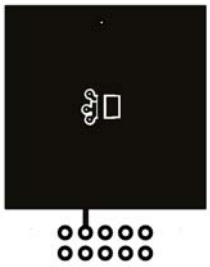
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 12 A (Note 2)		0.83	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 12 A, di/dt = 100 A/μs		25	40	ns
Q_{rr}	Reverse Recovery Charge			9	18	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 65°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 155°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 21 mJ is based on starting T_J = 25°C, L = 0.3 mH, I_{AS} = 12 A, V_{DD} = 36 V, V_{GS} = 10 V. 100% tested at L = 3 mH, I_{AS} = 5 A.
4. As an N−ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

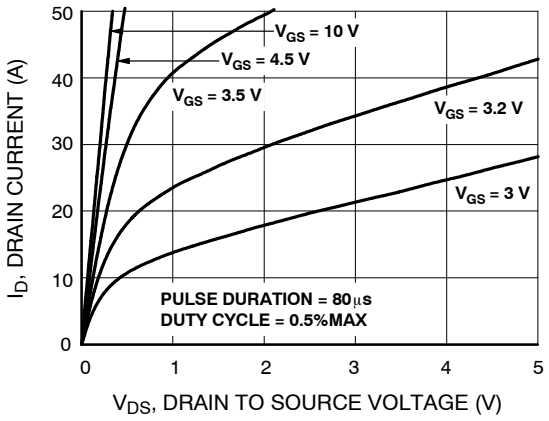


Figure 1. On−Region Characteristics

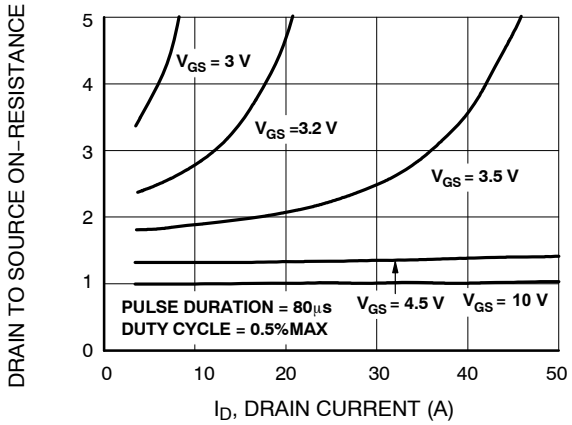


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

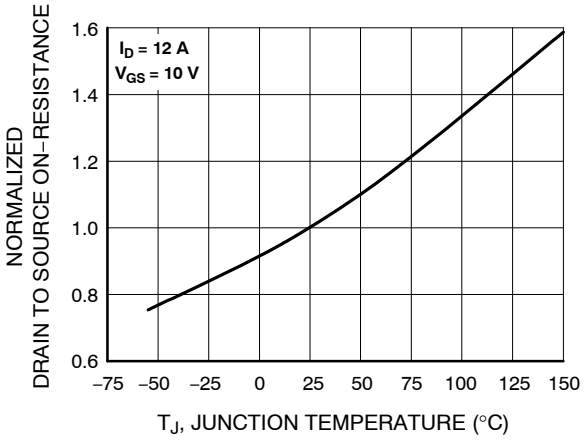


Figure 3. Normalized On−Resistance vs Junction Temperature

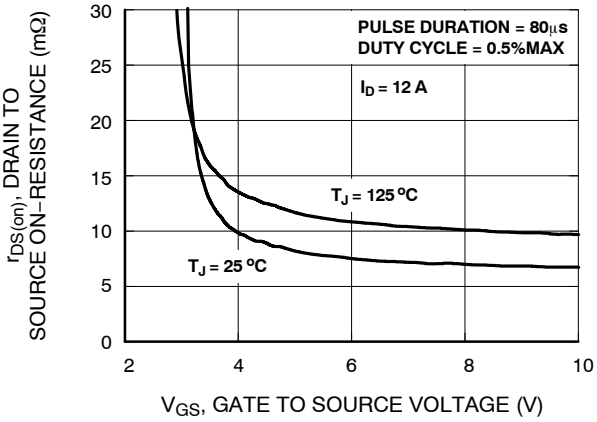


Figure 4. On−Resistance vs Gate to Source Voltage

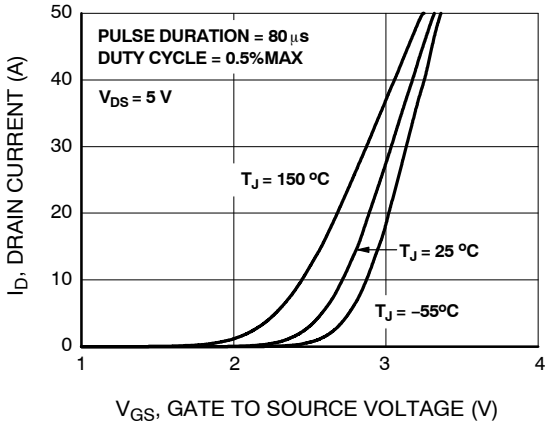


Figure 5. Transfer Characteristics

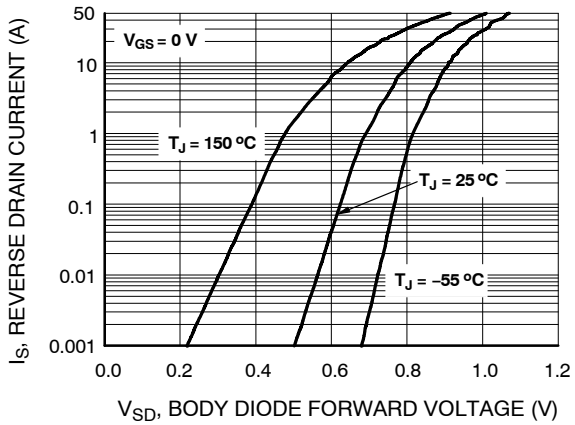


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

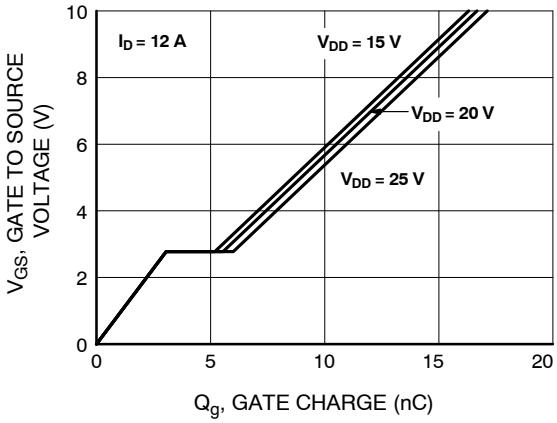


Figure 7. Gate Charge Characteristics

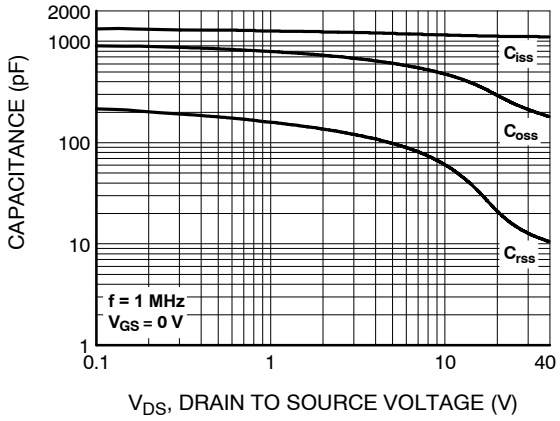


Figure 8. Capacitance vs Drain to Source Voltage

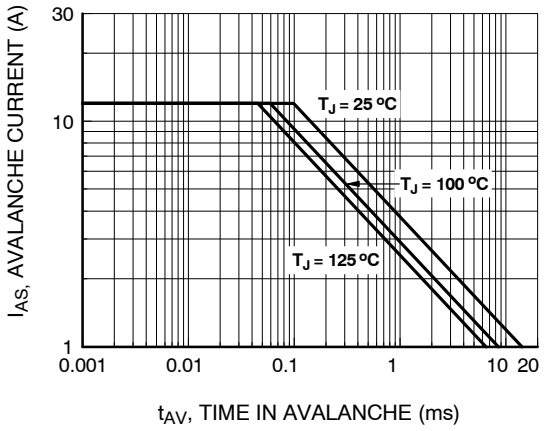


Figure 9. Unclamped Inductive Switching Capability

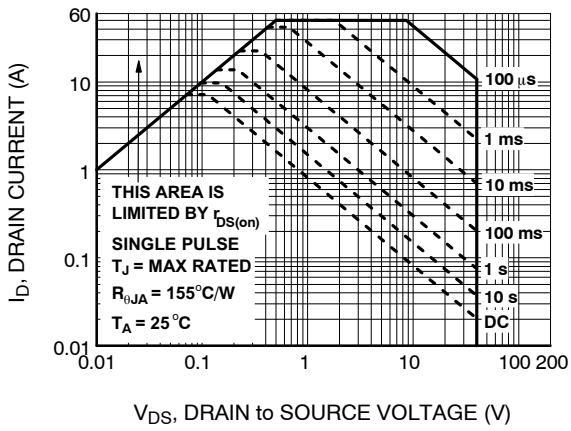


Figure 10. Forward Bias Safe Operating Area

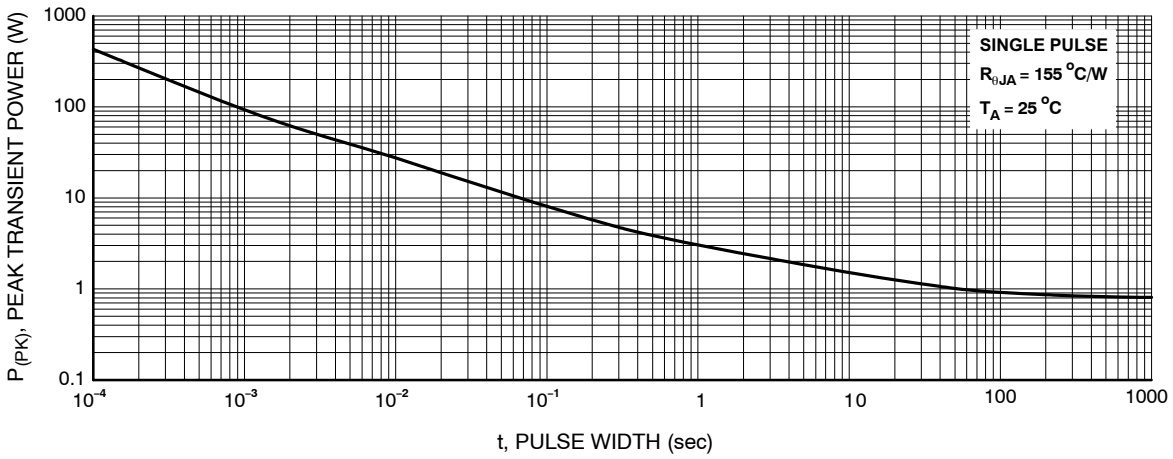


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

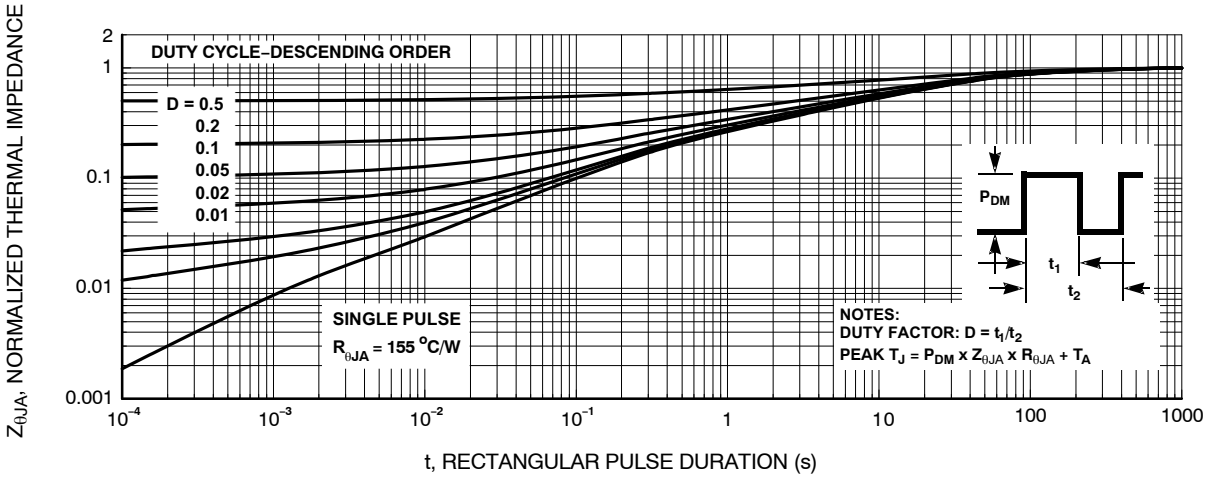


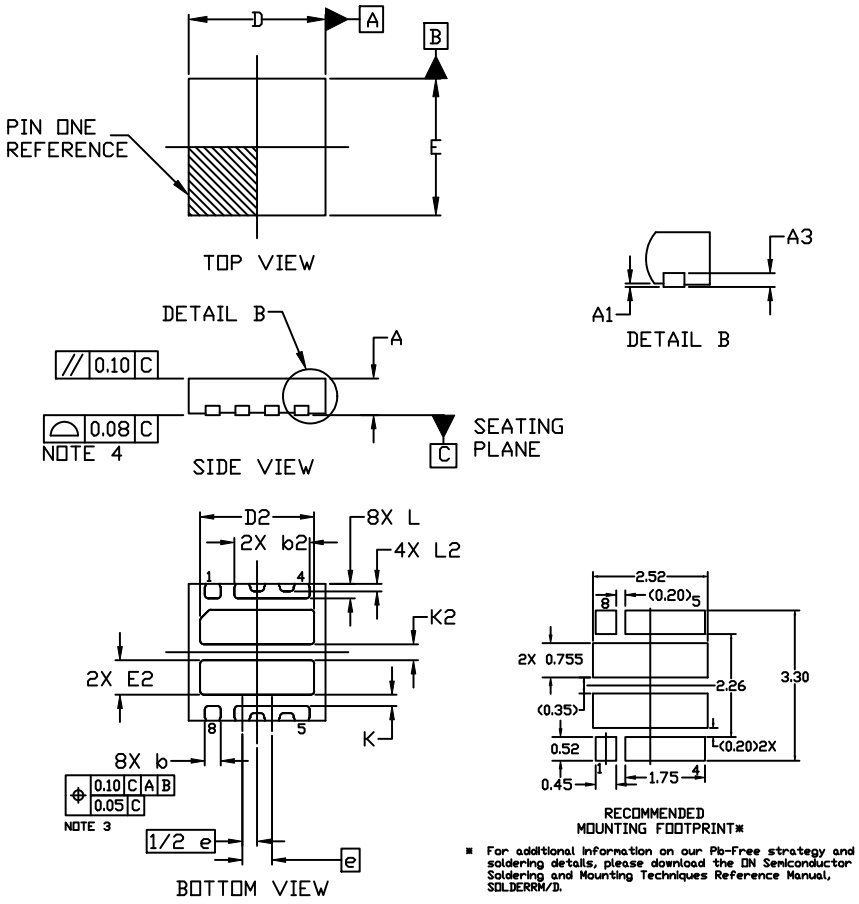
Figure 12. Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

WDFN8 3x3, 0.65P
CASE 511DG
ISSUE A

DATE 12 FEB 2019



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
b	0.30	0.35	0.40
b2		1.65 REF	
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e		0.65 BSC	
K	0.25	---	---
K2		0.35 REF	
L	0.27	0.32	0.37
L2		0.163 REF	

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3x3, 0.65P**		**PAGE 1 OF 1**

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