

MOSFET – N-Channel, POWERTRENCH[®], SyncFET™

30 V, 18 A, 9.3 mΩ

FDMC7692S

General Description

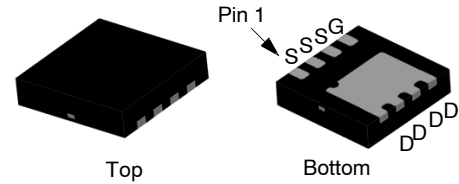
This FDMC7692S is produced using onsemi’s advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- Max $r_{DS(on)}$ = 9.3 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 12.5\text{ A}$
- Max $r_{DS(on)}$ = 13.6 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 10.4\text{ A}$
- High Performance Technology for Extremely Low $r_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

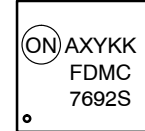
Applications

- DC – DC Buck Converters
- Notebook DC – DC Application



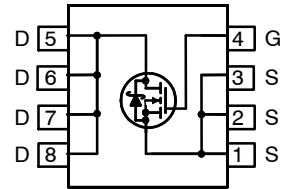
Top Bottom
 WDFN8 3.3x3.3, 0.65P
 CASE 511DQ (Option A)

MARKING DIAGRAM



FDMC7692S = Specific Device Code
 A = Assembly Location
 XY = 2-Digit Date Code
 KK = 2-Digit Lot Run Traceability Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMC7692S

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

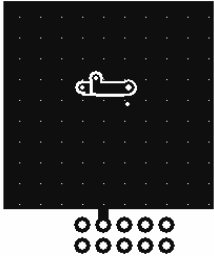
Symbol	Parameter	Rating	Unit			
V_{DS}	Drain to Source Voltage	30	V			
V_{GS}	Gate to Source Voltage	± 20	V			
I_D	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	18	A	
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$			12.5
		Pulsed				45
E_{AS}	Single Pulse Avalanche Energy (Note 2)	21	mJ			
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	27	W		
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.3			
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$			

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. E_{AS} of 21 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 0.3$ mH, $I_{AS} = 12.0$ A, $V_{DD} = 27$ V, $V_{GS} = 10$ V. 100% test at $L = 3$ mH, $I_{AS} = 3.2$ A.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0 V	30	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, referenced to 25°C	–	16	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	500	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS (Note 3)

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 1 mA	1.2	2.0	3.0	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 10 mA, referenced to 25°C	–	–5	–	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 12.5 A	–	7.8	9.3	mΩ
		V _{GS} = 4.5 V, I _D = 10.4 A	–	10.8	13.6	
		V _{GS} = 10 V, I _D = 12.5 A, T _J = 125°C	–	9.6	13.0	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 12.5 A	–	62	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	–	1040	1385	pF
C _{oss}	Output Capacitance		–	445	590	pF
C _{rss}	Reverse Transfer Capacitance		–	40	60	pF
R _g	Gate Resistance	f = 1 MHz	–	1.1	2.9	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 12.5 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	9	17	ns
t _r	Rise Time		–	3	10	ns
t _{d(off)}	Turn-Off Delay Time		–	19	34	ns
t _f	Fall Time		–	3	10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 15 V, I _D = 12.5 A	–	16	23	nC
		V _{GS} = 0 V to 4.5 V, V _{DD} = 15 V, I _D = 12.5 A	–	8	10	nC
Q _{gs}	Total Gate Charge	V _{DD} = 15 V, I _D = 12.5 A	–	4	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	2	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 12.5 A (Note 3)	–	0.9	1.3	V
		V _{GS} = 0 V, I _S = 0.9 A (Note 3)	–	0.5	0.7	
t _{rr}	Reverse Recovery Time	I _F = 12.5 A, di/dt = 300 A/μs	–	21	33	ns
Q _{rr}	Reverse Recovery Charge		–	16	29	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

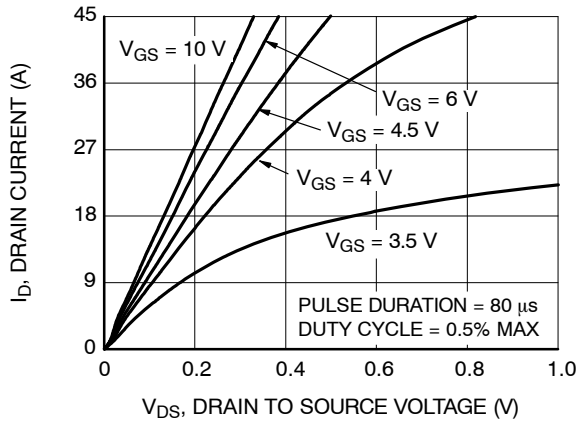


Figure 1. On Region Characteristics

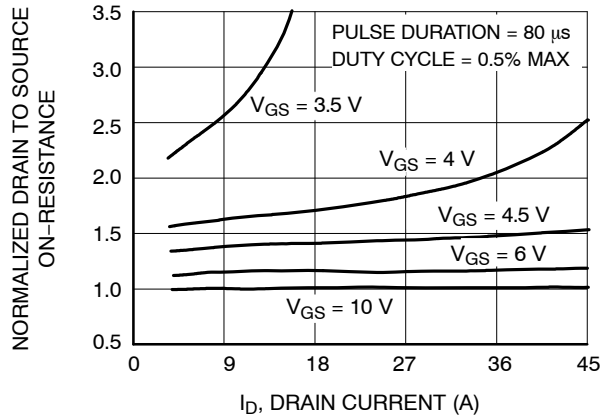


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

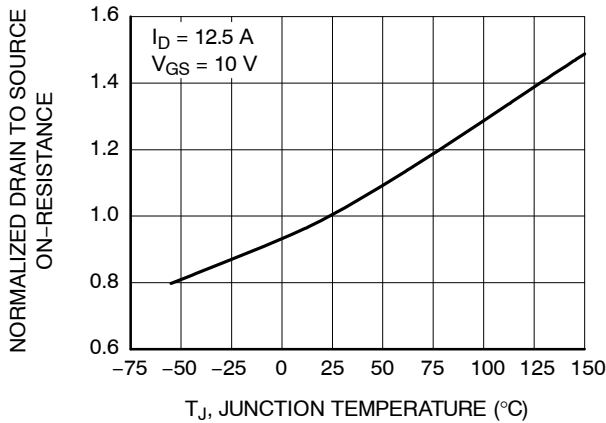


Figure 3. Normalized On Resistance vs. Junction Temperature

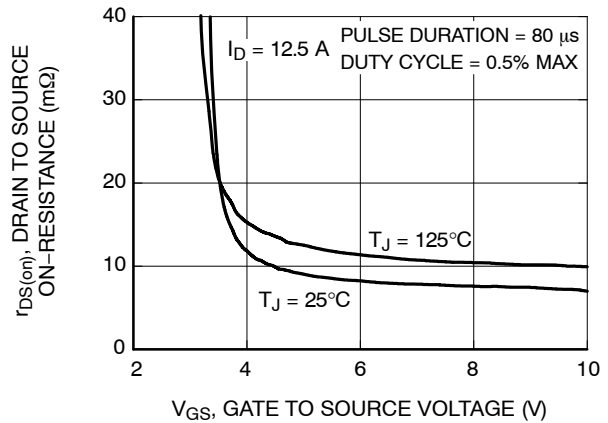


Figure 4. On-Resistance vs. Gate to Source Voltage

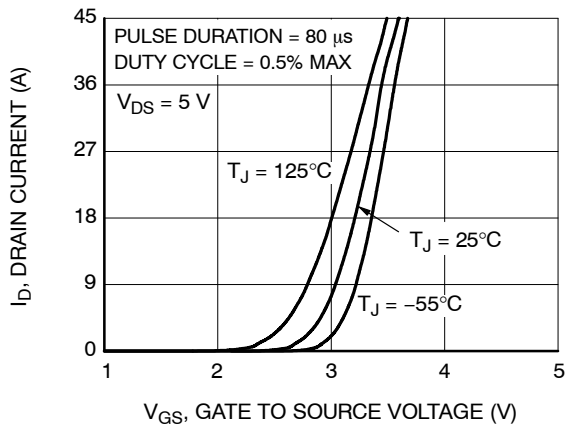


Figure 5. Transfer Characteristics

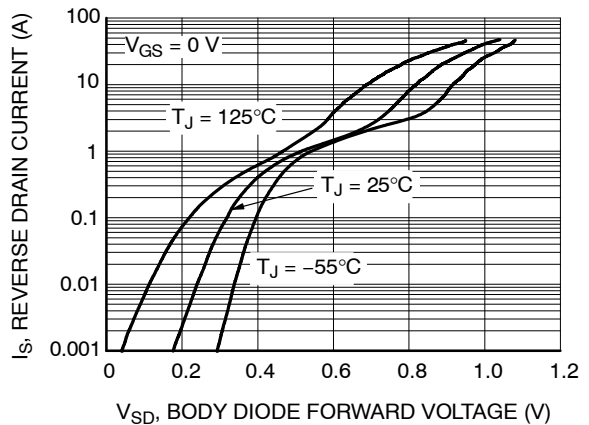


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

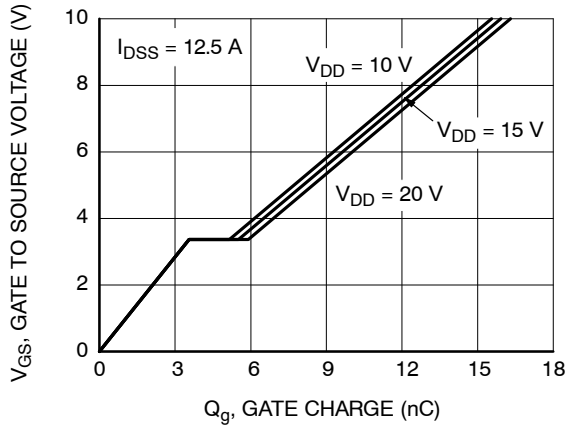


Figure 7. Gate Charge Characteristics

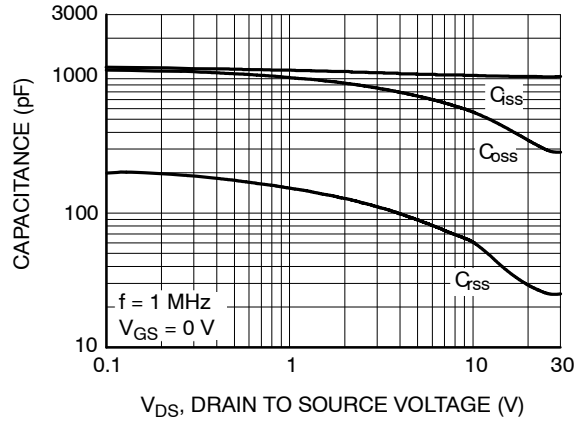


Figure 8. Capacitance vs. Drain to Source Voltage

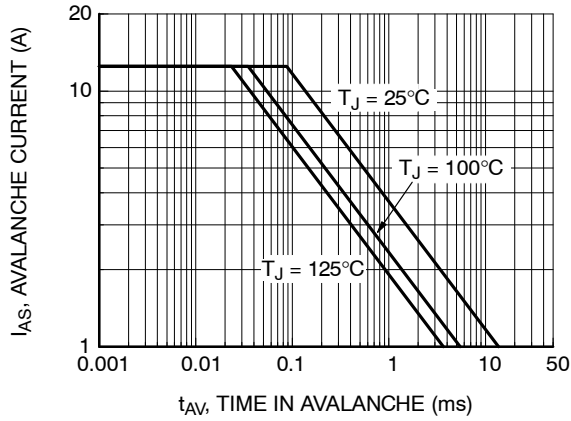


Figure 9. Unclamped Inductive Switching Capability

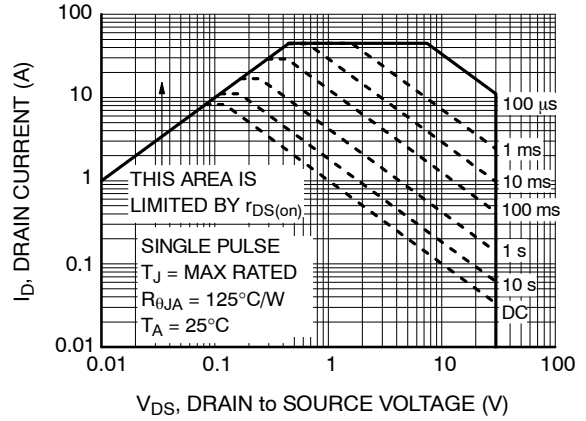


Figure 10. Forward Bias Safe Operating Area

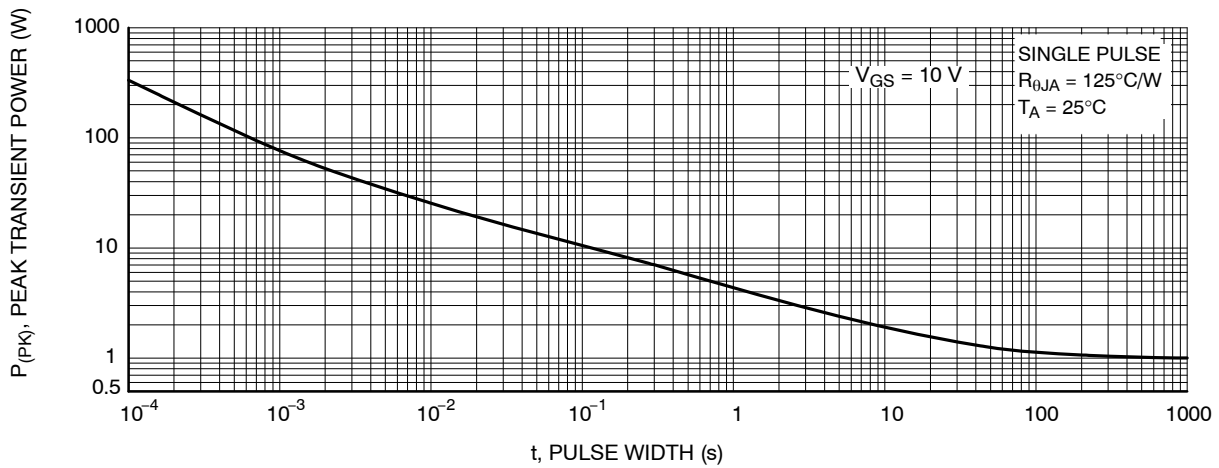


Figure 11. Single Pulse Maximum Power Dissipation

FDMC7692S

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

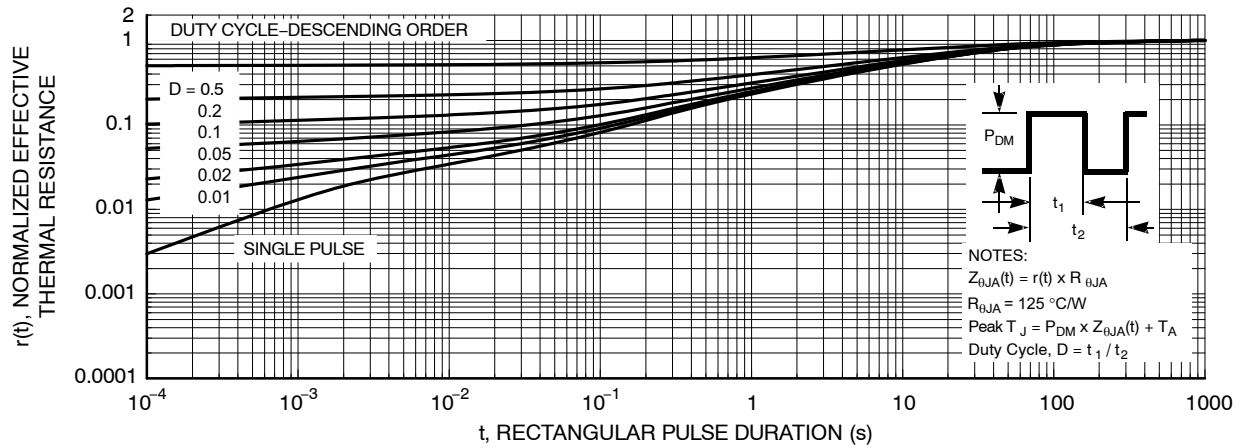


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDMC7692S	FDMC7692S	WDFN8 3.3x3.3, 0.65P case 511DQ (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

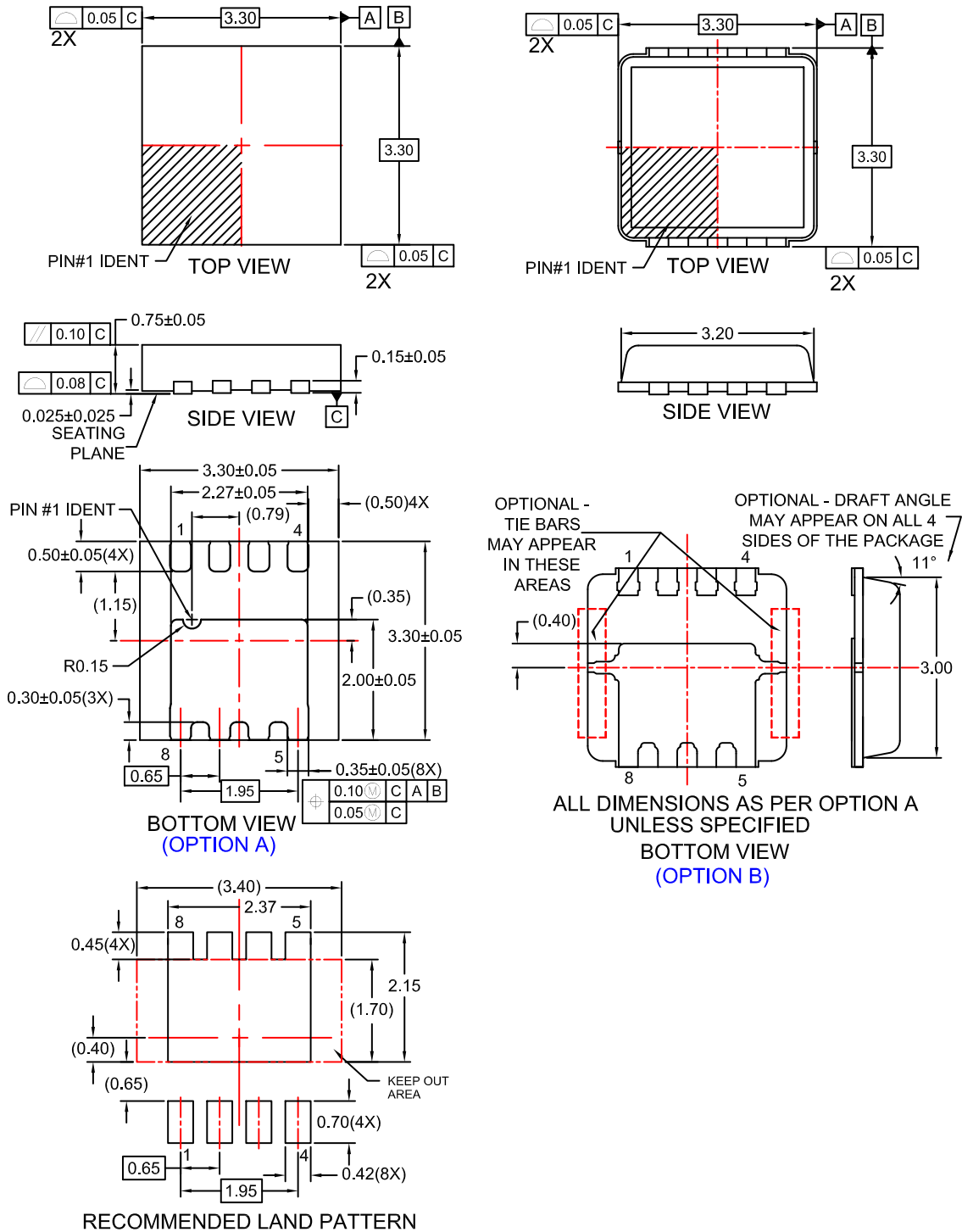


WDFN8 3.3x3.3, 0.65P

CASE 511DQ

ISSUE O

DATE 31 OCT 2016

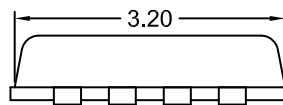
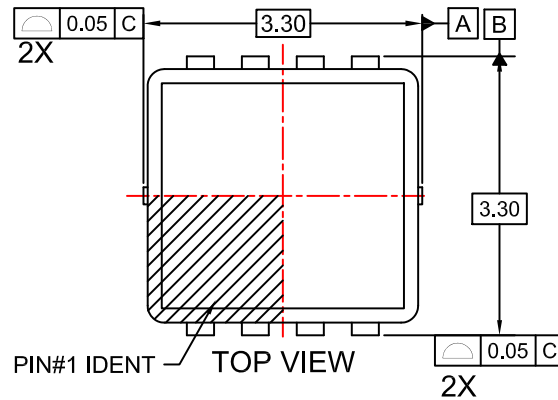


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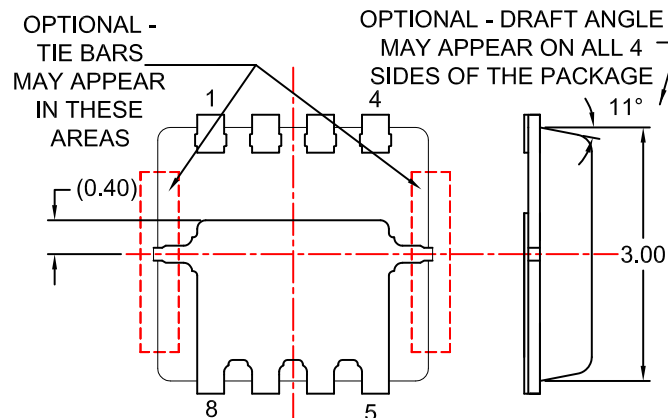
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CASE 511DQ
ISSUE O

DATE 31 OCT 2016



SIDE VIEW



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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