

MOSFET – P-Channel, POWERTRENCH®

-30 V, -18 A, 20 mΩ

FDMC4435BZ, FDMC4435BZ-F127

General Description

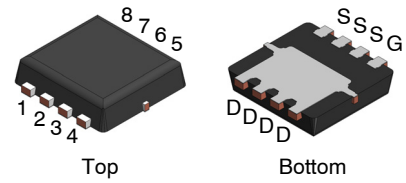
This P-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

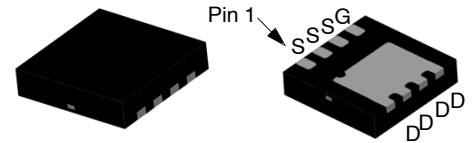
- Max $r_{DS(on)}$ = 20 mΩ at $V_{GS} = -10$ V, $I_D = -8.5$ A
- Max $r_{DS(on)}$ = 37 mΩ at $V_{GS} = -4.5$ V, $I_D = -6.3$ A
- Extended V_{GSS} Range (-25 V) for Battery Applications
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability
- HBM ESD Protection Level > 7 kV Typical*
- 100% UIL Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

- High Side in DC – DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook

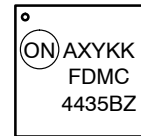


WDFN8 3.3x3.3, 0.65P
CASE 511DR
FDMC4435BZ

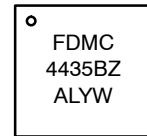


WDFN8 3.3x3.3, 0.65P
CASE 511DQ
FDMC4435BZ-F127

MARKING DIAGRAM



FDMC4435BZ



FDMC4435BZ-F127

FDMC4435BZ = Specific Device Code

A = Assembly Location

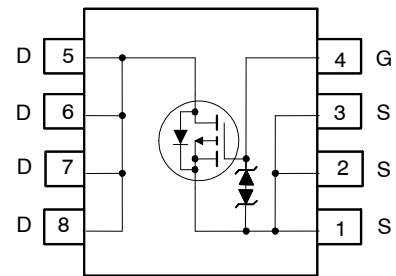
XY = 2-Digit Date Code

KK = 2-Digit Lot Run Traceability Code

L = Wafer Lot Number

YW = Assembly Start Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

*The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

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MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

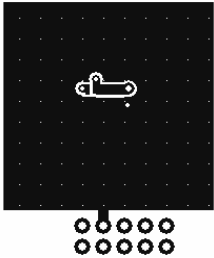
Symbol	Parameter	Rating	Unit	
V_{DS}	Drain to Source Voltage	-30	V	
V_{GS}	Gate to Source Voltage	± 25	V	
I_D	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	A
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	
		Pulsed		
E_{AS}	Single Pulse Avalanche Energy (Note 2)	32	mJ	
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	31	W
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to + 150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

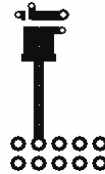
THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Starting $T_J = 25^\circ\text{C}$; P-ch: $L = 1 \text{ mH}$, $I_{AS} = -8 \text{ A}$, $V_{DD} = -27 \text{ V}$, $V_{GS} = -10 \text{ V}$.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-30			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C		21		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -24 V, V _{GS} = 0 V, T _J = 125°C			-100	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±25 V, V _{DS} = 0 V			±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-1.0	-1.8	-3.0	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C		-5		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -10 V, I _D = -8.5 A		14	20	mΩ
		V _{GS} = -4.5 V, I _D = -6.3 A		21	37	
		V _{GS} = -10 V, I _D = -8.5 A, T _J = 125°C		20	29	
g _{FS}	Forward Transconductance	V _{DD} = -5 V, I _D = -8.5 A		25		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz		1535	2040	pF
C _{oss}	Output Capacitance			310	410	pF
C _{rss}	Reverse Transfer Capacitance			280	420	pF
R _g	Gate Resistance	f = 1 MHz		4		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -15 V, I _D = -8.5 A, V _{GS} = -10 V, R _{GEN} = 6 Ω		10	20	ns
t _r	Rise Time			9	18	ns
t _{d(off)}	Turn-Off Delay Time			35	56	ns
t _f	Fall Time			19	34	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to -10 V, V _{DD} = -15 V, I _D = -8.5 A		38	53	nC
		V _{GS} = 0 V to -4.5 V, V _{DD} = -15 V, I _D = -8.5 A		20	28	nC
Q _{gs}	Gate to Source Charge	V _{DD} = -15 V, I _D = -8.5 A		4.3		nC
Q _{gd}	Gate to Drain "Miller" Charge			11		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -8.5 A (Note 3)		0.86	1.5	V
		V _{GS} = 0 V, I _S = -1.9 A (Note 3)		0.74	1.2	
t _{rr}	Reverse Recovery Time	I _F = -8.5 A, di/dt = 100 A/μs		26	40	ns
Q _{rr}	Reverse Recovery Charge			12	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

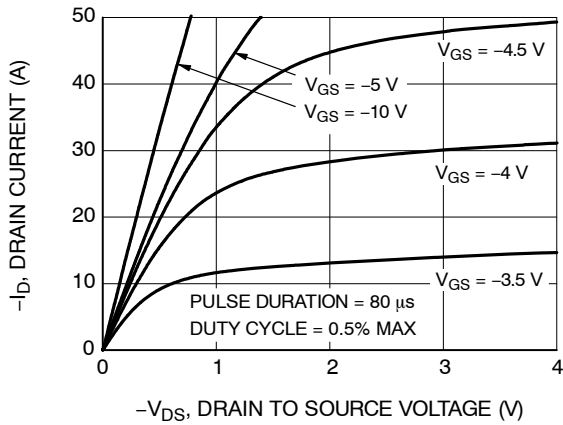


Figure 1. On Region Characteristics

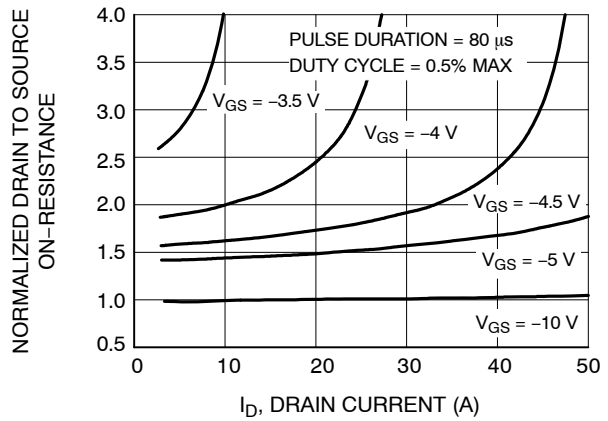


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

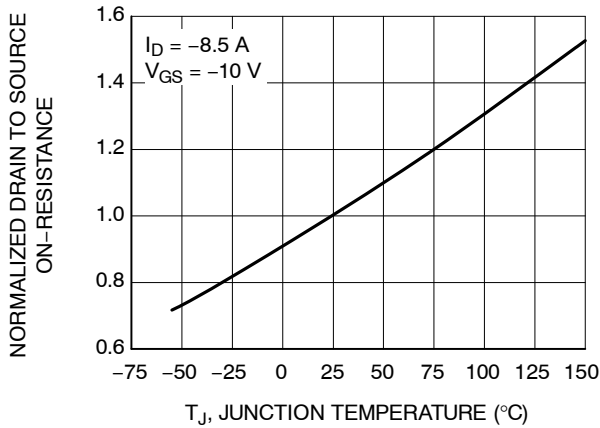


Figure 3. Normalized On Resistance vs. Junction Temperature

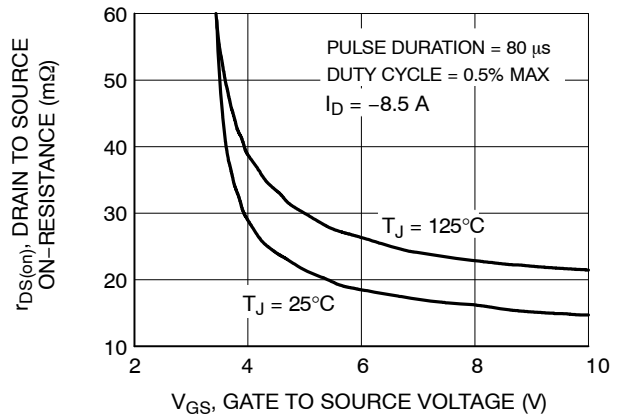


Figure 4. On-Resistance vs. Gate to Source Voltage

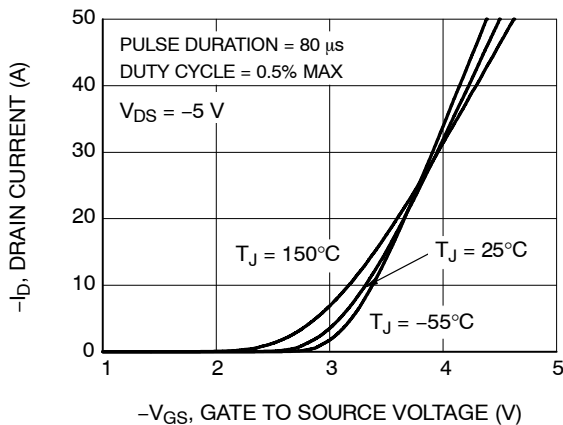


Figure 5. Transfer Characteristics

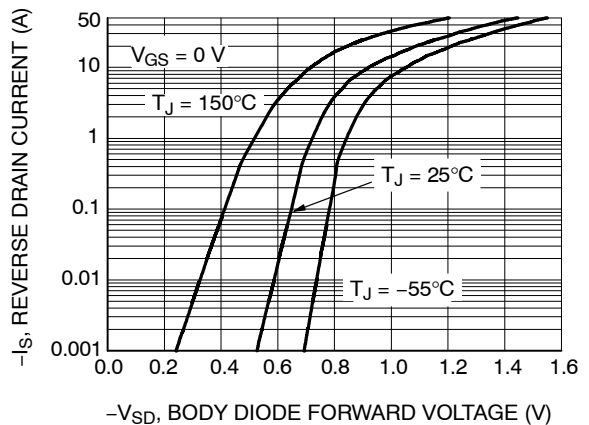


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

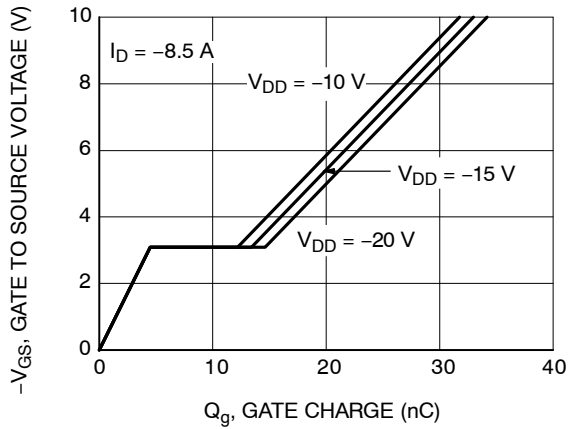


Figure 7. Gate Charge Characteristics

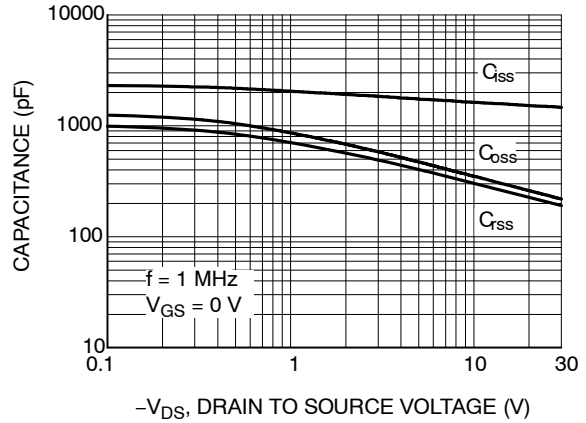


Figure 8. Capacitance vs. Drain to Source Voltage

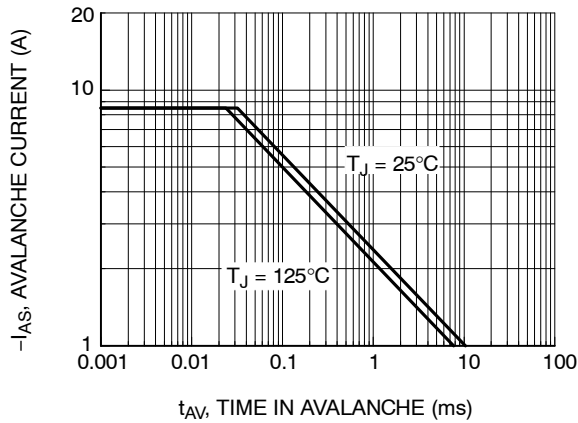


Figure 9. Unclamped Inductive Switching Capability

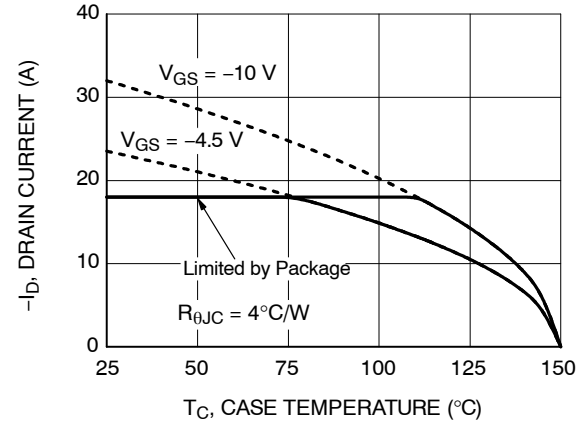


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

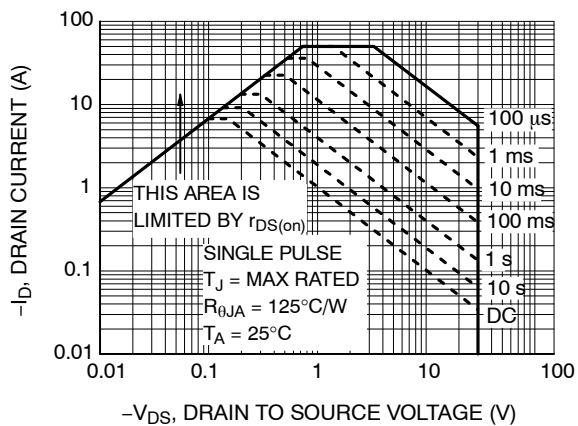


Figure 11. Forward Bias Safe Operating Area

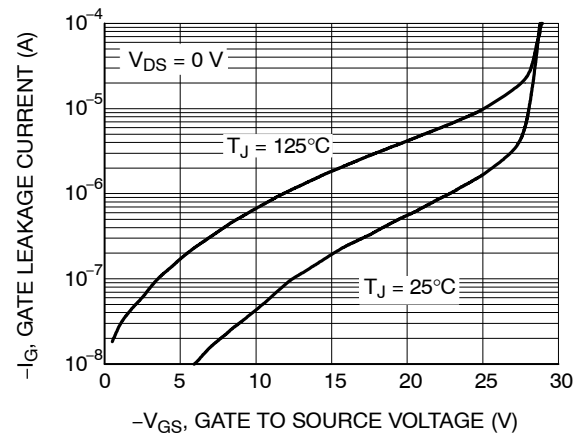


Figure 12. I_{GSS} vs. V_{GSS}

FDMC4435BZ, FDMC4435BZ-F127

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

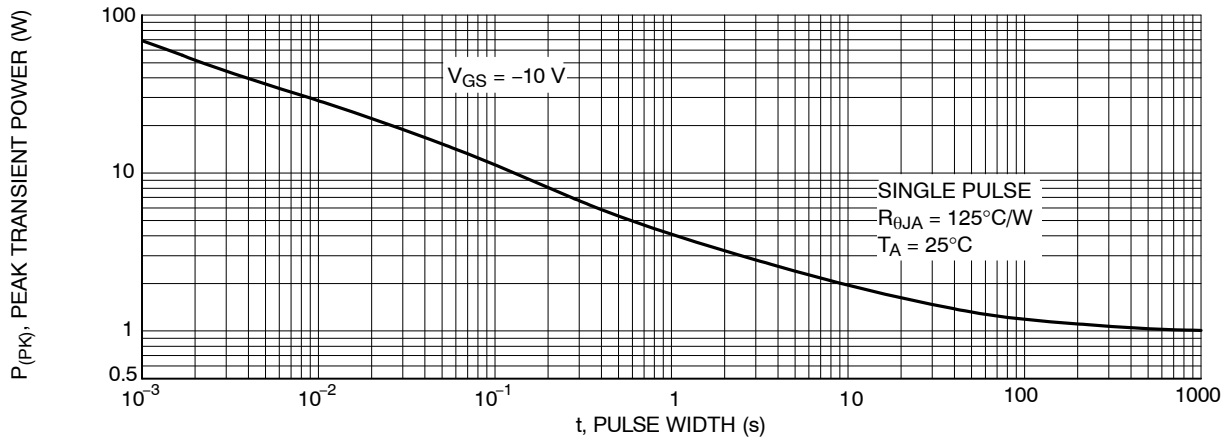


Figure 13. Single Pulse Maximum Power Dissipation

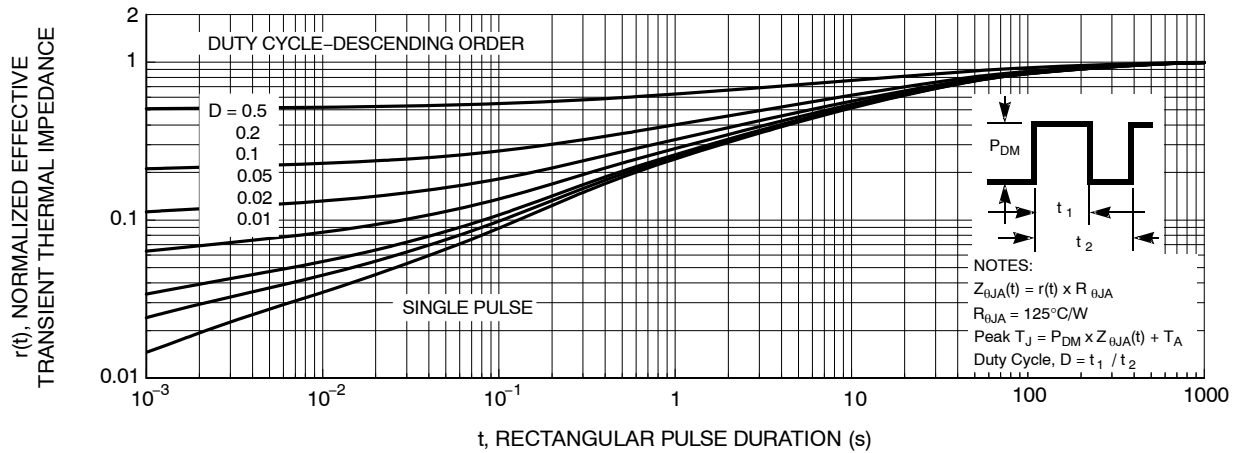


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDMC4435BZ	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DR (Pb-Free)	3000 / Tape & Reel
FDMC4435BZ-F127	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DQ (Pb-Free)	3000 / Tape & Reel
FDMC4435BZ-F127-L701	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DQ (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

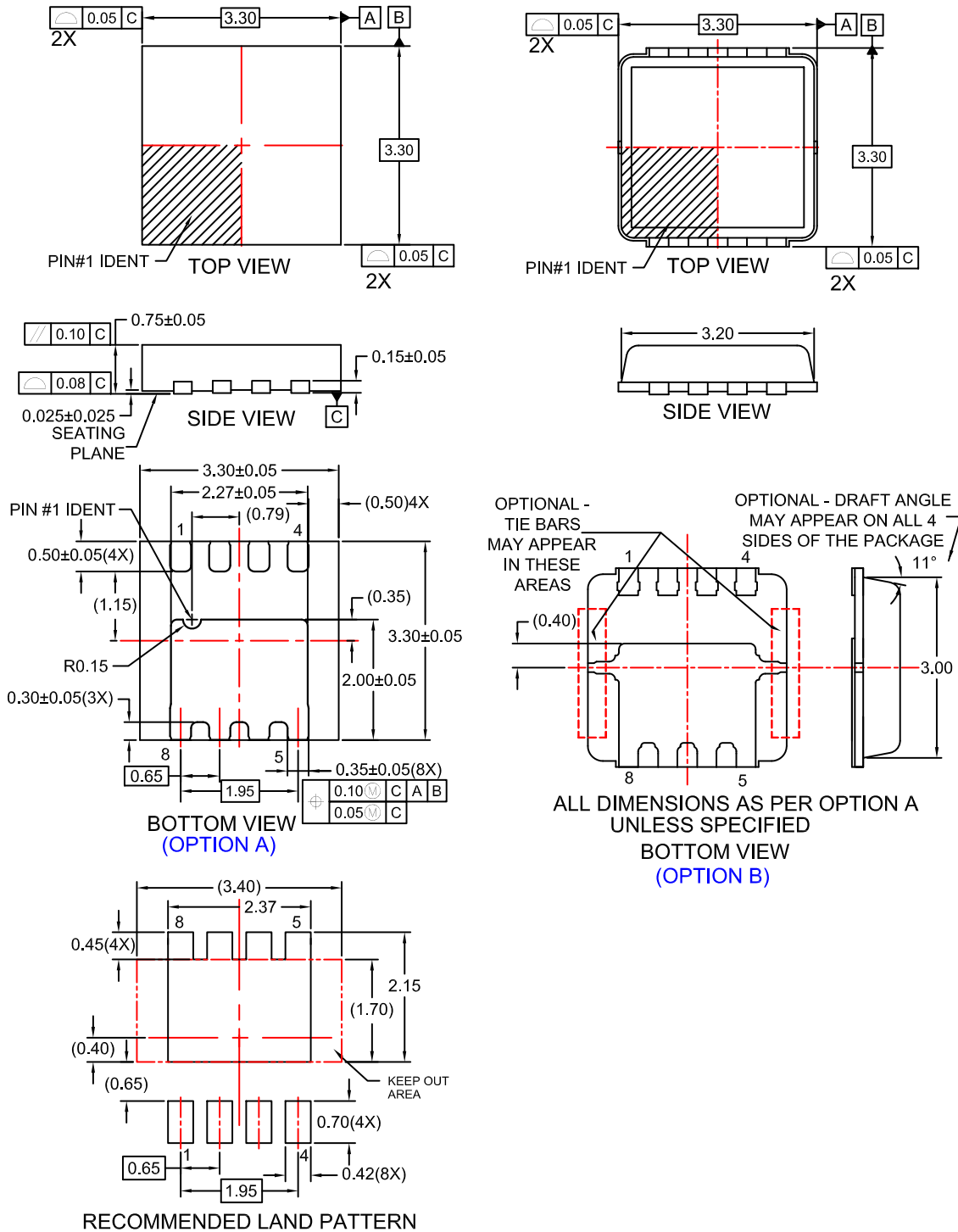


WDFN8 3.3x3.3, 0.65P

CASE 511DQ

ISSUE O

DATE 31 OCT 2016

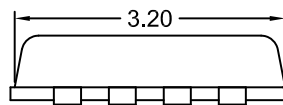
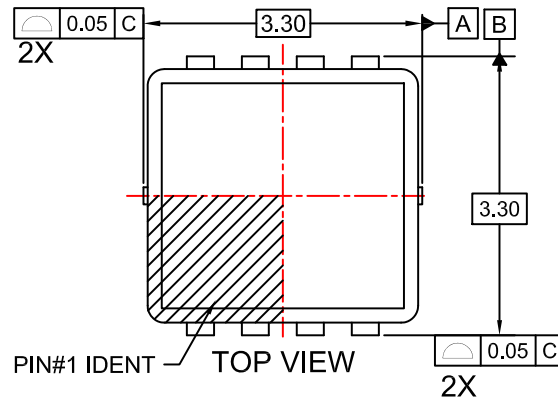


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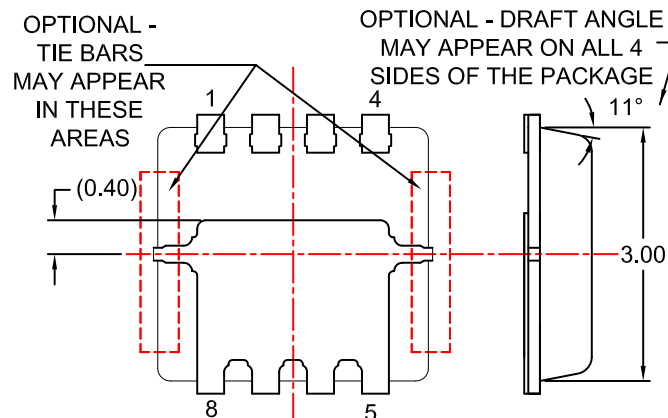
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WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

DATE 31 OCT 2016



SIDE VIEW



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

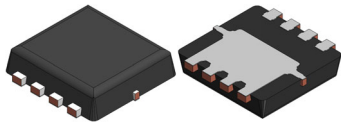
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- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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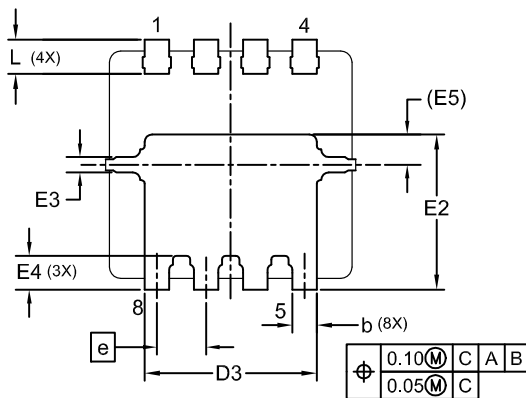
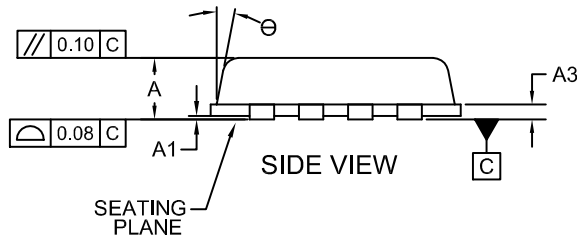
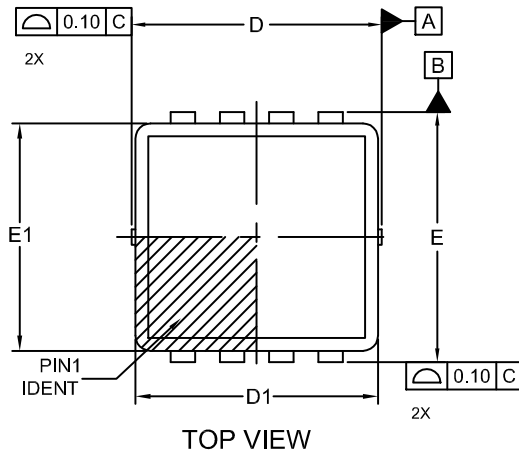
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

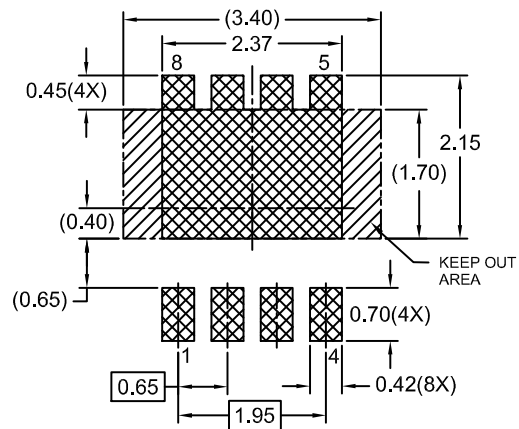
DATE 02 FEB 2022



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
θ	0°	-	12°

NOTES:

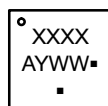
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RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

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