

MOSFET – N-Channel, POWERTRENCH®

100 V, 12 A, 110 mΩ

FDMC3612, FDMC3612-L701

General Description

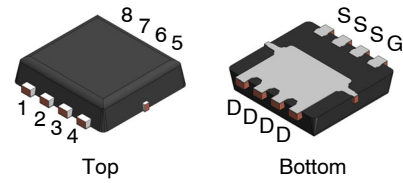
This N-Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Features

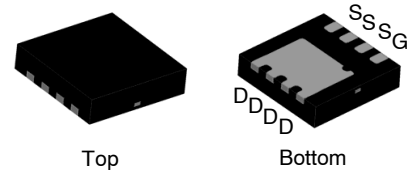
- Max $r_{DS(on)}$ = 110 mΩ at $V_{GS} = 10$ V, $I_D = 3.3$ A
- Max $r_{DS(on)}$ = 122 mΩ at $V_{GS} = 6$ V, $I_D = 3.0$ A
- Low Profile – 1 mm Max in Power 33
- 100% UIL Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC – DC Conversion
- PSE Switch

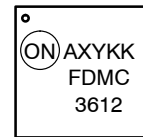


WDFN8 3.3x3.3, 0.65P
 CASE 511DR
 FDMC3612

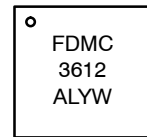


WDFN8 3.3x3.3, 0.65P
 CASE 511DQ
 FDMC3612-L701

MARKING DIAGRAM



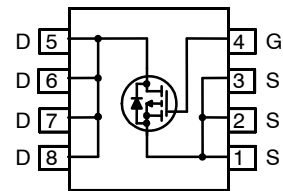
FDMC3612



FDMC3612-L701

FDMC3612 = Specific Device Code
 A = Assembly Location
 XY = 2-Digit Date Code
 KK = 2-Digit Lot Run Traceability Code
 L = Wafer Lot Number
 YW = Assembly Start Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

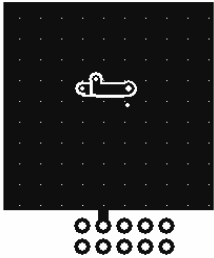
Symbol	Parameter	Rating	Unit	
V_{DS}	Drain to Source Voltage	100	V	
V_{GS}	Gate to Source Voltage	± 20	V	
I_D	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	A
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	
		Pulsed		
E_{AS}	Single Pulse Avalanche Energy (Note 2)	32	mJ	
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	35	W
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to + 150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

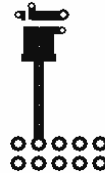
THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Starting $T_J = 25^\circ\text{C}$; N-ch: $L = 1 \text{ mH}$, $I_{AS} = 8 \text{ A}$, $V_{DD} = 90 \text{ V}$, $V_{GS} = 10 \text{ V}$.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	100	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	109	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	2.5	4.0	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–7	–	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 3.3 A	–	92	110	mΩ
		V _{GS} = 6 V, I _D = 3.0 A	–	98	122	
		V _{GS} = 10 V, I _D = 3.3 A, T _J = 125°C	–	177	212	
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 3.3 A	–	13	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	–	662	880	pF
C _{oss}	Output Capacitance		–	40	55	pF
C _{rss}	Reverse Transfer Capacitance		–	23	35	pF
R _g	Gate Resistance		–	1.3	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 50 V, I _D = 3.3 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	7.4	15	ns
t _r	Rise Time		–	2.8	10	ns
t _{d(off)}	Turn-Off Delay Time		–	19	34	ns
t _f	Fall Time		–	2	10	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 50 V, I _D = 3.3 A	–	14.4	21	nC
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 5 V, V _{DD} = 50 V, I _D = 3.3 A	–	7.9	12	nC
Q _{gs}	Total Gate Charge	V _{DD} = 50 V, I _D = 3.3 A	–	2.3	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	3.7	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 3.3 A (Note 3)	–	0.88	1.2	V
		V _{GS} = 0 V, I _S = 2 A (Note 3)	–	0.77	1.2	
t _{rr}	Reverse Recovery Time	I _F = 3.3 A, di/dt = 100 A/μs	–	34	55	ns
Q _{rr}	Reverse Recovery Charge		–	37	60	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

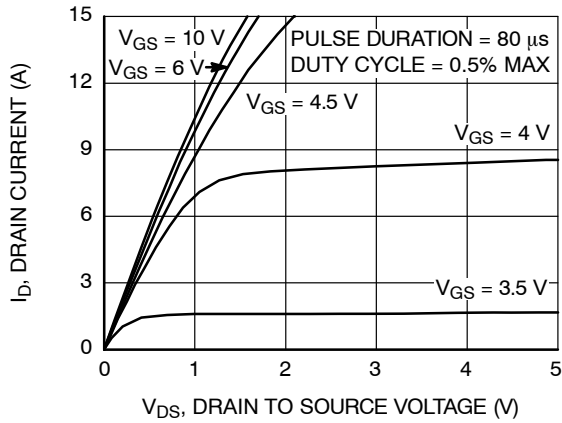


Figure 1. On Region Characteristics

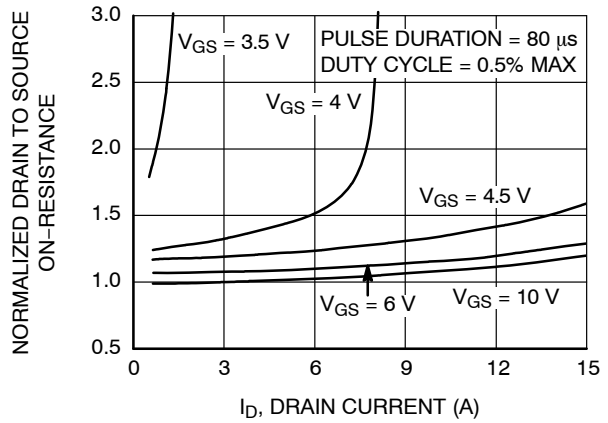


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

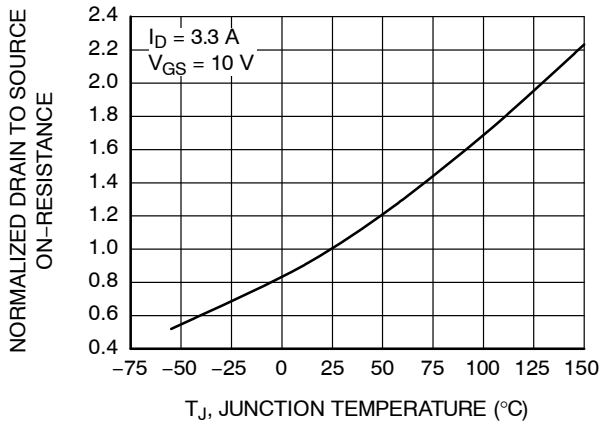


Figure 3. Normalized On Resistance vs. Junction Temperature

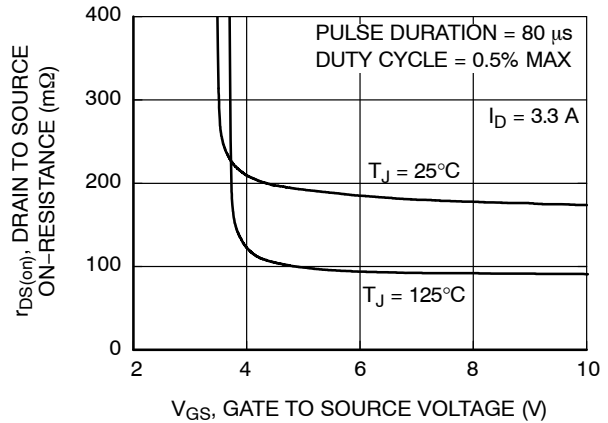


Figure 4. On-Resistance vs. Gate to Source Voltage

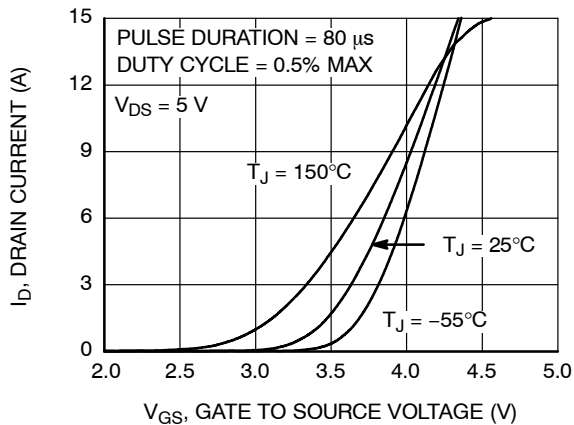


Figure 5. Transfer Characteristics

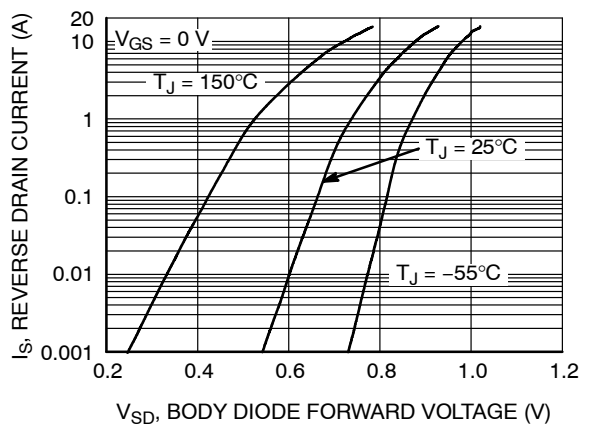


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDMC3612, FDMC3612-L701

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

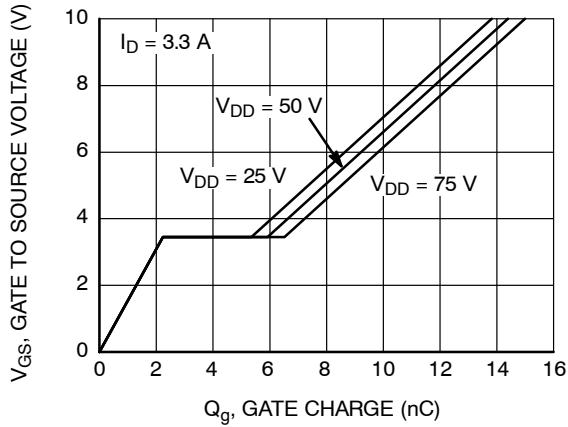


Figure 7. Gate Charge Characteristics

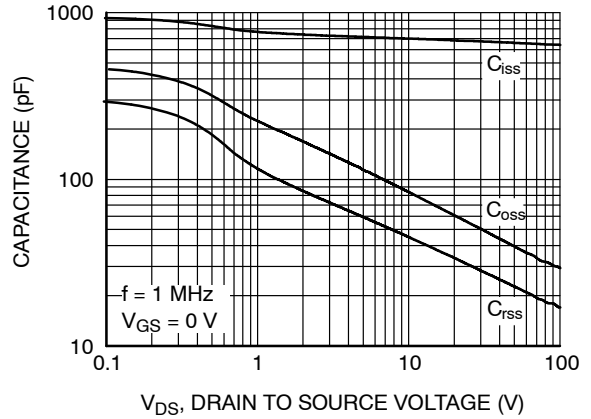


Figure 8. Capacitance vs. Drain to Source Voltage

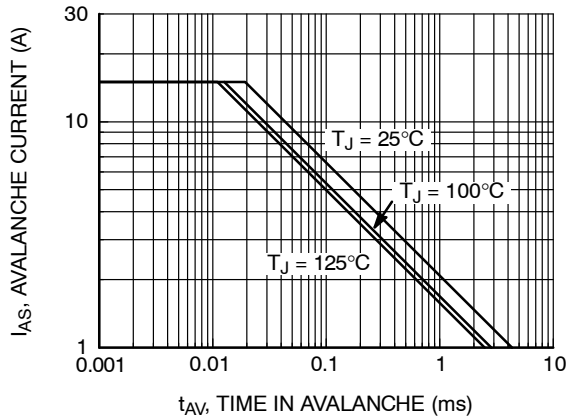


Figure 9. Unclamped Inductive Switching Capability

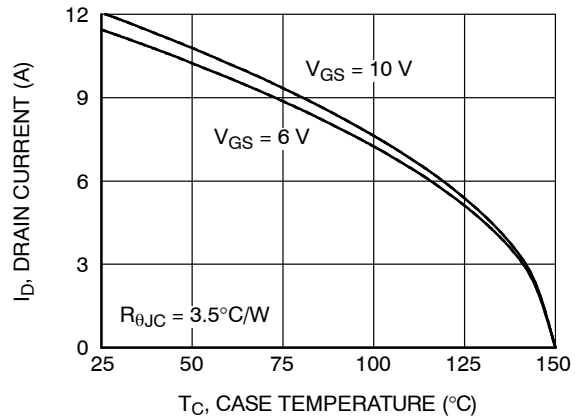


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

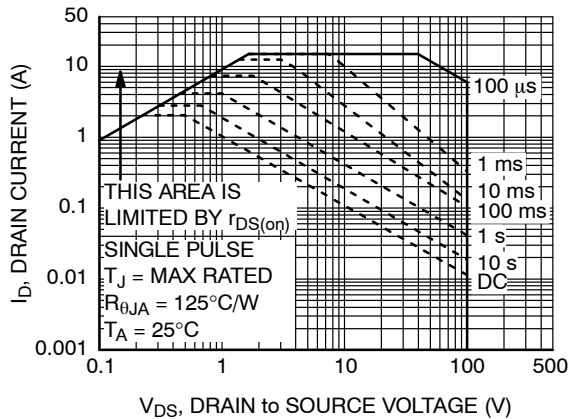


Figure 11. Forward Bias Safe Operating Area

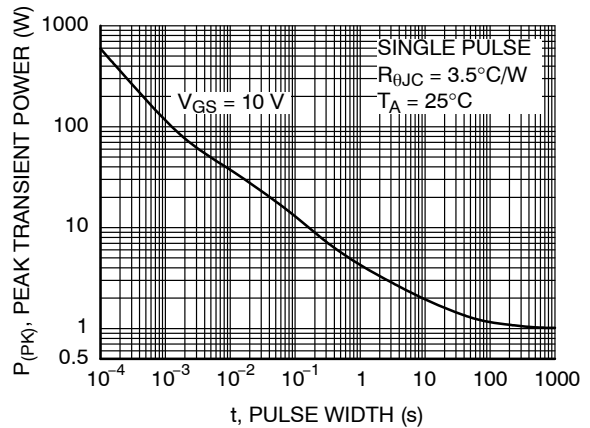


Figure 12. Single Pulse Maximum Power Dissipation

FDMC3612, FDMC3612-L701

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

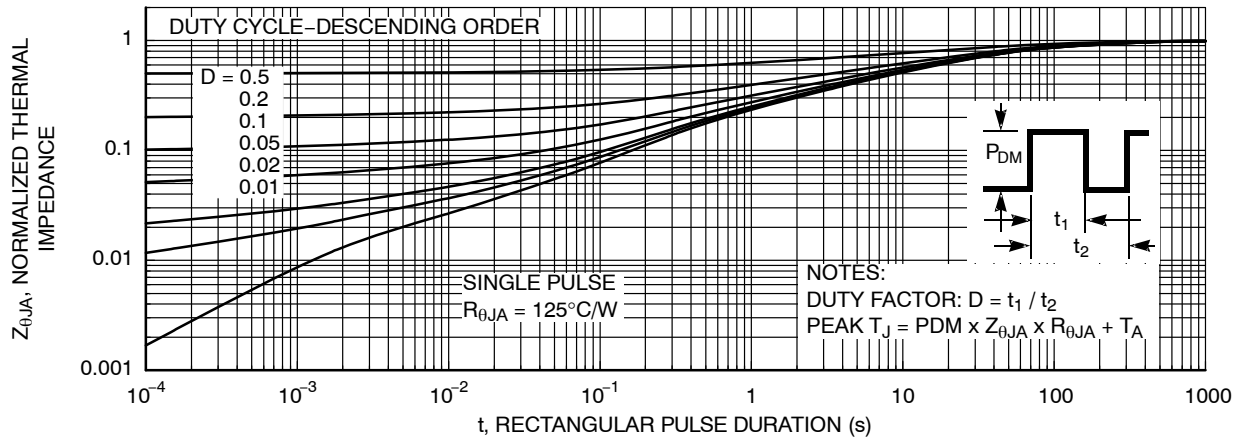


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC3612	FDMC3612	WDFN8 3.3x3.3, 0.65P Power 33 (Pb-Free)	13"	12 mm	3000 / Tape & Reel
FDMC3612-L701	FDMC3612	WDFN8 3.3x3.3, 0.65P Power 33 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

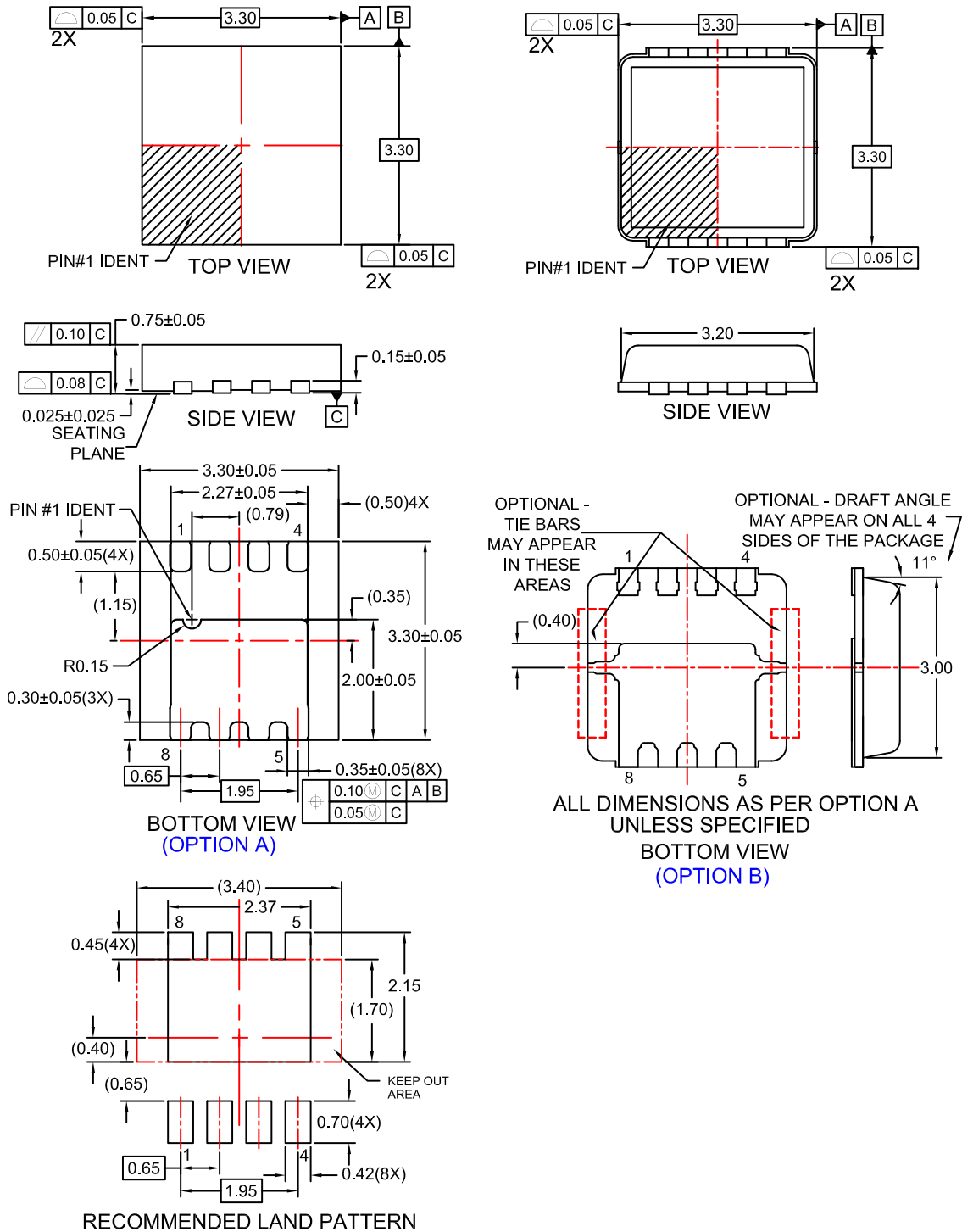


WDFN8 3.3x3.3, 0.65P

CASE 511DQ

ISSUE O

DATE 31 OCT 2016

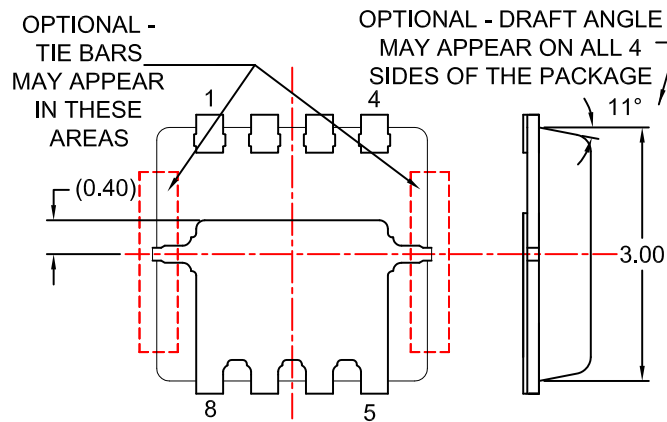
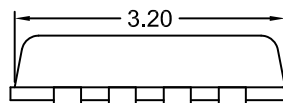
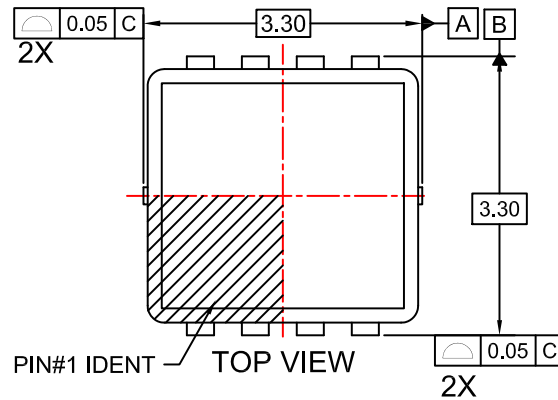


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WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

DATE 31 OCT 2016



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

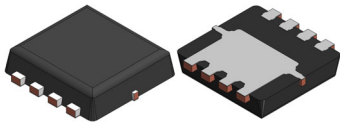
NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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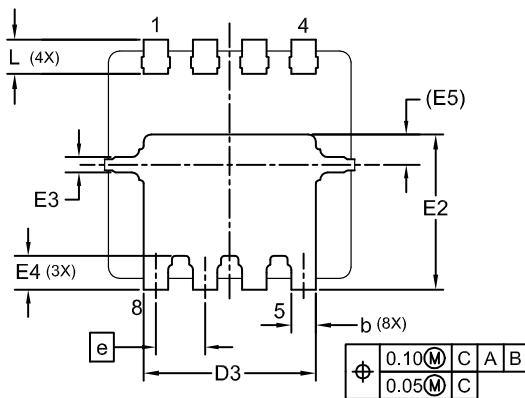
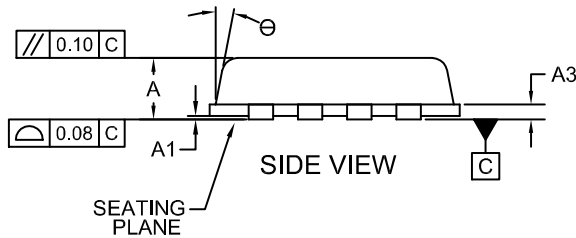
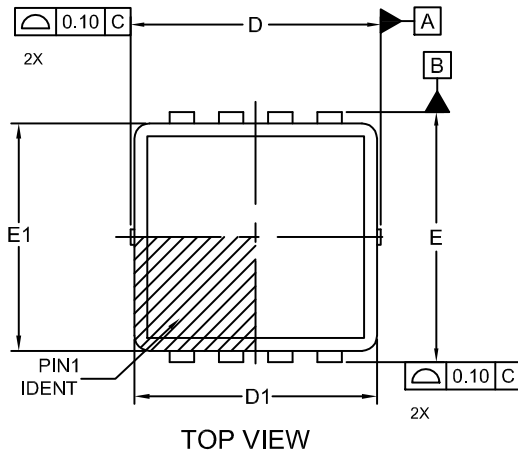
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

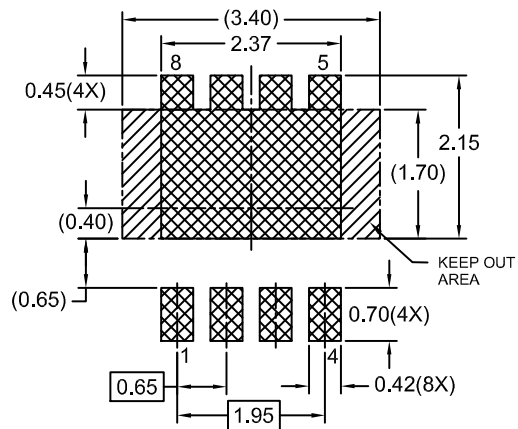
DATE 02 FEB 2022



NOTES:

- A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

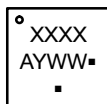
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
Θ	0°	-	12°



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

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Europe, Middle East and Africa Technical Support:

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