MOSFET – Dual, N-Channel, Common Drain, POWERTRENCH®

20 V, 9.7 A, 16.5 mΩ

FDMB2307NZ

V_{S1S2}	$r_{S1S2(on)}$ MAX	I_{S1S2} MAX
20 V	16.5 mΩ @ 4.5 V	9.7 A
	18 mΩ @ 4.2 V	
	21 mΩ @ 3.1 V	
	24 mΩ @ 2.5 V	

General Description

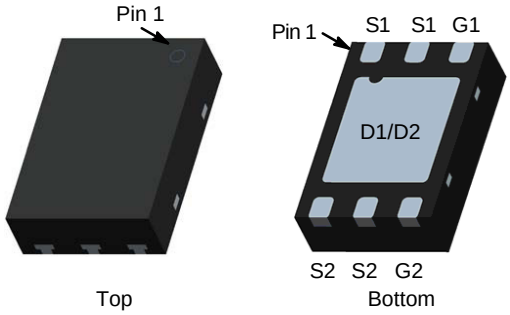
This device is designed specifically as a single package solution for Li−Ion battery pack protection circuit and other ultra−portable applications. It features two common drain N−channel MOSFETs, which enables bidirectional current flow, on **onsemi**'s advanced POWERTRENCH process with state of the art MicroFET ™ Leadframe, the FDMB2307NZ minimizes both PCB space and $r_{S1S2(on)}$.

Features

- Max $r_{S1S2(on)}$ = 16.5 mΩ at V_{GS} = 4.5 V, I_D = 8 A
- Max $r_{S1S2(on)}$ = 18 mΩ at V_{GS} = 4.2 V, I_D = 7.4 A
- Max $r_{S1S2(on)}$ = 21 mΩ at V_{GS} = 3.1 V, I_D = 7 A
- Max $r_{S1S2(on)}$ = 24 mΩ at V_{GS} = 2.5 V, I_D = 6.7 A
- Low Profile − 0.8 mm Maximum − in the New Package MicroFET 2x3 mm
- HBM ESD Protection Level > 2 kV (Note 3)
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- Li−Ion Battery Pack

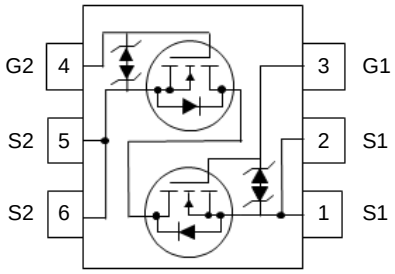


WDFN6 2x3, 0.65P
CASE 511CX

MARKING DIAGRAM

&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
307 = Specific Device Code

PIN ASSIGNMENT



MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{S1S2}	Source1 to Source2 Voltage	20	V
V_{GS}	Gate to Source Voltage (Note 4)	±12	V
I_{S1S2}	Source1 to Source2 Current −Continuous T_A = 25°C (Note 1a) −Pulsed	 9.7 40	A
P_D	Power Dissipation T_A = 25°C (Note 1a) T_A = 25°C (Note 1b)	 2.2 0.8	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	57	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	161	

ORDERING INFORMATION

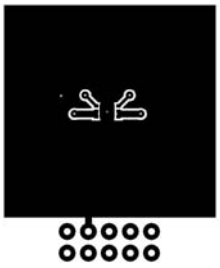
See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

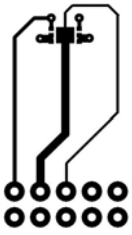
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
I_{S1S2}	Zero Gate Voltage Source1 to Source2 Current	V_{S1S2} = 16 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 12 V, V_{S1S2} = 0 V	–	–	10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{S1S2}, I_{S1S2} = 250 μA	0.6	1	1.5	V
$r_{S1S2(on)}$	Static Source1 to Source2 On Resistance	V_{GS} = 4.5 V, I_{S1S2} = 8 A	10.5	13.5	16.5	mΩ
		V_{GS} = 4.2 V, I_{S1S2} = 7.4 A	11	14	18	
		V_{GS} = 3.1 V, I_{S1S2} = 7 A	11.5	16	21	
		V_{GS} = 2.5 V, I_{S1S2} = 6.7 A	12	18	24	
		V_{GS} = 4.5 V, I_{S1S2} = 8 A, T_J = 125°C	11	20	29	
g_{FS}	Forward Transconductance	V_{S1S2} = 5 V, I_{S1S2} = 8 A	–	41	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{S1S2} = 10 V, V_{GS} = 0 V, f = 1 MHz	–	1760	2640	pF
C_{oss}	Output Capacitance		–	229	345	pF
C_{rss}	Reverse Transfer Capacitance		–	211	320	pF
R_g	Gate Resistance (Note 5)		0.1	2.6	8	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{S1S2} = 10 V, I_{S1S2} = 8 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	–	12	22	ns
t_r	Rise Time		–	19	34	ns
$t_{d(off)}$	Turn−Off Delay Time		–	32	51	ns
t_f	Fall Time		–	9.5	17	ns
Q_g	Total Gate Charge	V_{G1S1} = 0 V to 5 V, V_{S1S2} = 10 V, I_{S1S2} = 8 A, V_{G2S2} = 0 V	–	20	28	nC
Q_g	Total Gate Charge	V_{G1S1} = 0 V to 4.5 V, V_{S1S2} = 10 V, I_{S1S2} = 8 A, V_{G2S2} = 0 V	–	18	25	nC
Q_{gs}	Gate1 to Source1 Charge	V_{S1S2} = 10 V, I_{S1S2} = 8 A, V_{G2S2} = 0 V	–	2.8	–	nC
Q_{gd}	Gate1 to Source2 “Miller” Charge		–	5.3	–	nC
DRAIN−SOURCE CHARACTERISTICS						
I_{fss}	Maximum Continuous Source1−Source2 Diode Forward Current		–	–	8	A
V_{fss}	Source1 to Source2 Diode Forward Voltage	V_{G1S1} = 0 V, V_{G2S2} = 4.5 V, I_{fss} = 8 A (Note 2)	–	0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 57°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 161°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. As an N−ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.
5. Rg is measured on 100% of the die at wafer level.

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

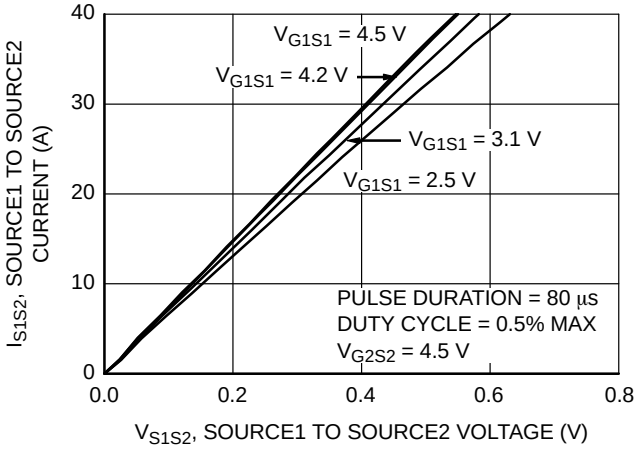


Figure 1. On−Region Characteristics

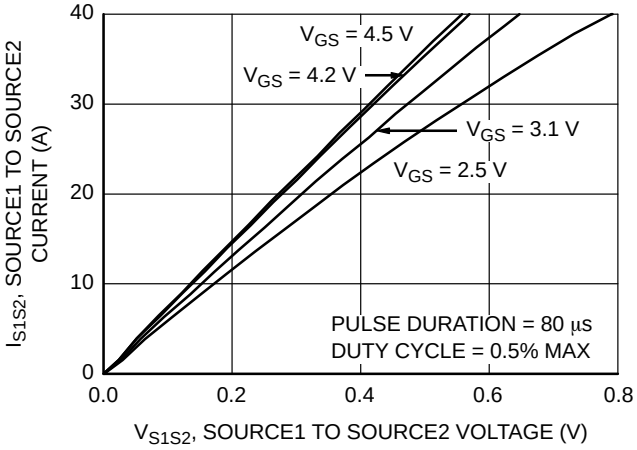


Figure 2. On−Region Characteristics

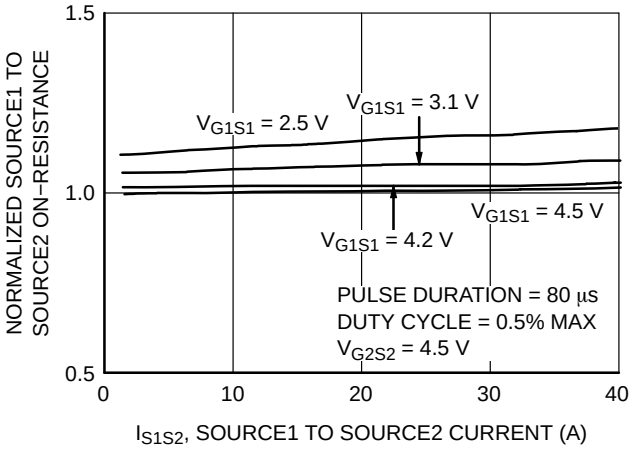


Figure 3. Normalized On−Resistance vs. Source1 to Source2 Current and Gate Voltage

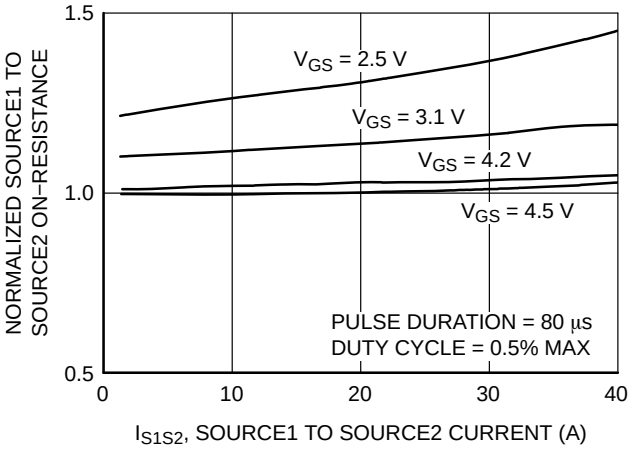


Figure 4. Normalized On−Resistance vs. Source1 to Source2 Current and Gate Voltage

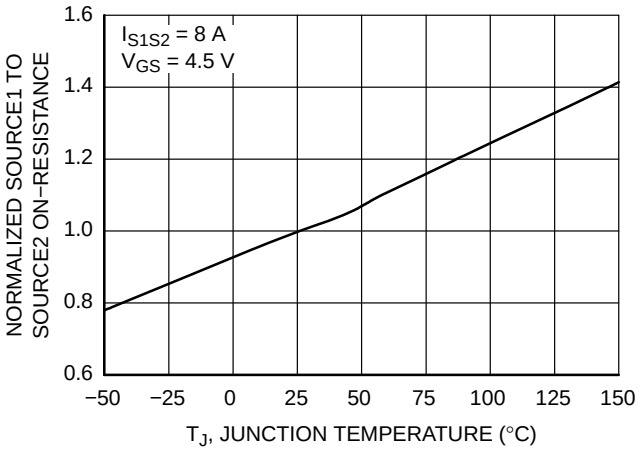


Figure 5. Normalized On Resistance vs. Junction Temperature

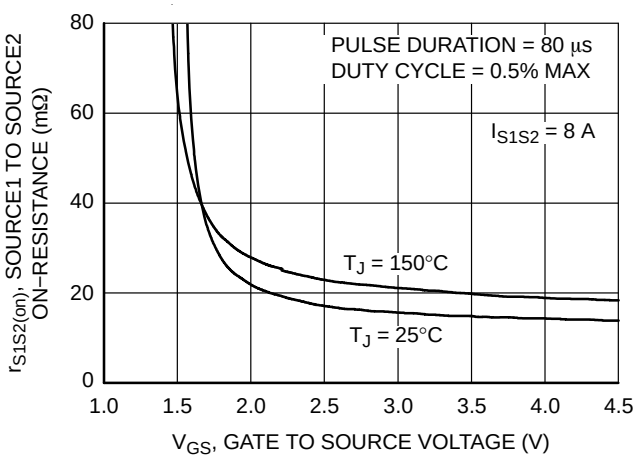


Figure 6. On Resistance vs. Gate to Source Voltage

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

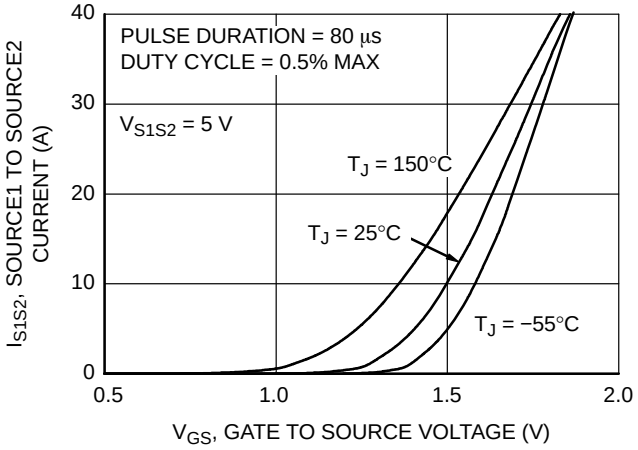


Figure 7. Transfer Characteristics

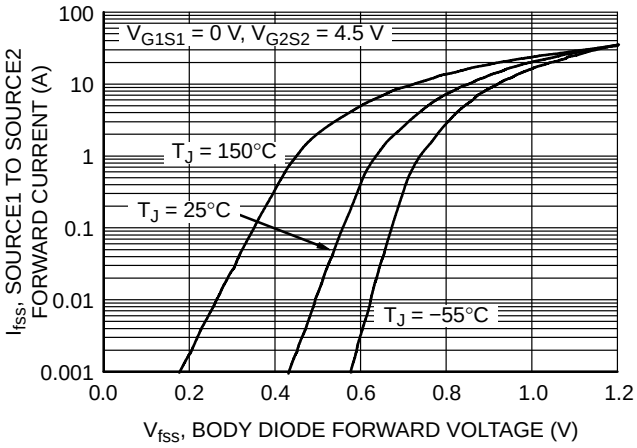


Figure 8. Source1 to Source2 Diode Forward Voltage vs. Source Current

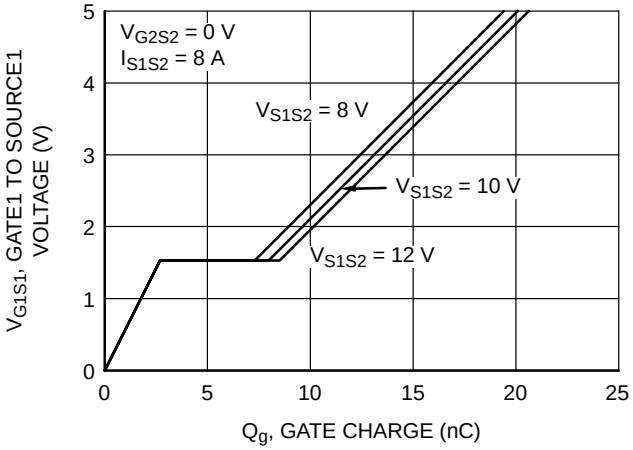


Figure 9. Gate Charge Characteristics

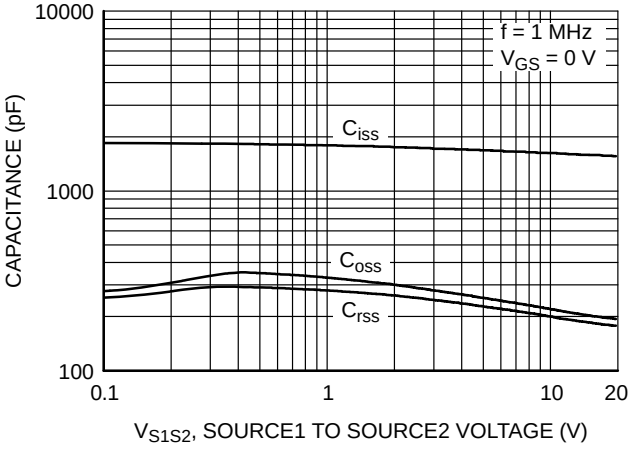


Figure 10. Capacitance vs. Source1 to Source2 Voltage

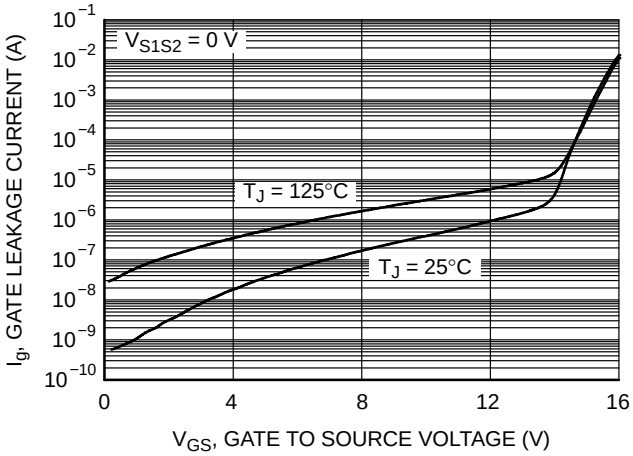


Figure 11. Gate Leakage Current vs. Gate to Source Voltage

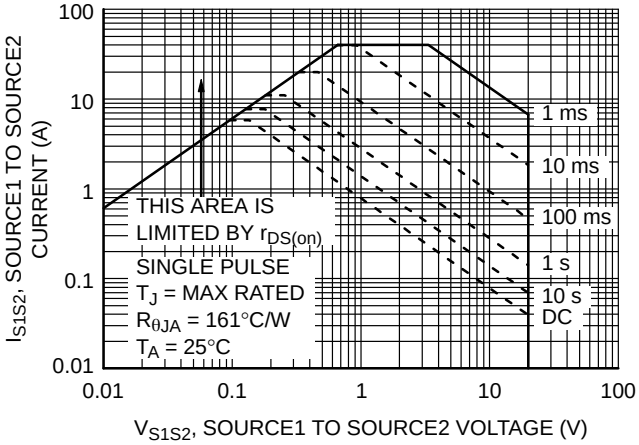


Figure 12. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

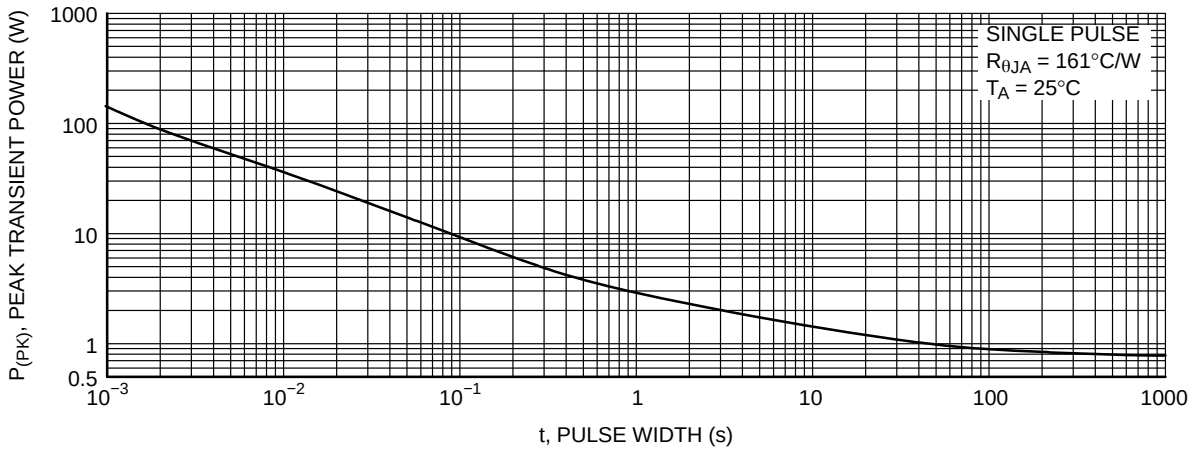


Figure 13. Single Pulse Maximum Power Dissipation

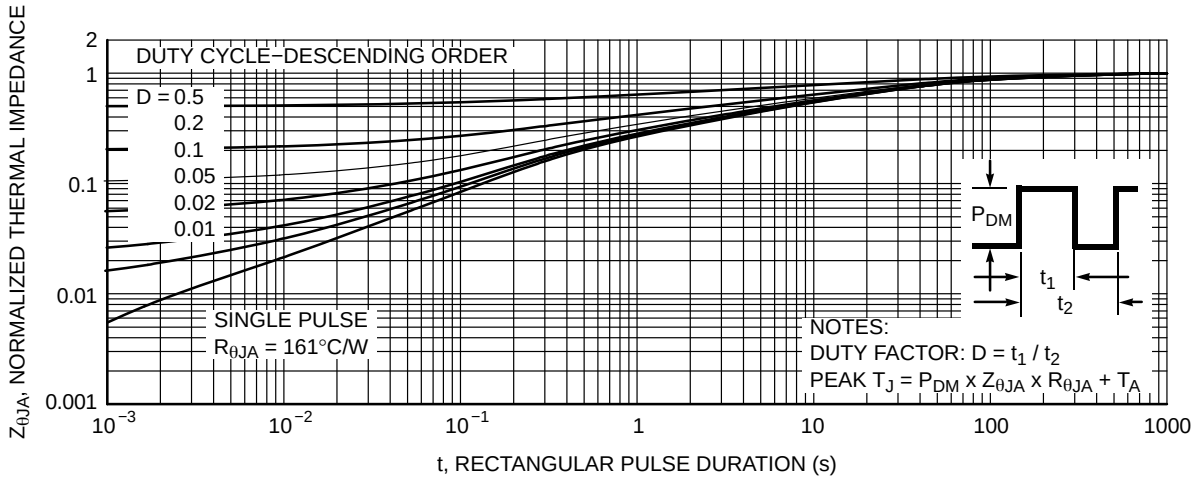


Figure 14. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMB2307NZ	307	WDFN6 2x3, 0.65P (Pb−Free, Halide Free)	7”	8 mm	3000 / Tape & Reel

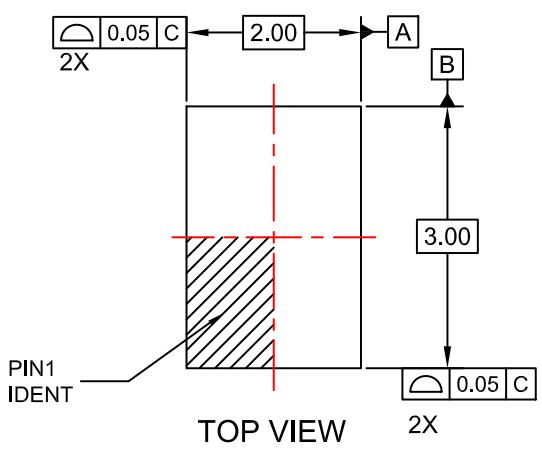
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

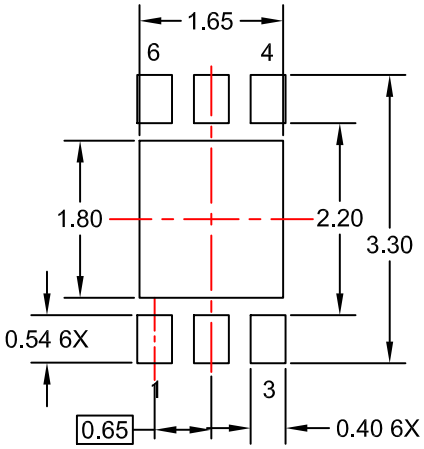
ON Semiconductor®

WDFN6 2x3, 0.65P
CASE 511CX
ISSUE O

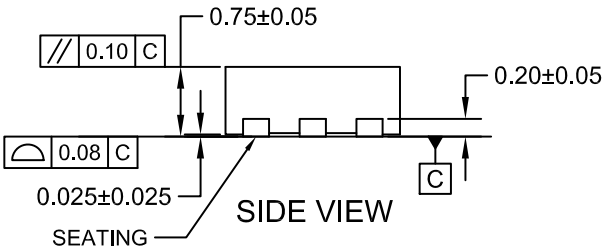
DATE 31 JUL 2016



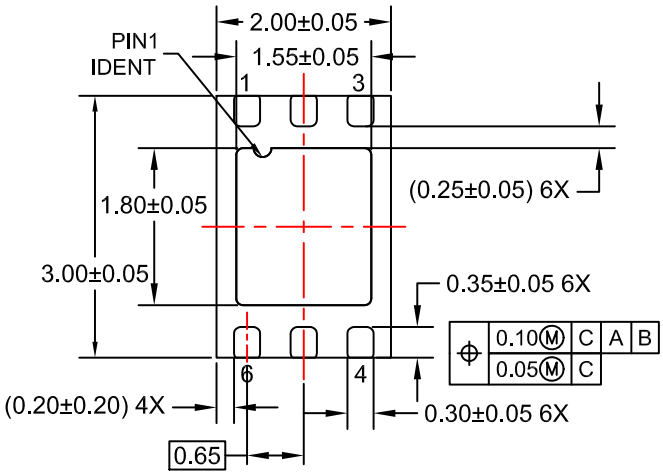
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. PACKAGE CONFORMS TO JEDEC MO-229 EXCEPT WHERE NOTED.

B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

D. DIMENSIONS ARE IN MILLIMETERS.

E. REFERENCE DIMENSIONS ARE UNCONTROLLED

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DESCRIPTION:	**WDFN6 2X3, 0.65P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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