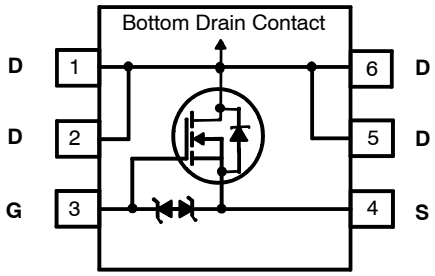
MOSFET – N-Channel, POWERTRENCH®, Ultra Thin, 1.5 V

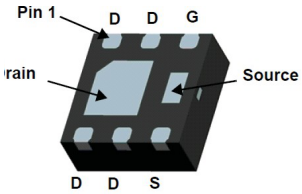
20 V, 9.5 A, 23 mΩ

FDMA410NZT

V_{DS}	$R_{DS(on)}$ MAX	$I_{D\ MAX}$
20 V	23 mΩ @ 4.5 V	9.5 A

Ultra Thin N−Channel





UDFN6 2.05x2,05 0.65P
(MicroFET)
CASE 517DT

Description

This Single N−Channel MOSFET has been designed using **onsemi**'s advanced Power Trench process to optimize the $R_{DS(on)}$ @ V_{GS} = 1.5 V on special MicroFET™ leadframe.

This design is similar to the FDMA410NZ, however it features our new advanced 0.55 mm max 2 x 2 MLP package technology.

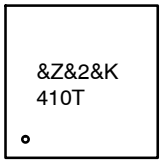
Features

- 0.55 mm max package height MicroFET 2 x 2 mm Package
- Max $R_{DS(on)}$ = 23 mΩ at V_{GS} = 4.5 V, I_D = 9.5 A
- Max $R_{DS(on)}$ = 29 mΩ at V_{GS} = 2.5 V, I_D = 8.0 A
- Max $R_{DS(on)}$ = 36 mΩ at V_{GS} = 1.8 V, I_D = 4.0 A
- Max $R_{DS(on)}$ = 60 mΩ at V_{GS} = 1.5 V, I_D = 2.0 A
- HBM ESD protection level > 1.5 kV (Note 3)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Li−Ion Battery Pack
- Baseband Switch
- Load Switch
- DC−DC Conversion
- Mobile Device Switching

MARKING DIAGRAM



&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
410T	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	–Continuous, T_A = 25°C (Note 1a)	9.5	A
	–Pulsed (Note 4)	63	
P_D	Power Dissipation, T_A = 25°C (Note 1a)	2.4	W
	Power Dissipation, T_A = 25°C (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping (Qty / Packing)†	Pin 1 Orientation
410T	FDMA410NZT	MicroFET 2x2	3000 / Tape & Reel	Top left
410T	FDMA410NZT–F130	MicroFET 2x2	3000 / Tape & Reel	Top right

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	15	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.4	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–3	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 9.5 A	–	14	23	mΩ
		V_{GS} = 2.5 V, I_D = 8.0 A	–	18	29	
		V_{GS} = 1.8 V, I_D = 4.0 A	–	25	36	
		V_{GS} = 1.5 V, I_D = 2.0 A	–	35	60	
		V_{GS} = 4.5 V, I_D = 9.5 A, T_J = 125°C	–	21	32	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 9.5 A	–	36	–	S

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

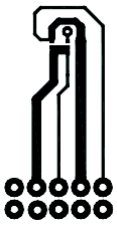
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	–	935	1310	pF
C_{oss}	Output Capacitance		–	122	170	pF
C_{rss}	Reverse Transfer Capacitance		–	84	118	pF
R_g	Gate Resistance	f = 1 MHz	0.1	1.4	3.0	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−on Delay Time	V_{DD} = 10 V, I_D = 9.5 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	–	8.5	17	ns
t_r	Rise Time		–	3.0	10	
$t_{d(off)}$	Turn−off Delay Time		–	27	44	
t_f	Fall Time		–	3.3	10	
Q_g	Total Gate Charge	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 9.5 A	–	10	14	nC
Q_{gs}	Gate to Source Charge		–	1.2	–	
Q_{gd}	Gate to Drain “Miller” Charge		–	2.0	–	
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	2.0	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 9.5 A, di/dt = 100 A/μs	–	16	30	ns
Q_{rr}	Reverse Recovery Charge		–	4.5	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JA}$ is determined by the user’s board design.

a) 52°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 145°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. Pulsed Id please refer to Figure 11 SOA curve for more details.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

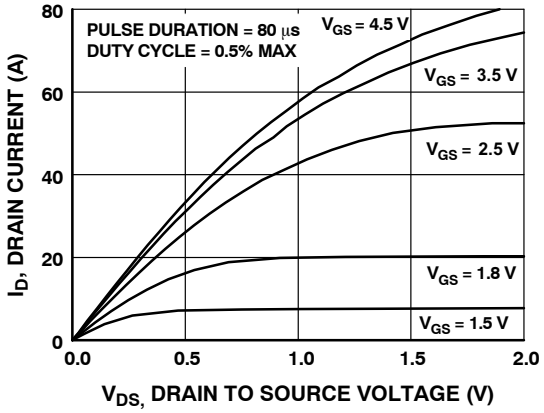


Figure 1. On Region Characteristics

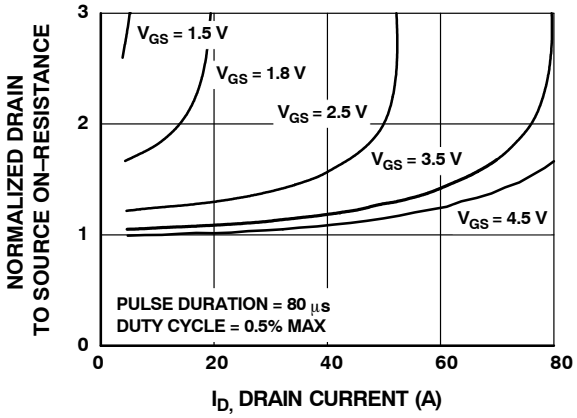


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

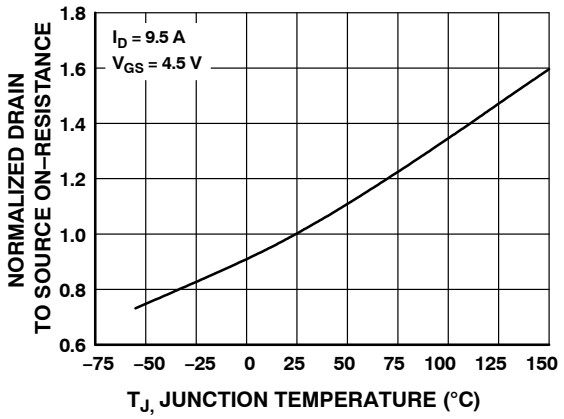


Figure 3. Normalized On Resistance vs. Junction Temperature

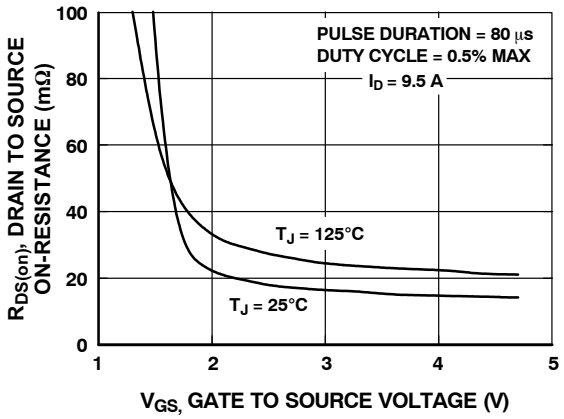


Figure 4. On-Resistance vs. Gate to Source Voltage

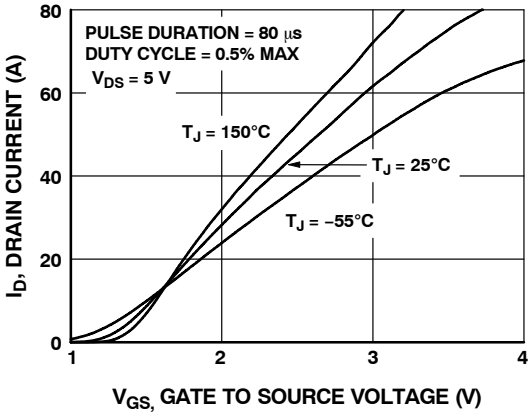


Figure 5. Transfer Characteristics

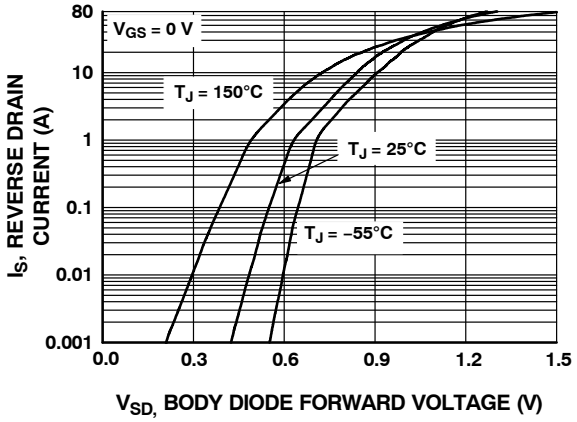


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

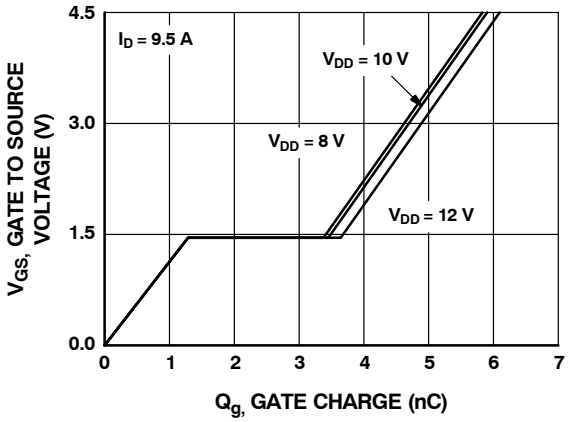


Figure 7. Gate Charge Characteristics

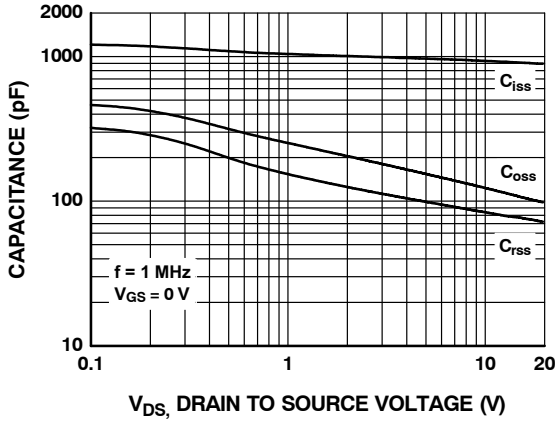


Figure 8. Capacitance vs. Drain to Source Voltage

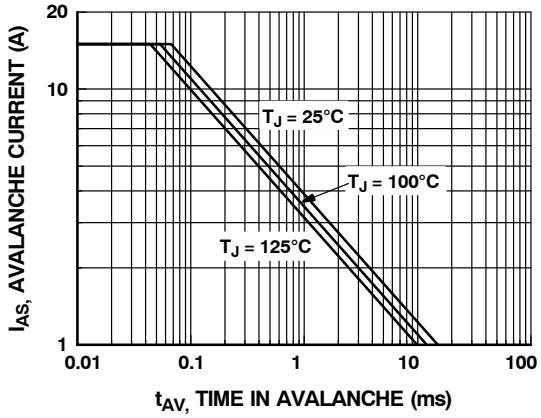


Figure 9. Unclamped Inductive Switching Capability

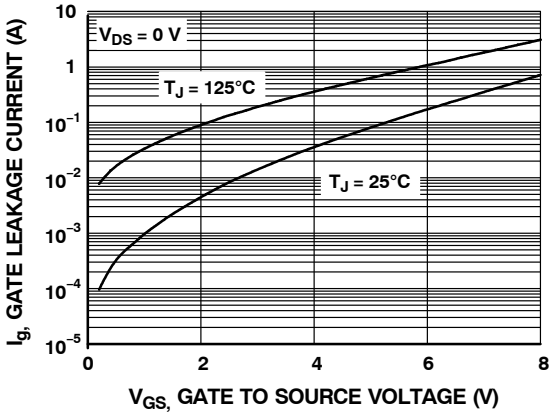


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

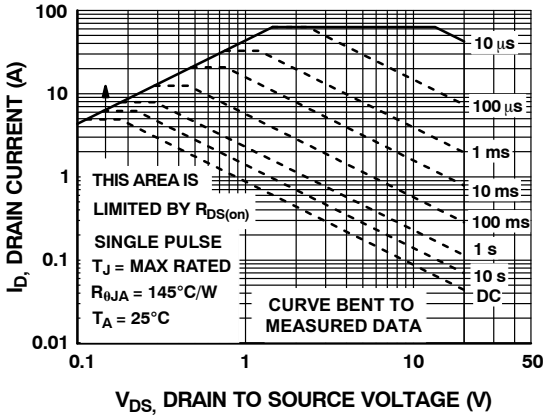


Figure 11. Forward Bias Safe Operating Area

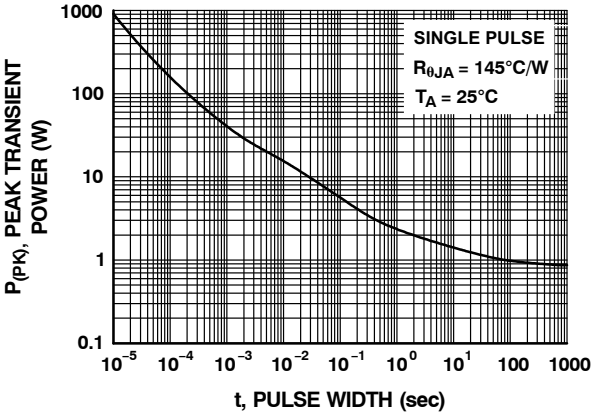


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

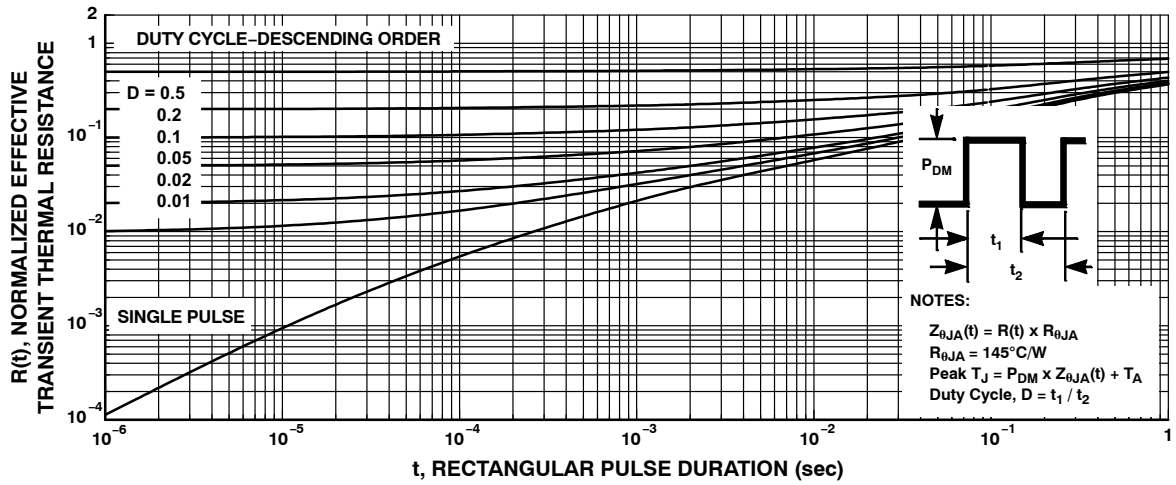


Figure 13. Junction−to−Case Transient Thermal Response Curve

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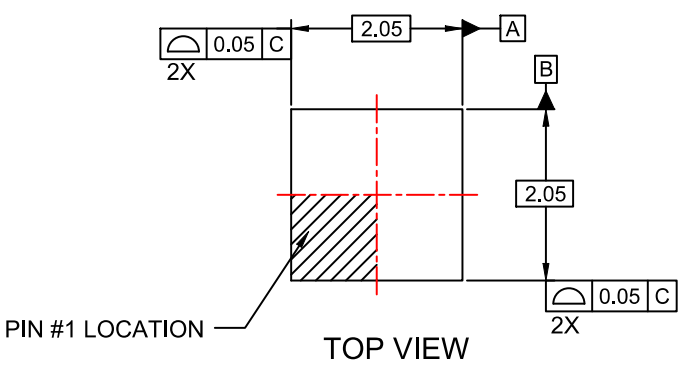
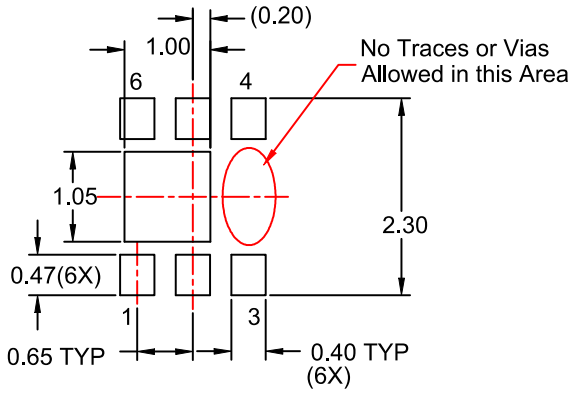
ISSUE O

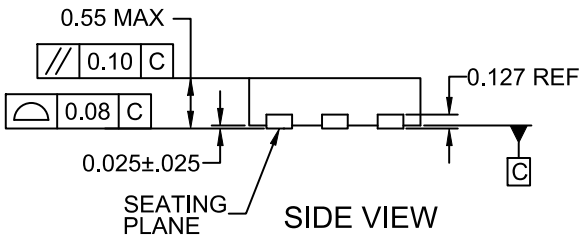
DATE 31 OCT 2016



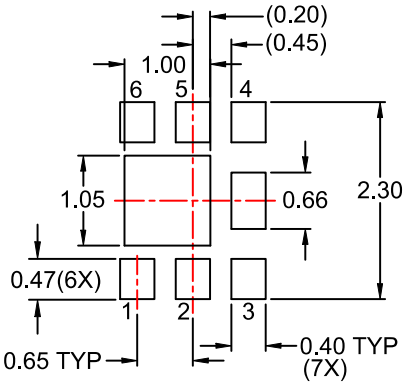
TOP VIEW



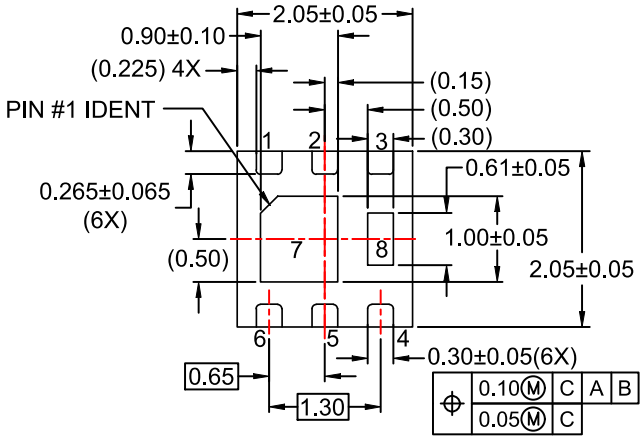
RECOMMENDED LAND PATTERN OPT 1



SIDE VIEW



RECOMMENDED LAND PATTERN OPT 2



BOTTOM VIEW

NOTES:
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