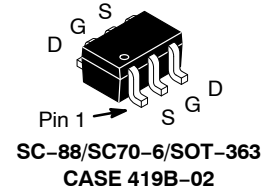


# MOSFET- N & P-Channel, POWERTRENCH®

20 V

## FDG6332C



### General Description

The N & P-Channel MOSFETs are produced using onsemi advanced POWERTRENCH process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive TSSOP-8 and SSOP-6 packages are impractical.

### Features

- Q1 0.7 A, 20 V
  - ♦  $R_{DS(ON)} = 300 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
  - ♦  $R_{DS(ON)} = 400 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- Q2 -0.6 A, -20 V
  - ♦  $R_{DS(ON)} = 420 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
  - ♦  $R_{DS(ON)} = 630 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(ON)}$
- SC70-6 Package: Small Footprint (51% Smaller than SSOT-6); Low Profile (1 mm Thick)
- These Devices are Pb-Free and are RoHS Compliant

### Applications

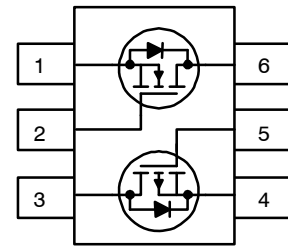
- DC-DC Converter
- Load Switch
- LCD Display Inverter

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Q1	Q2	Units	
$V_{DSS}$	Drain-Source Voltage	20	-20	V	
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	$\pm 12$	V	
$I_D$	Drain Current	Continuous (Note 1)	0.7	-0.6	A
		Pulsed	2.1	-2	
$P_D$	Power Dissipation for Single Operation (Note 1)	0.3		W	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150		$^\circ\text{C}$	

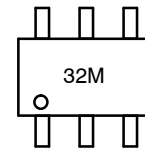
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### PIN CONNECTIONS



Complementary

### MARKING DIAGRAM



32 = Specific Device Code  
M = Assembly Operation Month

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDG6332C

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	$^{\circ}\text{C}/\text{W}$

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA} = 415^{\circ}\text{C}/\text{W}$  on minimum pad mounting on FR-4 board in still air.

## ORDERING INFORMATION

Device Marking	Device	Reel Size	Tape Width	Shipping <sup>†</sup>
32	FDG6332C	7"	8 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

$BV_{DSS}$	Drain-Source Breakdown Voltage	Q1	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20	-	-	V
		Q2	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	Q1	$I_D = 250\ \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$	-	14	-	$\text{mV}/^{\circ}\text{C}$
		Q2	$I_D = -250\ \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$	-	-14	-	
$I_{DSS}$	Zero Gate Voltage Drain Current	Q1	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		Q2	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	
$I_{GSSF} / I_{GSSR}$	Gate-Body Leakage, Forward	$V_{DS} = \pm 12\text{ V}, V_{GS} = 0\text{ V}$		-	-	$\pm 100$	nA
$I_{GSSF} / I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$		-	-	$\pm 100$	nA

### ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	Q1	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	1.1	1.5	V
		Q2	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6	-1.2	-1.5	
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	Q1	$I_D = 250\ \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$	-	-2.8	-	$\text{mV}/^{\circ}\text{C}$
		Q2	$I_D = -250\ \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$	-	3	-	
$R_{DS(on)}$	Static Drain-Source On-Resistance	Q1	$V_{GS} = 4.5\text{ V}, I_D = 0.7\text{ A}$	-	180	300	m $\Omega$
			$V_{GS} = 2.5\text{ V}, I_D = 0.6\text{ A}$	-	293	400	
			$V_{GS} = 4.5\text{ V}, I_D = 0.7\text{ A}, T_J = 125^{\circ}\text{C}$	-	247	442	
		Q2	$V_{GS} = -4.5\text{ V}, I_D = -0.6\text{ A}$	-	300	420	
			$V_{GS} = -2.5\text{ V}, I_D = -0.5\text{ A}$	-	470	630	
			$V_{GS} = -4.5\text{ V}, I_D = -0.6\text{ A}, T_J = 125^{\circ}\text{C}$	-	400	700	
$g_{FS}$	Forward Transconductance	Q1	$V_{DS} = 5\text{ V}, I_D = 0.7\text{ A}$	-	2.8	-	S
		Q2	$V_{DS} = -5\text{ V}, I_D = -0.6\text{ A}$	-	1.8	-	
$I_{D(on)}$	On-State Drain Current	Q1	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	1	-	-	A
		Q2	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-2	-	-	

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	Q1	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	113	-	pF
		Q2	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	114	-	
$C_{oss}$	Output Capacitance	Q1	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	34	-	pF
		Q2	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	24	-	

# FDG6332C

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### DYNAMIC CHARACTERISTICS

$C_{rss}$	Reverse Transfer Capacitance	Q1	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	-	16	-	pF
		Q2	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	-	9	-	

### SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn-On Delay Time	Q1	For Q1 V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 $\Omega$	-	5	10	ns
		Q2		-	5.5	11	
$t_r$	Turn-On Rise Time	Q1	For Q2 V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 A, V <sub>GS</sub> = -4.5 V, R <sub>GEN</sub> = 6 $\Omega$	-	7	15	ns
		Q2		-	14	25	
$t_{d(off)}$	Turn-Off Delay Time	Q1		-	9	18	ns
		Q2		-	6	12	
$t_f$	Turn-Off Fall Time	Q1		-	1.5	3	ns
		Q2		-	1.7	3.4	
Q <sub>g</sub>	Total Gate Charge	Q1	For Q1 V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.7 A, V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 $\Omega$	-	1.1	1.5	nC
		Q2		-	1.4	2	
Q <sub>gs</sub>	Gate-Source Charge	Q1	For Q2 V <sub>DS</sub> = -10 V, I <sub>D</sub> = -0.6 A, V <sub>GS</sub> = -4.5 V, R <sub>GEN</sub> = 6 $\Omega$	-	0.24	-	nC
		Q2		-	0.3	-	
Q <sub>gd</sub>	Gate-Drain Charge	Q1		-	0.3	-	nC
		Q2		-	0.4	-	

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	Q1		-	-	0.25	A
		Q2		-	-	-0.25	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	Q1	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.25 A (Note 2)	-	0.74	1.2	V
		Q2	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.25 A (Note 2)	-	-0.77	-1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

TYPICAL PERFORMANCE CHARACTERISTICS: N-CHANNEL

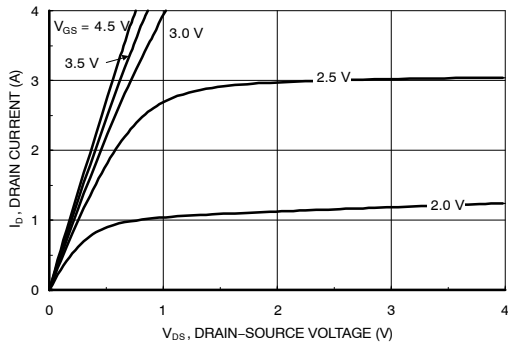


Figure 1. On-Region Characteristics

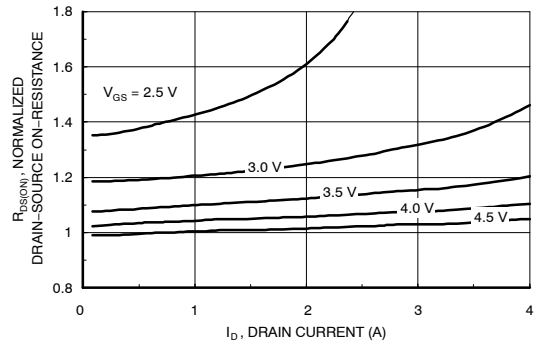


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

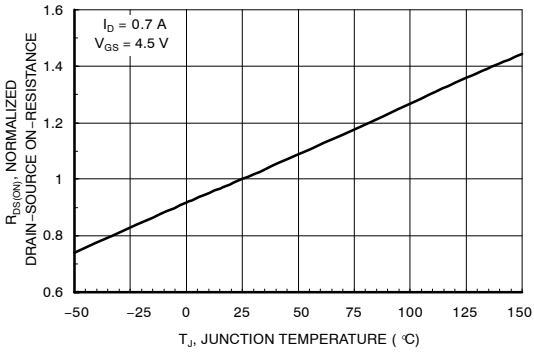


Figure 3. On-Resistance Variation with Temperature

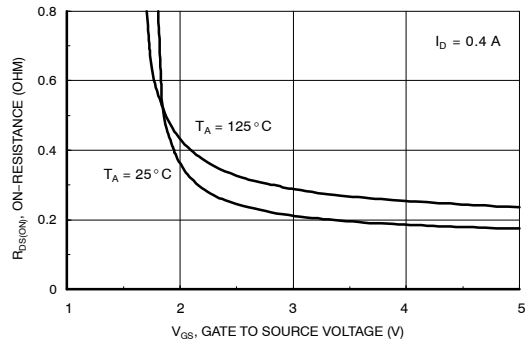


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

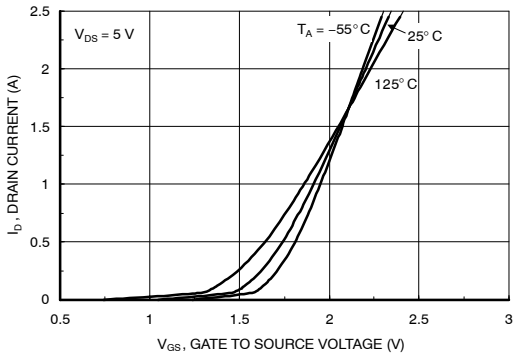


Figure 5. Transfer Characteristics

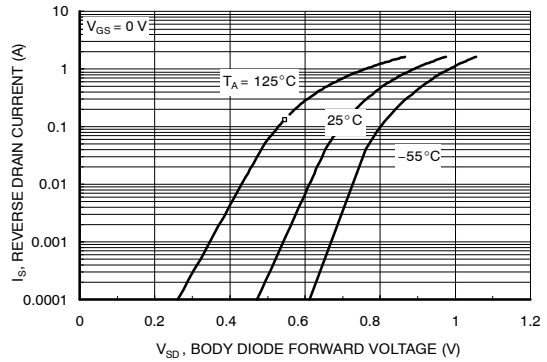


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS: N-CHANNEL (CONTINUED)

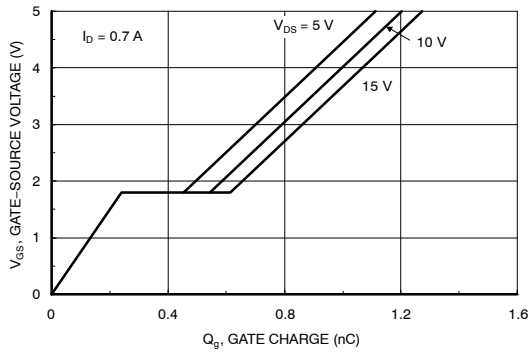


Figure 7. Gate Charge Characteristics

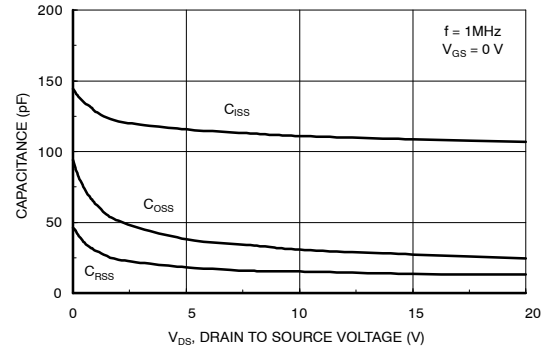


Figure 8. Capacitance Characteristics

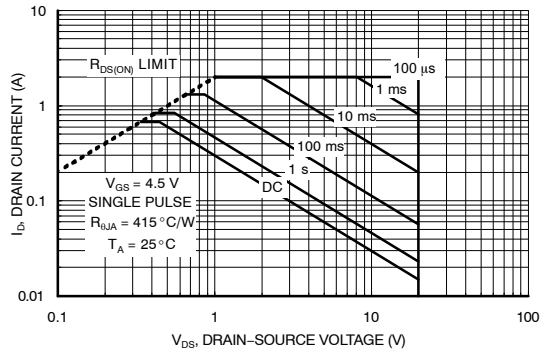


Figure 9. Maximum Safe Operating Area

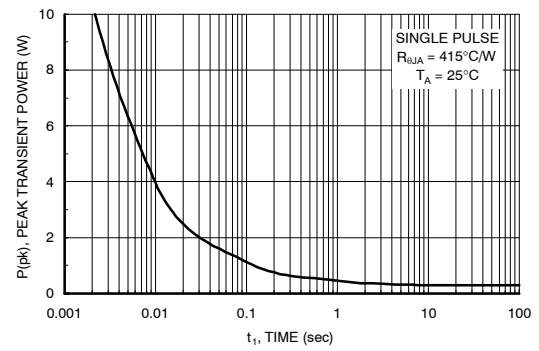


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS: P-CHANNEL

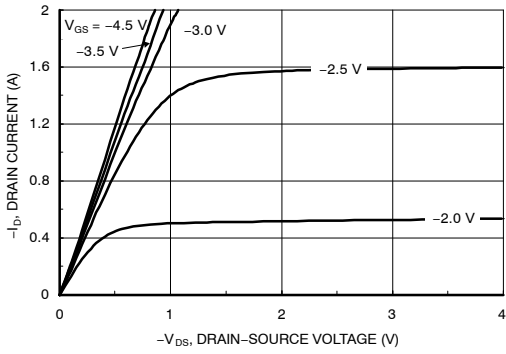


Figure 11. On-Region Characteristics

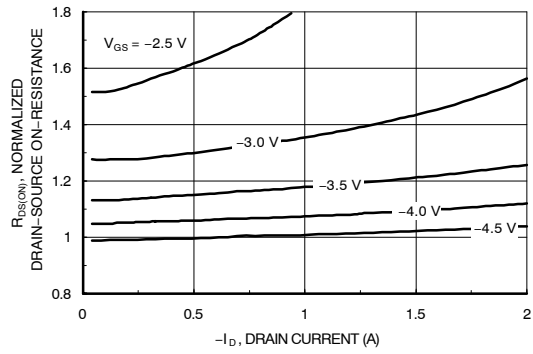


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage

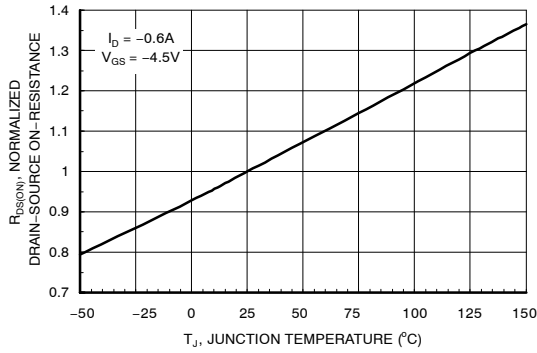


Figure 13. On-Resistance Variation with Temperature

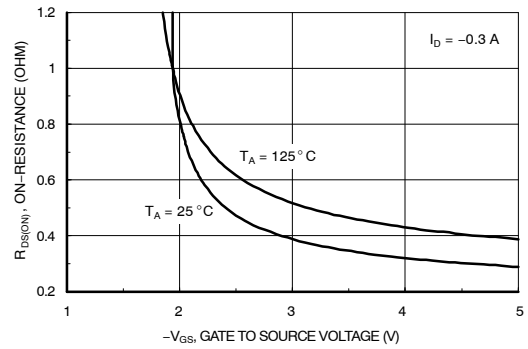


Figure 14. On-Resistance Variation with Gate-to-Source Voltage

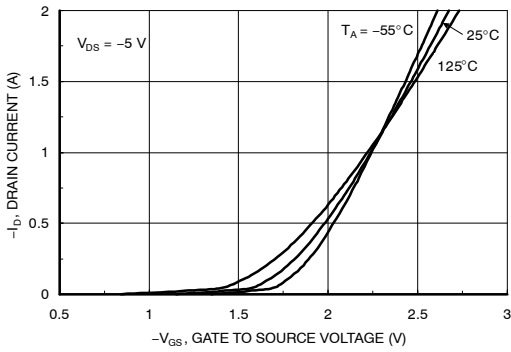


Figure 15. Transfer Characteristics

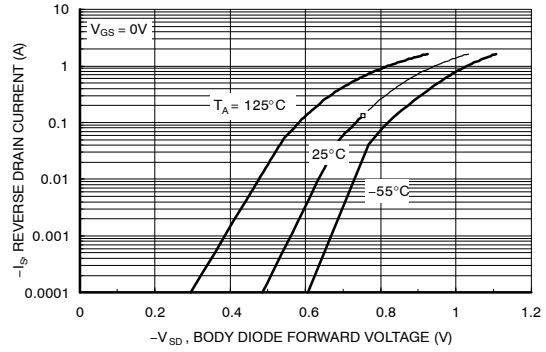


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

# FDG6332C

## TYPICAL PERFORMANCE CHARACTERISTICS: P-CHANNEL (CONTINUED)

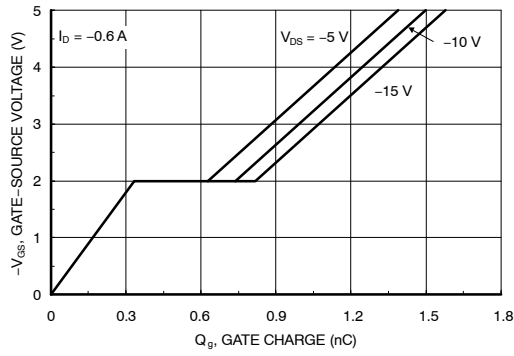


Figure 17. Gate Charge Characteristics

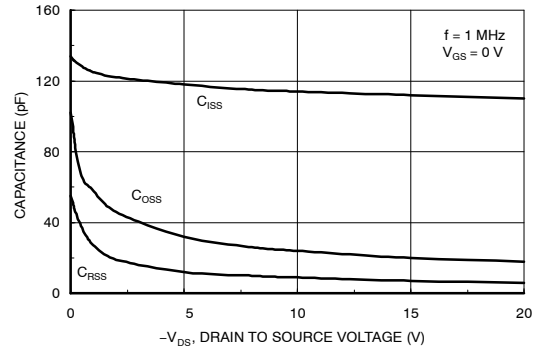


Figure 18. Capacitance Characteristics

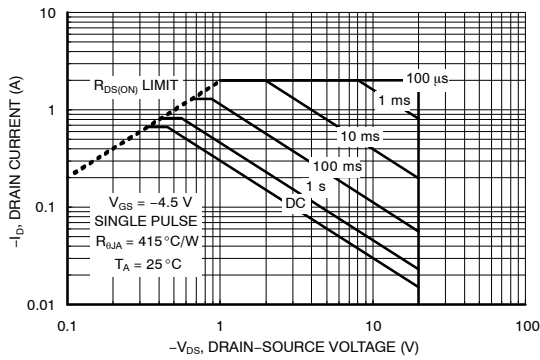


Figure 19. Maximum Safe Operating Area

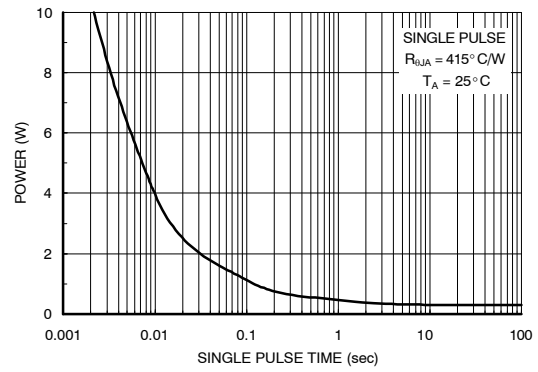
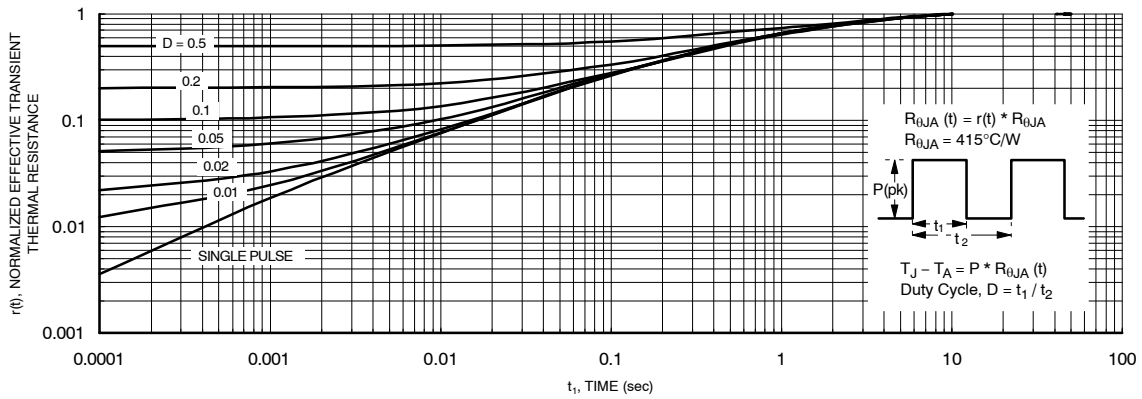


Figure 20. Single Pulse Maximum Power Dissipation



Thermal characterization performed using the conditions described in Note 1.  
Transient thermal response will change depending on the circuit board design.

Figure 21. Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

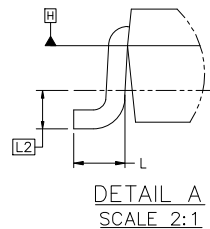
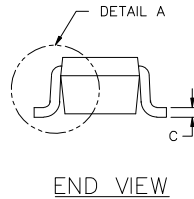
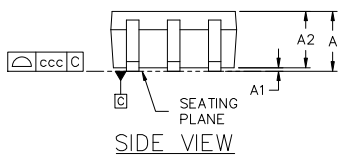
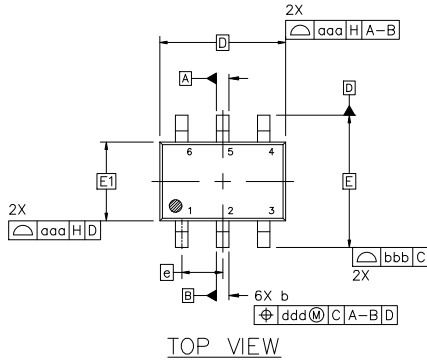


**SC-88 2.00x1.25x0.90, 0.65P**  
CASE 419B-02  
ISSUE Z

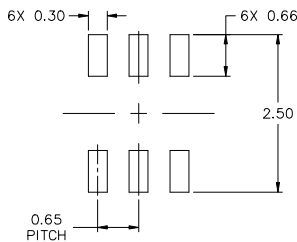
DATE 18 APR 2024

NOTES:

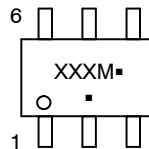
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT\*  
\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**STYLES ON PAGE 2**

<b>DOCUMENT NUMBER:</b>	<b>98ASB42985B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SC-88 2.00x1.25x0.90, 0.65P</b>	<b>PAGE 1 OF 2</b>

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



**SC-88 2.00x1.25x0.90, 0.65P**  
**CASE 419B-02**  
**ISSUE Z**

DATE 18 APR 2024

<b>STYLE 1:</b> PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	<b>STYLE 2:</b> CANCELLED	<b>STYLE 3:</b> CANCELLED	<b>STYLE 4:</b> PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	<b>STYLE 5:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 6:</b> PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
<b>STYLE 7:</b> PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	<b>STYLE 8:</b> CANCELLED	<b>STYLE 9:</b> PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	<b>STYLE 10:</b> PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	<b>STYLE 11:</b> PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	<b>STYLE 12:</b> PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
<b>STYLE 13:</b> PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 14:</b> PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	<b>STYLE 15:</b> PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	<b>STYLE 16:</b> PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	<b>STYLE 17:</b> PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	<b>STYLE 18:</b> PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
<b>STYLE 19:</b> PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	<b>STYLE 20:</b> PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	<b>STYLE 21:</b> PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	<b>STYLE 22:</b> PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	<b>STYLE 23:</b> PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	<b>STYLE 24:</b> PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
<b>STYLE 25:</b> PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	<b>STYLE 26:</b> PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	<b>STYLE 27:</b> PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	<b>STYLE 28:</b> PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	<b>STYLE 29:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	<b>STYLE 30:</b> PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

<b>DOCUMENT NUMBER:</b>	<b>98ASB42985B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SC-88 2.00x1.25x0.90, 0.65P</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)