

MOSFET– N-Channel, Logic Level, **POWERTRENCH**[®]

FDG315N

General Description

This N-Channel Logic Level MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 2 A, 30 V
 - ◆ $R_{DS(ON)} = 0.12 \Omega @ V_{GS} = 10 V$
 - ◆ $R_{DS(ON)} = 0.16 \Omega @ V_{GS} = 4.5 V$
- Low Gate Charge (2.1 nC Typical)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- Compact Industry Standard SC70-6 Surface Mount Package
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC/DC Converter
- Load Switch
- Power Management

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current	Continuous (Note 1a)	2
		Pulsed	6
P_D	Power Dissipation for Single Operation	(Note 1a)	0.75
		(Note 1b)	0.48
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

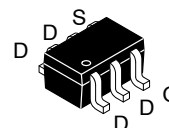
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	260	$^\circ C/W$

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
 - 170 $^\circ C/W$ when mounted on a 1 in² pad of 2 oz copper.
 - 260 $^\circ C/W$ when mounted on a minimum pad.



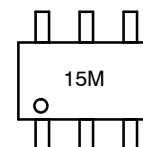
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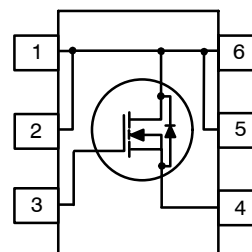
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CASE 419B-02

MARKING DIAGRAM



15 = Specific Device Code
M = Assembly Operation Month

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDG315N

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Reel Size	Tape Width	Shipping [†]
15	FDG315N	7"	8 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	26	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate–Body Leakage Forward	V _{GS} = 16 V, V _{DS} = 0 V	–	–	100	nA
I _{GSS}	Gate–Body Leakage Reverse	V _{GS} = –16 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.8	3	V
ΔV _{GS(th)} / ΔT _J	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	–4	–	mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 2 A V _{GS} = 10 V, I _D = 2 A, T _J = 125°C V _{GS} = 4.5 V, I _D = 1.7 A	–	0.100 0.140 0.130	0.12 0.20 0.16	Ω
I _{D(on)}	On–State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V	3	–	–	A
G _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 2 A	–	5	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	–	220	–	pF
C _{oss}	Output Capacitance		–	50	–	pF
C _{rss}	Reverse Transfer Capacitance		–	20	–	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	3	6	ns
t _r	Turn-On Rise Time		–	11	22	ns
t _{d(off)}	Turn-Off Delay Time		–	7	14	ns
t _f	Turn-Off Fall Time		–	3	6	ns
Q _g	Total Gate Charge	V _{DS} = 15 V, I _D = 2 A, V _{GS} = 5 V	–	2.1	4	nC
Q _{gs}	Gate–Source Charge		–	0.8	–	nC
Q _{gd}	Gate–Drain Charge		–	0.7	–	nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current	–	–	0.42	A	
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.42 A (Note 2)	–	0.7	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL PERFORMANCE CHARACTERISTICS

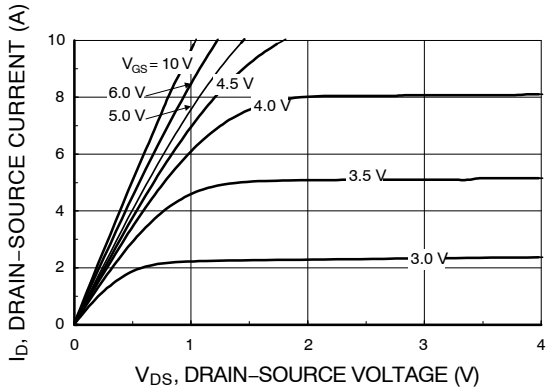


Figure 1. On-Region Characteristics

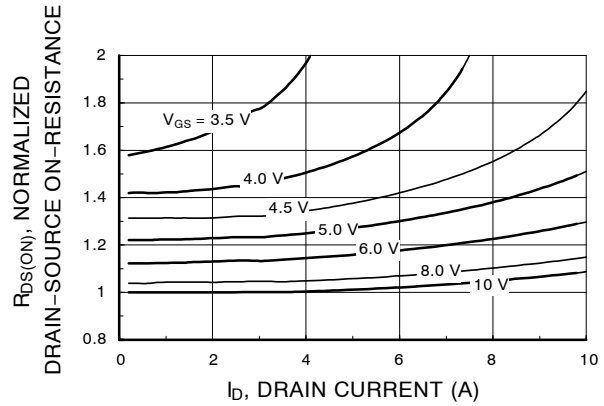


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

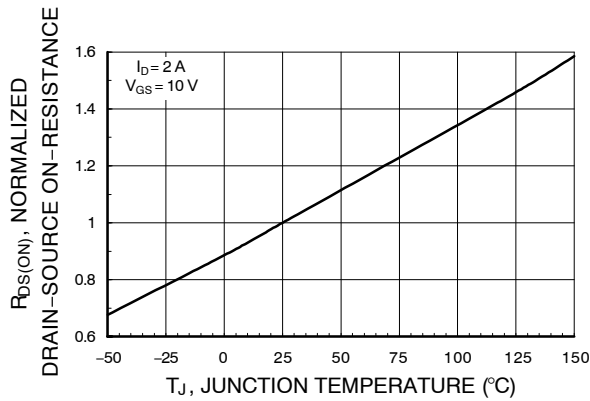


Figure 3. On-Resistance Variation with Temperature

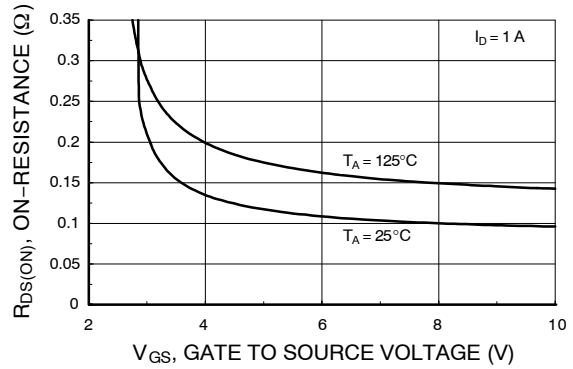


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

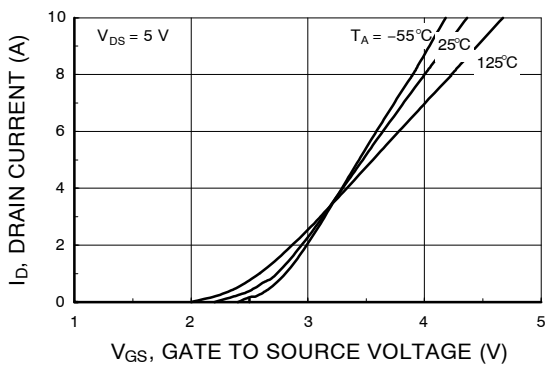


Figure 5. Transfer Characteristics

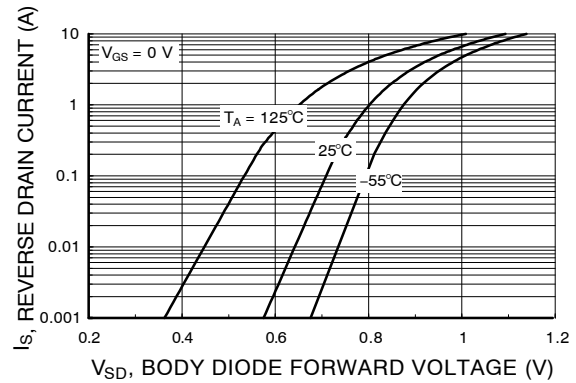


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

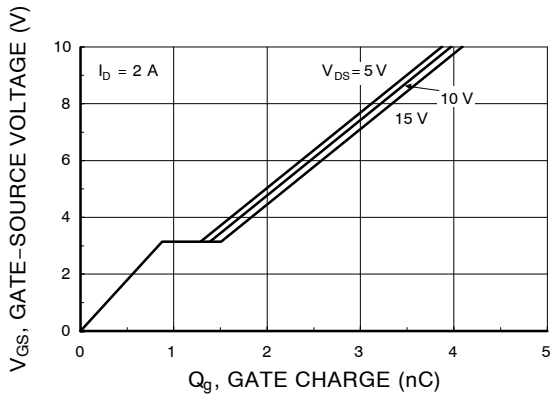


Figure 7. Gate Charge Characteristics

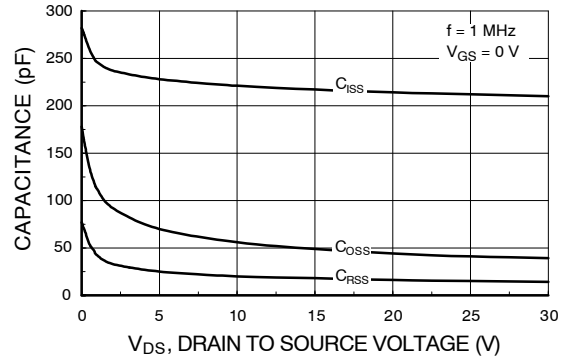


Figure 8. Capacitance Characteristics

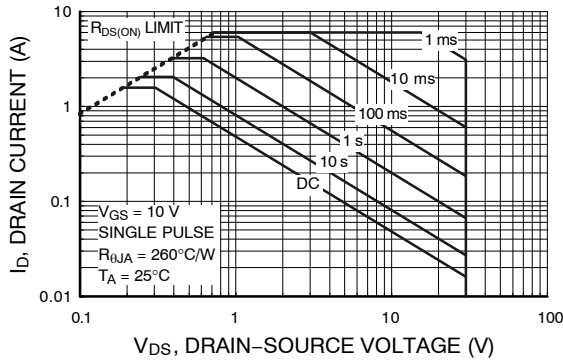


Figure 9. Maximum Safe Operating Area

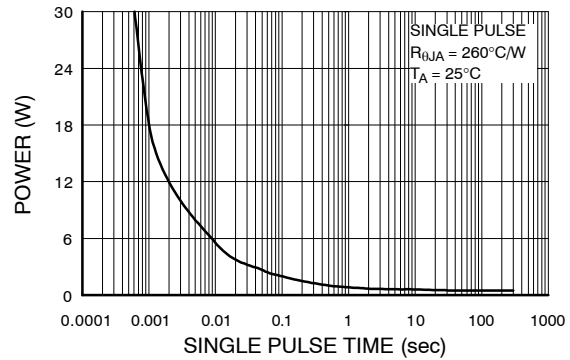
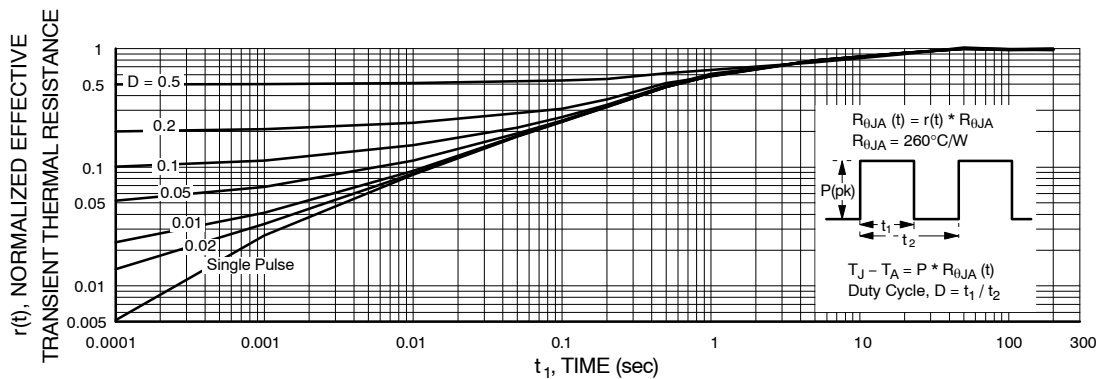


Figure 10. Single Pulse Maximum Power Dissipation



Thermal characterization performed using the conditions described in Note 1b.
 Transient thermal response will change depending on the circuit board design.

Figure 11. Transient Thermal Response Curve



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 SCALE 2:1

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 CASE 419B-02
 ISSUE Y

DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

GENERIC MARKING DIAGRAM*



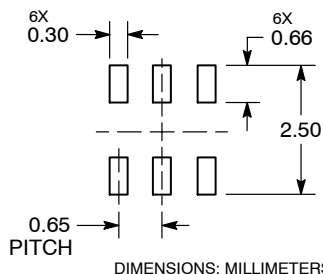
XXX = Specific Device Code
 M = Date Code*
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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