

# Dual, N & P-Channel, Digital FET

## FDC6321C

### General Description

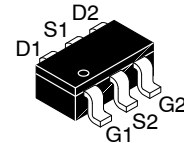
These dual N & P Channel logic level enhancement mode field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors in load switching applications. Since bias resistors are not required this dual digital FET can replace several digital transistors with different bias resistors.

### Features

- N-Channel 0.68 A, 25 V  
 $R_{DS(ON)} = 0.45 \Omega @ V_{GS} = 4.5 V$
- P-Channel -0.46 A, -25 V  
 $R_{DS(ON)} = 1.1 \Omega @ V_{GS} = -4.5 V$
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits.  $V_{GS(th)} < 1.0 V$ .
- Gate-Source Zener for ESD Ruggedness. >6 kV Human Body Model
- Replace Multiple Dual NPN & PNP Digital Transistors
- This is a Pb-Free Device

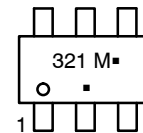
N-Channel		
$V_{DSS}$	$R_{DS(ON)} MAX$	$I_D MAX$
25 V	0.45 $\Omega @ 4.5 V$	0.68 A

P-Channel		
$V_{DSS}$	$R_{DS(ON)} MAX$	$I_D MAX$
-25 V	1.1 $\Omega @ -4.5 V$	-0.46 A



TSOT23 6-Lead  
SUPERSOT™ -6  
CASE 419BL

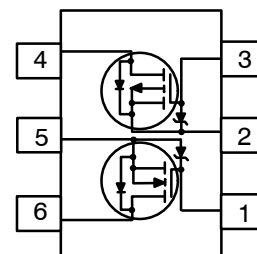
### MARKING DIAGRAM



- 321 = Specific Device Code
- M = Assembly Operation Month
- = Pb-Free Package

(Note: Microdot may be in either location)

### PINOUT



### ORDERING INFORMATION

Device	Package	Shipping†
FDC6321C	TSOT-23-6 (Pb-free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# FDC6321C

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Unit
V <sub>DSS</sub> , V <sub>CC</sub>	Drain-Source Voltage, Power Supply Voltage	25	-25	V
V <sub>GSS</sub> , V <sub>IN</sub>	Gate-Source Voltage	8	-8	V
I <sub>D</sub> , I <sub>O</sub>	Drain/Output Current	- Continuous	-0.46	A
		- Pulsed	-1.5	A
P <sub>D</sub>	Power Dissipation	(Note 1a)	0.9	W
		(Note 1b)	0.7	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100 pF / 1500 Ω)	6		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	140	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	60	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	N-Ch P-Ch	25 -25	- -	- -	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C I <sub>D</sub> = -250 μA, Referenced to 25°C	N-Ch P-Ch	- -	26 -22	- -	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	N-Ch	- -	- -	1 10	μA
		V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	P-Ch	- -	- -	-1 -10	nA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0 V	N-Ch P-Ch	- -	- -	100 -100	nA

### ON CHARACTERISTICS (Note 2)

$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C I <sub>D</sub> = -250 μA, Referenced to 25°C	N-Ch P-Ch	- -	-2.6 2.1	- -	mV/°C
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	N-Ch P-Ch	0.65 -0.65	0.8 -0.86	1.5 -1.5	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.5 A	N-Ch	-	0.33	0.45	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 125°C	N-Ch	-	0.51	0.72	
		V <sub>GS</sub> = 2.7 V, I <sub>D</sub> = 0.25 A	N-Ch	-	0.44	0.6	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.5 A	P-Ch	-	0.87	1.1	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.5 A, T <sub>J</sub> = 125°C	P-Ch	-	1.21	1.8	
		V <sub>GS</sub> = -2.7 V, I <sub>D</sub> = -0.25 A	P-Ch	-	1.22	1.5	
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5 V V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -5 V	N-Ch P-Ch	1 -1	- -	- -	A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 0.5 A V <sub>DS</sub> = -5 V, I <sub>D</sub> = -0.5 A	N-Ch P-Ch	- -	1.45 0.8	- -	S

# FDC6321C

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTICS</b>							
C <sub>iss</sub>	Input Capacitance	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	N-Ch	-	50	-	pF
			P-Ch	-	63	-	
C <sub>oss</sub>	Output Capacitance	P-Channel V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	N-Ch	-	28	-	pF
			P-Ch	-	34	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		N-Ch	-	9	-	pF
			P-Ch	-	10	-	

## SWITCHING CHARACTERISTICS (Note 2)

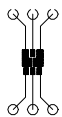
t <sub>d(on)</sub>	Turn-On Delay Time	N-Channel V <sub>DD</sub> = 6 V, I <sub>D</sub> = 0.5 A, V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 50 Ω	N-Ch	-	3	6	ns
			P-Ch	-	7	20	
t <sub>r</sub>	Turn-On Rise Time		N-Ch	-	8	16	ns
			P-Ch	-	9	18	
t <sub>d(off)</sub>	Turn-Off Delay Time	P-Channel V <sub>DD</sub> = -6 V, I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = -4.5 V, R <sub>GEN</sub> = 50 Ω	N-Ch	-	17	30	ns
			P-Ch	-	55	110	
t <sub>f</sub>	Turn-Off Fall Time		N-Ch	-	13	25	ns
			P-Ch	-	35	70	
Q <sub>g</sub>	Total Gate Charge	N-Channel V <sub>DS</sub> = 5 V, I <sub>D</sub> = 0.5 A, V <sub>GS</sub> = 4.5 V	N-Ch	-	1.64	2.3	nC
			P-Ch	-	1.1	1.5	
Q <sub>gs</sub>	Gate-Source Charge	P-Channel V <sub>DS</sub> = -5 V, I <sub>D</sub> = -0.25 A, V <sub>GS</sub> = -4.5 V	N-Ch	-	0.38	-	nC
			P-Ch	-	0.32	-	
Q <sub>gd</sub>	Gate-Drain Charge		N-Ch	-	0.45	-	nC
			P-Ch	-	0.25	-	

## DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		N-Ch	-	-	0.3	A
			P-Ch	-	-	-0.5	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage (Note 2)	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.5 A	N-Ch	-	0.83	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.5 A, T <sub>J</sub> = 125°C	N-Ch	-	0.69	0.85	
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.5 A	P-Ch	-	-0.89	-1.2	
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.5 A, T <sub>J</sub> = 125°C	P-Ch	-	-0.75	-0.85	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 140°C/W on a 0.125 in<sup>2</sup> pad of 2 oz. copper.



b. 180°C/W on a 0.005 in<sup>2</sup> pad of 2 oz. copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS: N-CHANNEL

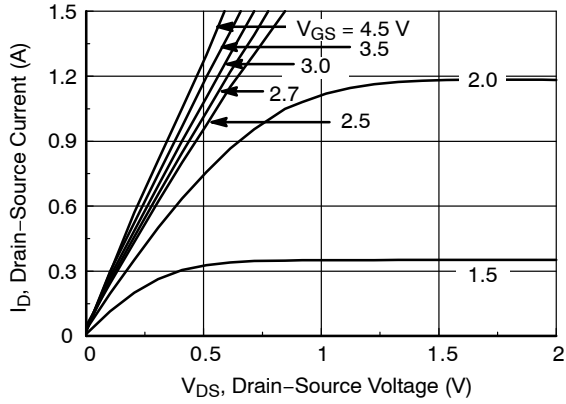


Figure 1. On-Region Characteristics

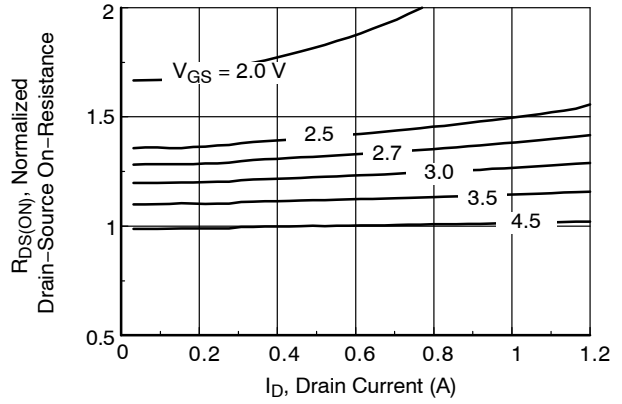


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

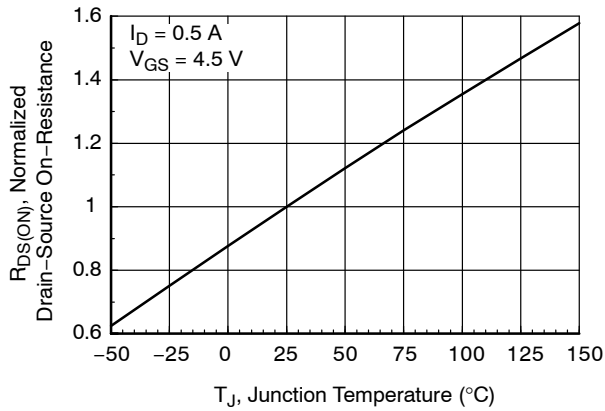


Figure 3. On-Resistance Variation with Temperature

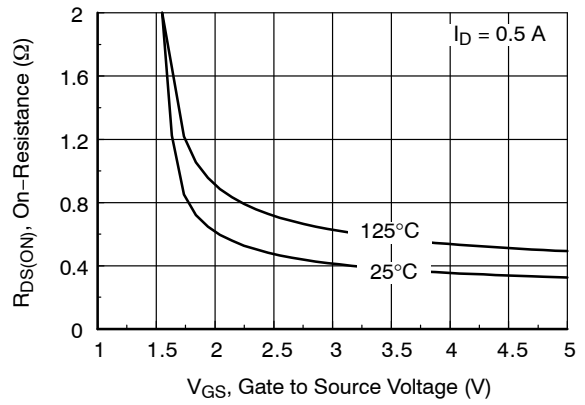


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

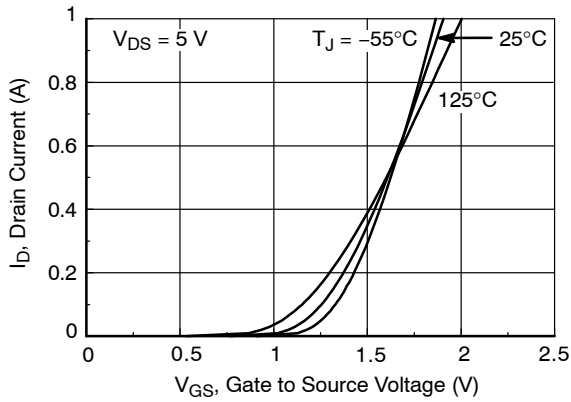


Figure 5. Transfer Characteristics

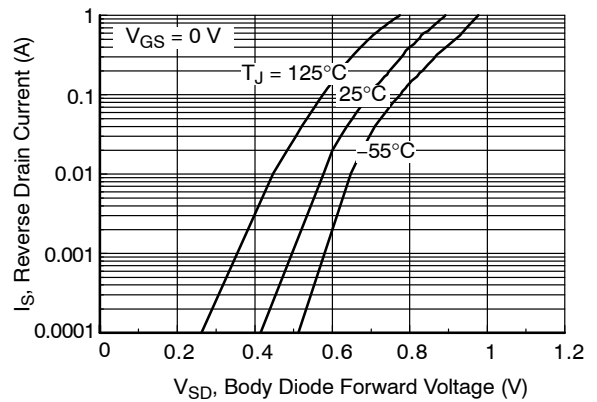


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: N-CHANNEL (continued)

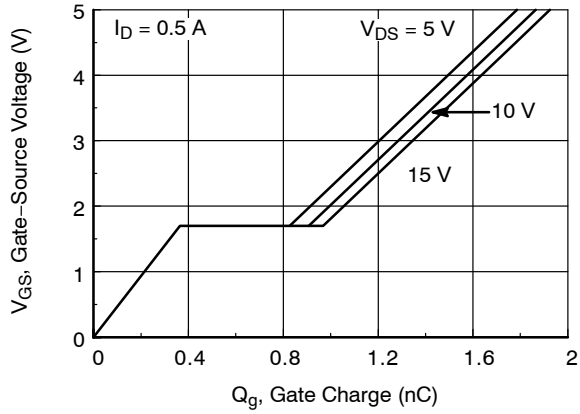


Figure 7. Gate Charge Characteristics

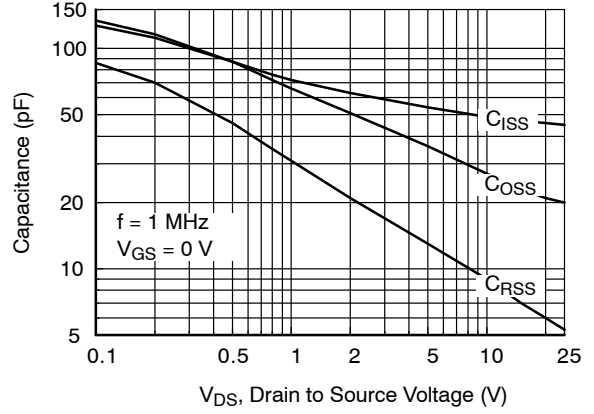


Figure 8. Capacitance Characteristics

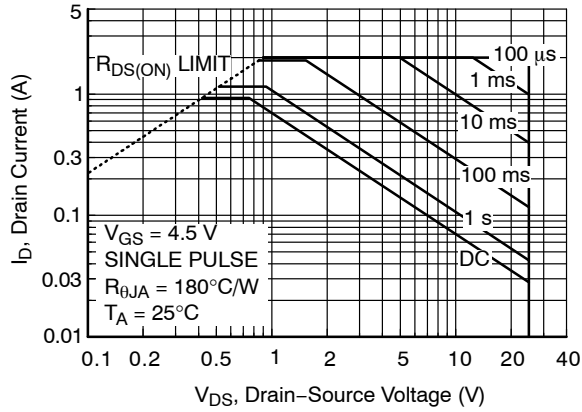


Figure 9. Maximum Safe Operating Area

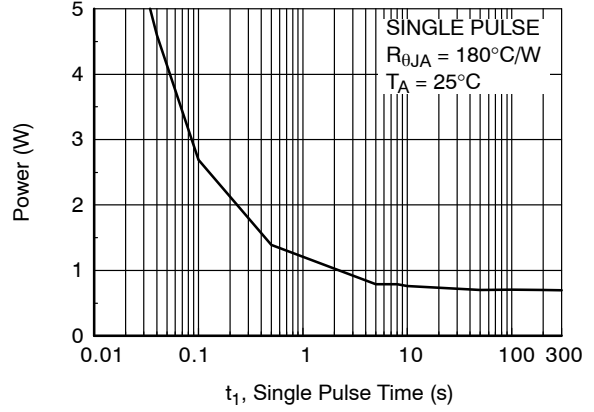


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS: P-CHANNEL

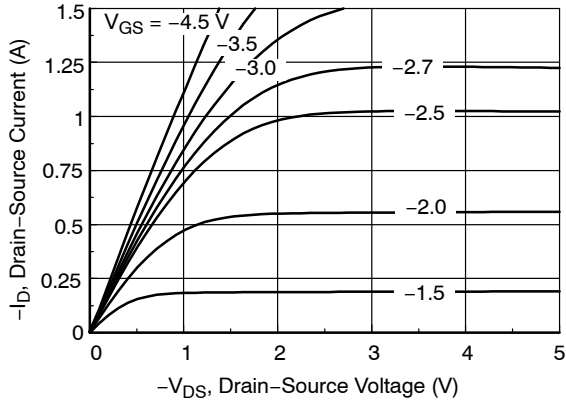


Figure 11. On-Region Characteristics

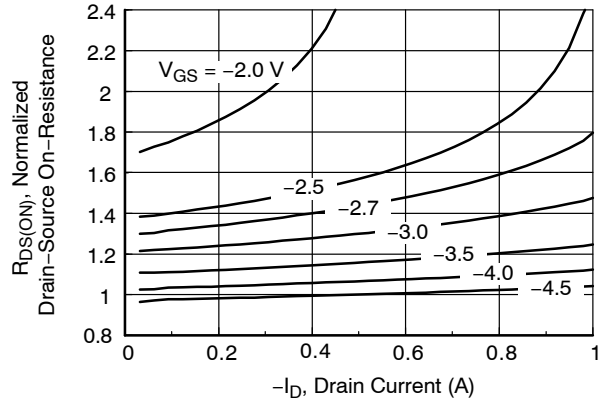


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage

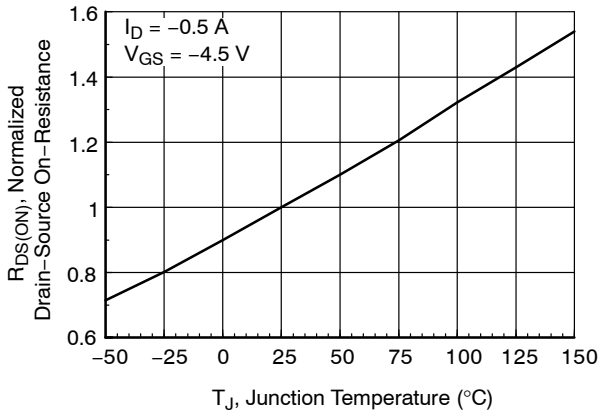


Figure 13. On-Resistance Variation with Temperature

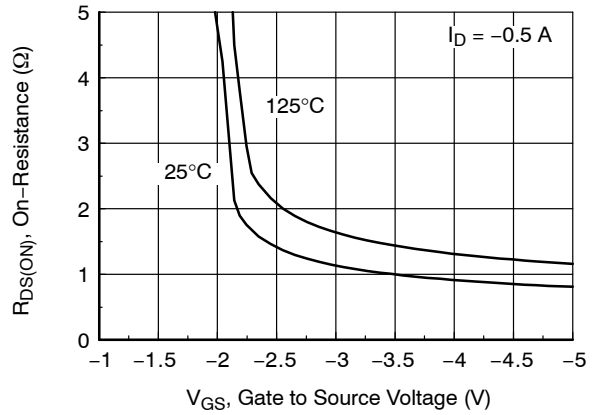


Figure 14. On-Resistance Variation with Gate-to-Source Voltage

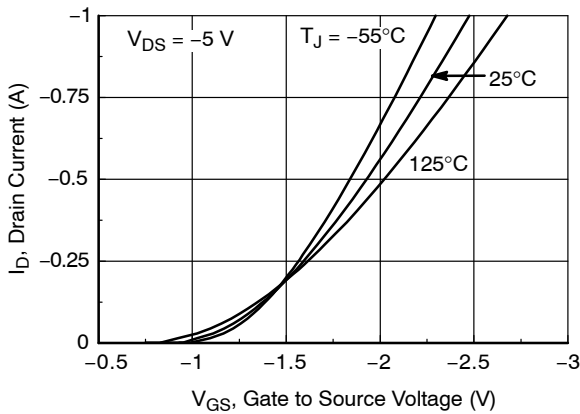


Figure 15. Transfer Characteristics

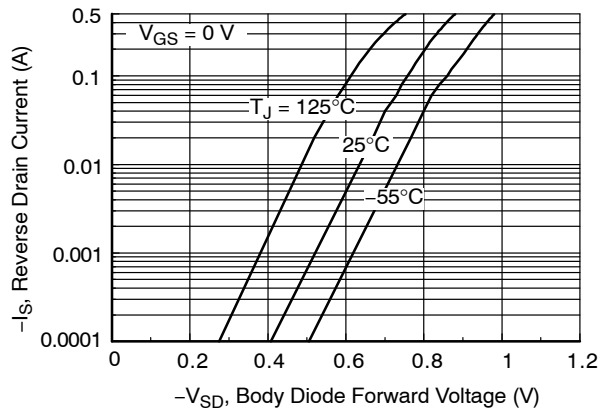


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: P-CHANNEL (continued)

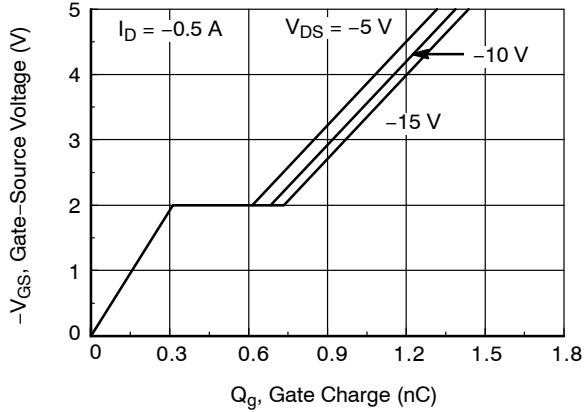


Figure 17. Gate Charge Characteristics

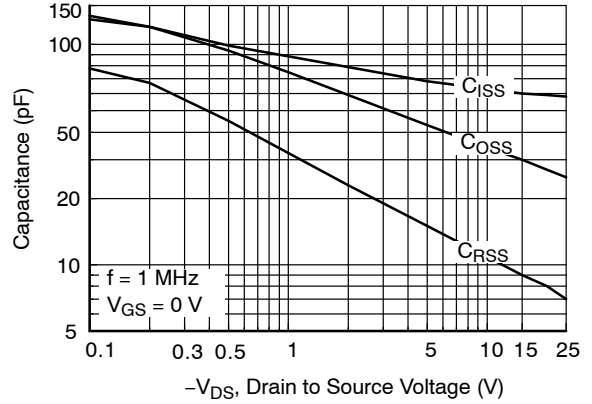


Figure 18. Capacitance Characteristics

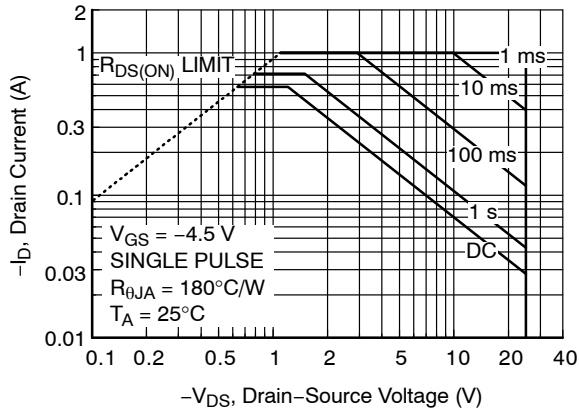


Figure 19. Maximum Safe Operating Area

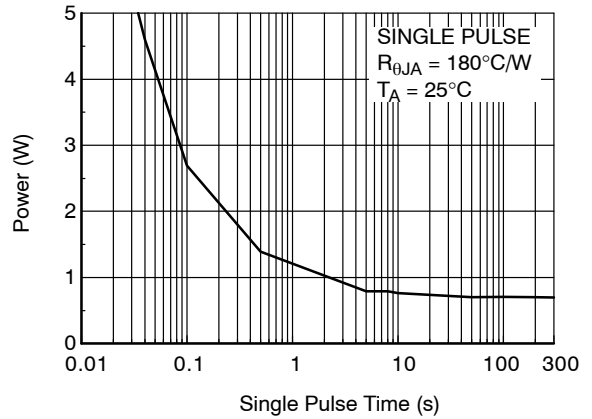


Figure 20. Single Pulse Maximum Power Dissipation

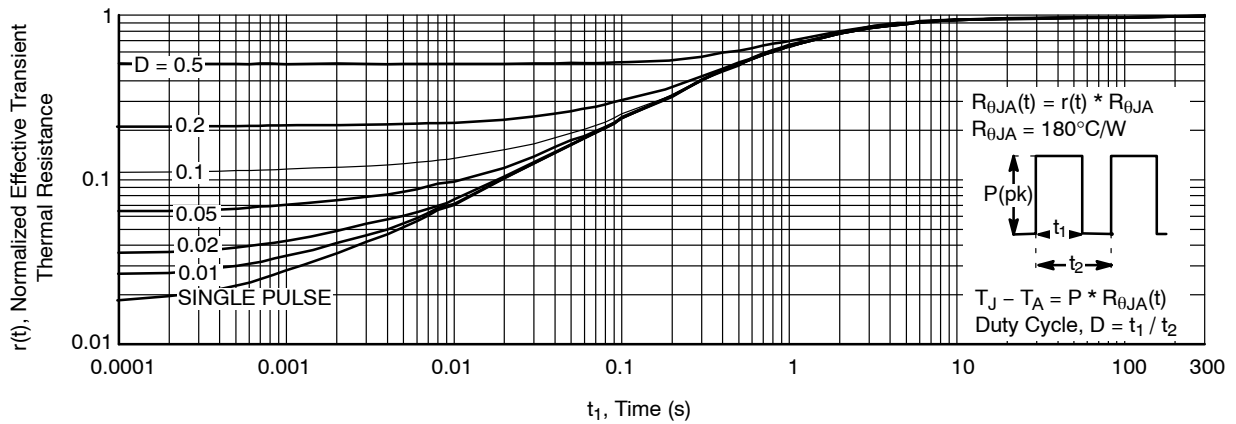


Figure 21. Transient Thermal Response Curve

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

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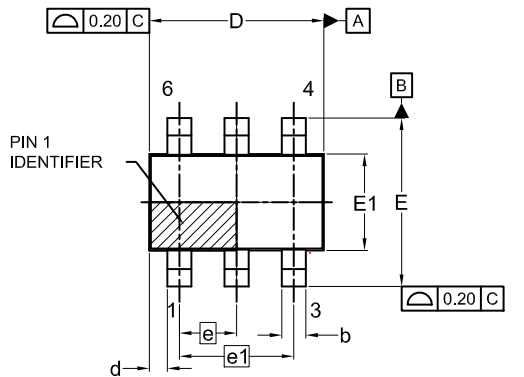




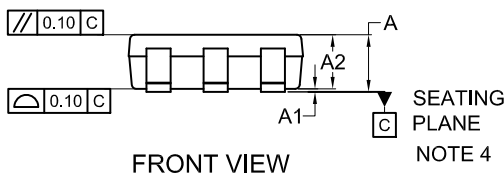
1  
SCALE 2:1

TSOT23 6-Lead  
CASE 419BL  
ISSUE A

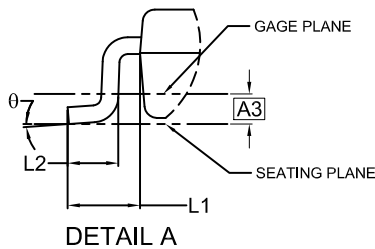
DATE 31 AUG 2020



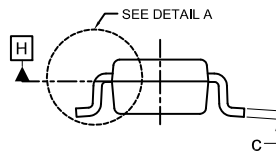
TOP VIEW



FRONT VIEW

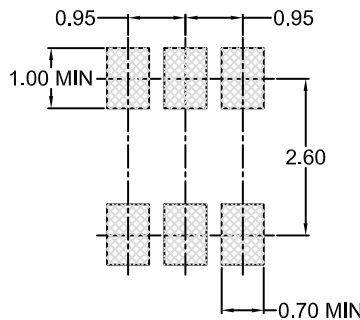


DETAIL A



SIDE VIEW

SYMM  
⌀



LAND PATTERN  
RECOMMENDATION

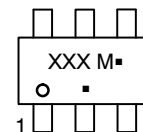
\*FOR ADDITIONAL INFORMATION ON OUR  
Pb-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⌀	0°	--	10°

GENERIC  
MARKING DIAGRAM\*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

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