

MOSFET – Dual, N-Channel, POWERTRENCH®

100 V Specified

FDC3601N

General Description

These N-Channel 100 V specified MOSFETs are produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

Features

- 1.0 A, 100 V
 $R_{DS(ON)} = 500 \Omega @ V_{GS} = 10 V$
 $R_{DS(ON)} = 550 \Omega @ V_{GS} = 6.0 V$
- Low Gate Charge (3.7 nC Typical)
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SUPERSOT™ -6 Package: Small Footprint 72% (Smaller than Standard SO-8); Low Profile (1 mm Thick)
- This is a Pb-Free Device

Applications

- Load Switch
- Battery Protection
- Power Management

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

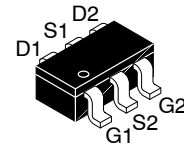
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current	- Continuous (Note 1a)	1.0 A
		- Pulsed	4.0 A
P_D	Power Dissipation for Single Operation	(Note 1a)	0.96 W
		(Note 1b)	0.9 W
		(Note 1c)	0.7 W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

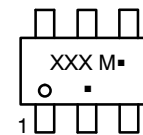
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ C/W$

V_{DSS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	500 m Ω @ 10 V	1.0 A
	550 m Ω @ 6.0 V	



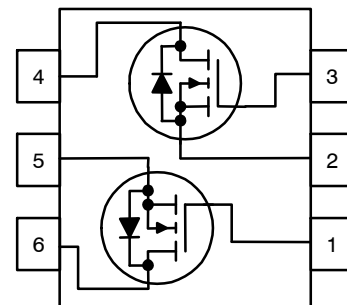
TSOT23 6-Lead
SUPERSOT-6
CASE 419BL

MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	105	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	–	–	10	μA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –20 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	2.6	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	–5	–	mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 1.0 A V _{GS} = 6 V, I _D = 0.9 A V _{GS} = 10 V, I _D = 1.0 A, T _J = 125°C	–	370 396 685	500 550 976	mΩ
I _{D(on)}	On–State Drain Current	V _{GS} = 10 V, V _{DS} = 10 V	3	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 1.0 A	–	3.6	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1.0 MHz	–	153	–	pF
C _{oss}	Output Capacitance		–	5	–	pF
C _{rss}	Reverse Transfer Capacitance		–	1	–	pF

SWITCHING CHARACTERISTICS (Note 2)

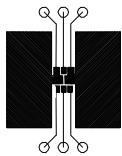
t _{d(on)}	Turn–On Delay Time	V _{DD} = 50 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	8	16	ns
t _r	Turn–On Rise Time		–	4	8	ns
t _{d(off)}	Turn–Off Delay Time		–	11	20	ns
t _f	Turn–Off Fall Time		–	6	12	ns
Q _g	Total Gate Charge	V _{DS} = 50 V, I _D = 1.0 A, V _{GS} = 10 V	–	3.7	5	nC
Q _{gs}	Gate–Source Charge		–	0.8	–	nC
Q _{gd}	Gate–Drain Charge		–	1	–	nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

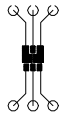
I _S	Maximum Continuous Drain–Source Diode Forward Current	–	–	0.8	A	
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.8 A (Note 2)	–	0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

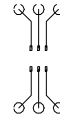
- R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



- a. 130°C/W when mounted on a 0.125 in² pad of 2 oz. copper.



- b. 140°C/W when mounted on a .005 in² pad of 2 oz. copper.



- c. 180°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS

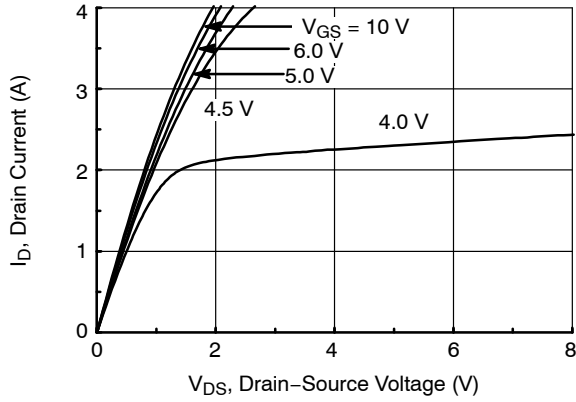


Figure 1. On-Region Characteristics

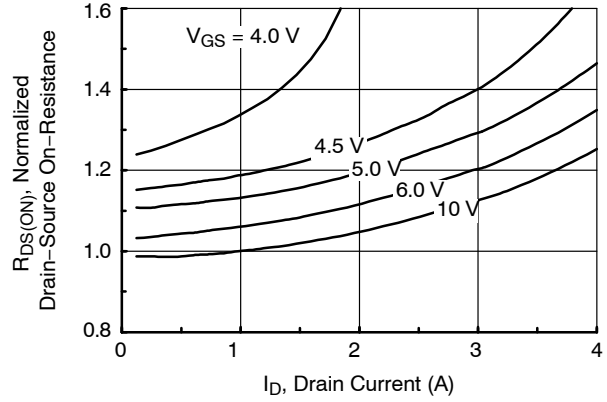


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

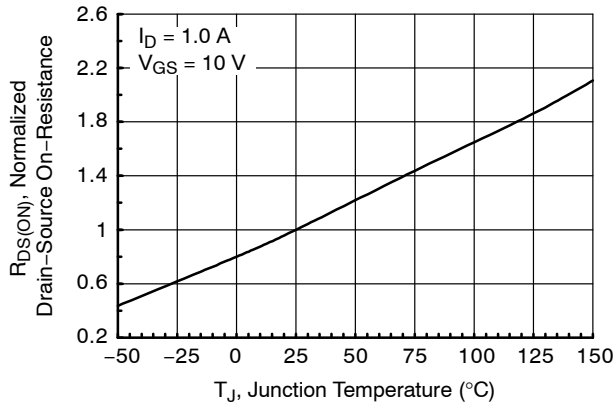


Figure 3. On-Resistance Variation with Temperature

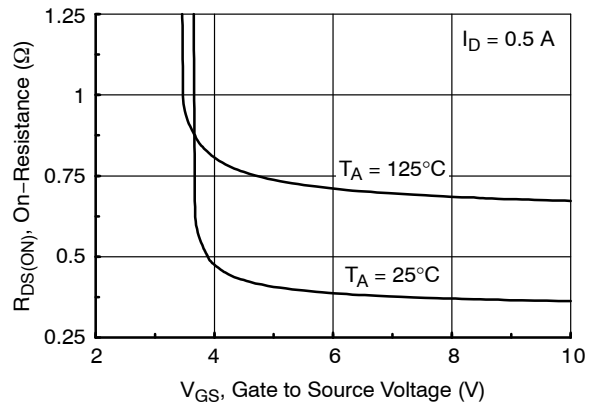


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

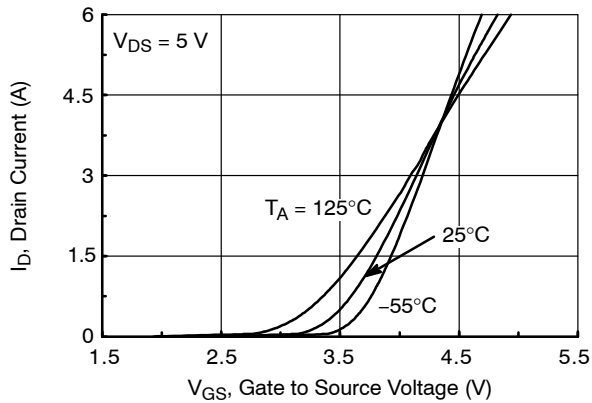


Figure 5. Transfer Characteristics

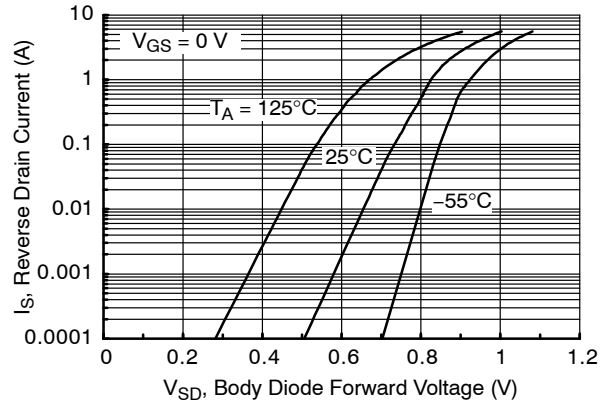


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

FDC3601N

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

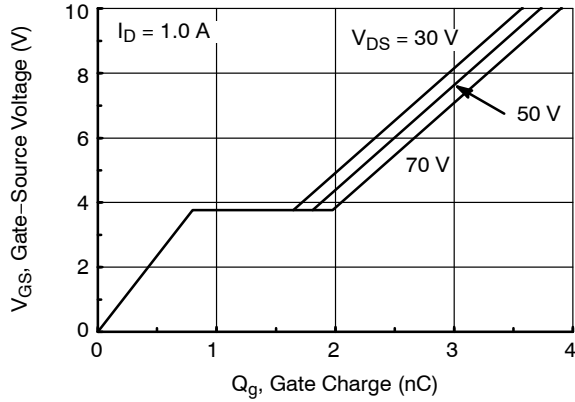


Figure 7. Gate Charge Characteristics

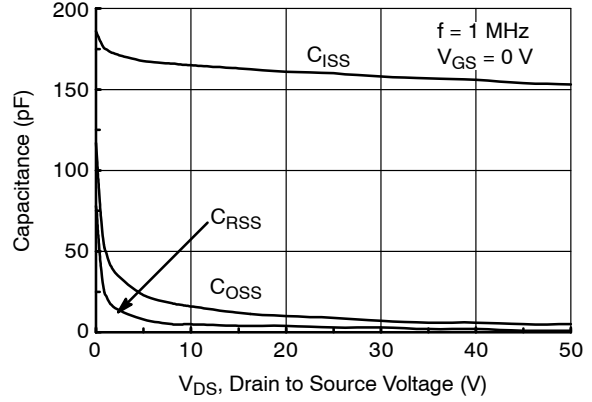


Figure 8. Capacitance Characteristics

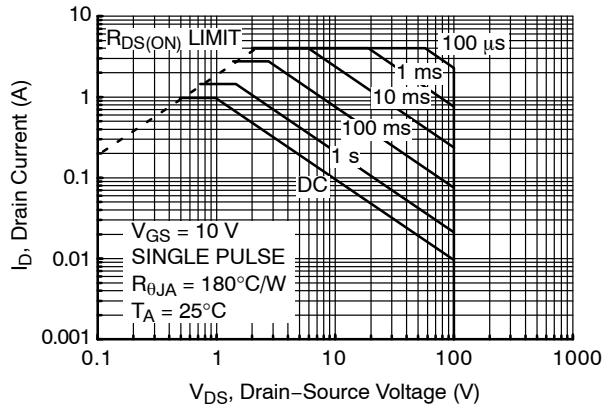


Figure 9. Maximum Safe Operating Area

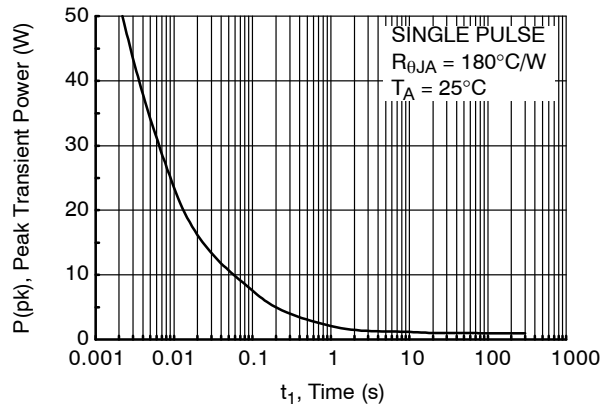


Figure 10. Single Pulse Maximum Power Dissipation

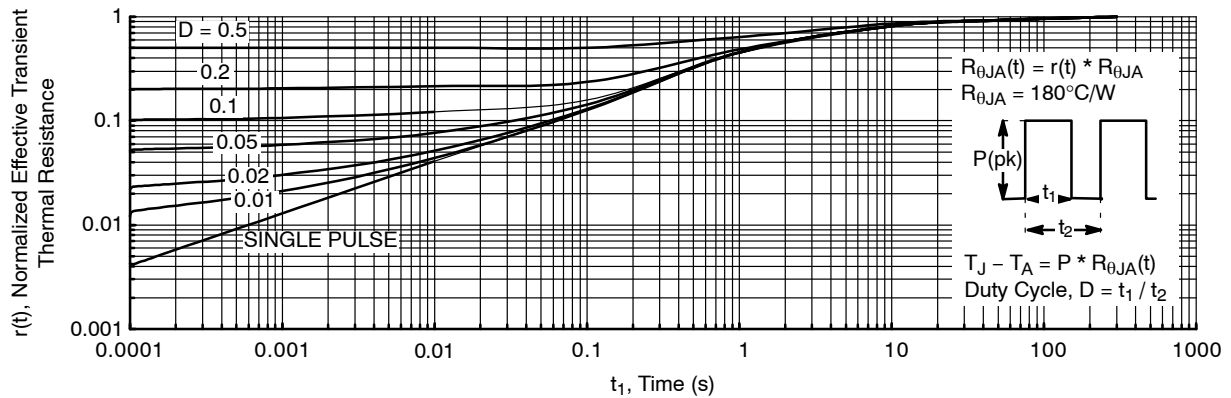


Figure 11. Transient Thermal Response Curve

(Note: Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.)

FDC3601N

ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDC3601N	.601	TSOT-23-6 (Pb-free)	7"	8 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

TSOT23 6-Lead CASE 419BL ISSUE A

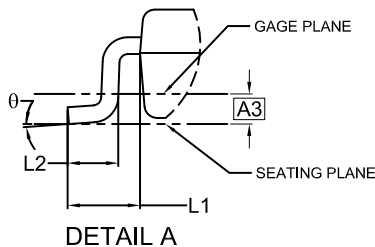
DATE 31 AUG 2020



TOP VIEW



FRONT VIEW

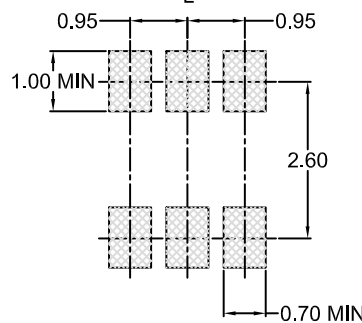


DETAIL A



SIDE VIEW

SYMM



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
Θ	0°	--	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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