

MOSFET – N-Channel, POWERTRENCH®

150 V, 169 A, 6.3 mΩ

FDBL86210-F085

Features

- Typical $r_{DS(on)} = 5\text{ m}\Omega$ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- Typical $Q_{g(tot)} = 70\text{ nC}$ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous ($V_{GS} = 10$), $T_C = 25^\circ\text{C}$ (Note 1)	169	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	502	mJ
P_D	Power Dissipation	500	W
	Derate Above 25°C	3.3	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

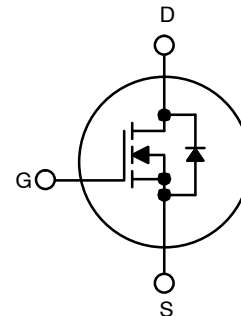
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting $T_J = 25^\circ\text{C}$, $L = 0.24\text{ mH}$, $I_{AS} = 64\text{ A}$, $V_{DD} = 100\text{ V}$ during inductor charging and $V_{DD} = 0\text{ V}$ during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

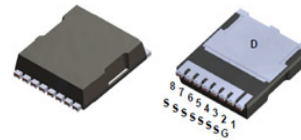


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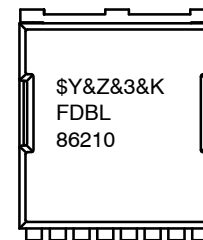


N-Channel



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86210	= Specific Device Code

ORDERING INFORMATION

Device	Top Mark	Package	Shipping†
FDBL86210-F085	FDBL86210	H-PSOF8L	2000 Units/ Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDBL86210-F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

B _V DSS	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	150	–	–	V	
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 150 V, V _{GS} = 0 V	T _J = 25°C	–	–	1	μA
			T _J = 175°C (Note 4)	–	–	1	mA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA	

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	2.8	4.0	V	
r _{DS(on)}	Drain to Source On Resistance	I _D = 80 A, V _{GS} = 10 V	T _J = 25°C	–	5	6.3	mΩ
			T _J = 175°C (Note 4)	–	14	17.5	mΩ

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz	–	5805	–	pF
C _{oss}	Output Capacitance		–	536	–	pF
C _{rss}	Reverse Transfer Capacitance		–	16	–	pF
R _g	Gate Resistance	f = 1 MHz	–	2.2	–	Ω
Q _{g(toT)}	Total Gate Charge at 10 V	V _{GS} = 0 to 10 V V _{DD} = 75 V, I _D = 80 A	–	70	90	nC
Q _{g(th)}	Threshold Gate Charge		V _{GS} = 0 to 2 V	–	10.5	13
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 75 V, I _D = 80 A	–	32.5	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	10	–	nC

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 75 V, I _D = 80 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	–	80	ns
t _{d(on)}	Turn-On Delay Time		–	39	–	ns
t _r	Rise Time		–	30	–	ns
t _{d(off)}	Turn-Off Delay Time		–	70	–	ns
t _f	Fall Time		–	23	–	ns
t _{off}	Turn-Off Time		–	–	130	ns

DRAIN-SOURCE DIODE CHARACTERISTIC

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 80 A, V _{GS} = 0 V	–	–	1.25	V
		I _{SD} = 40 A, V _{GS} = 0 V	–	–	1.2	V
T _{rr}	Reverse Recovery Time	I _F = 80 A, dI _{SD} /dt = 100 A/μs, V _{DD} = 120 V	–	108	125	ns
Q _{rr}	Reverse Recovery Charge		–	323	467	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

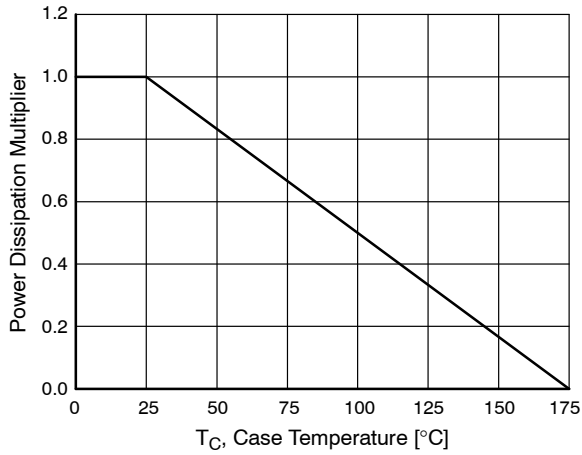


Figure 1. Normalized Power Dissipation vs. Case Temperature

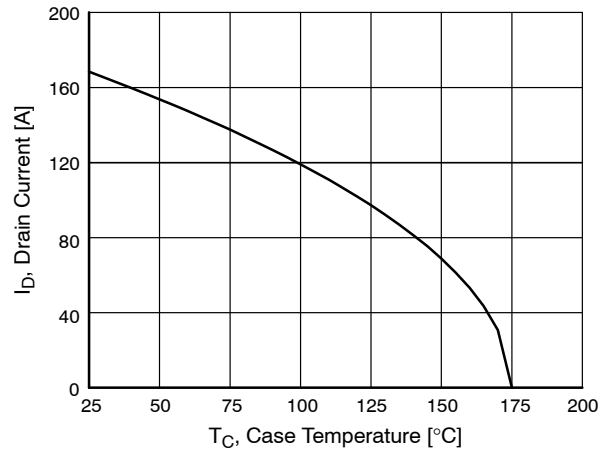


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

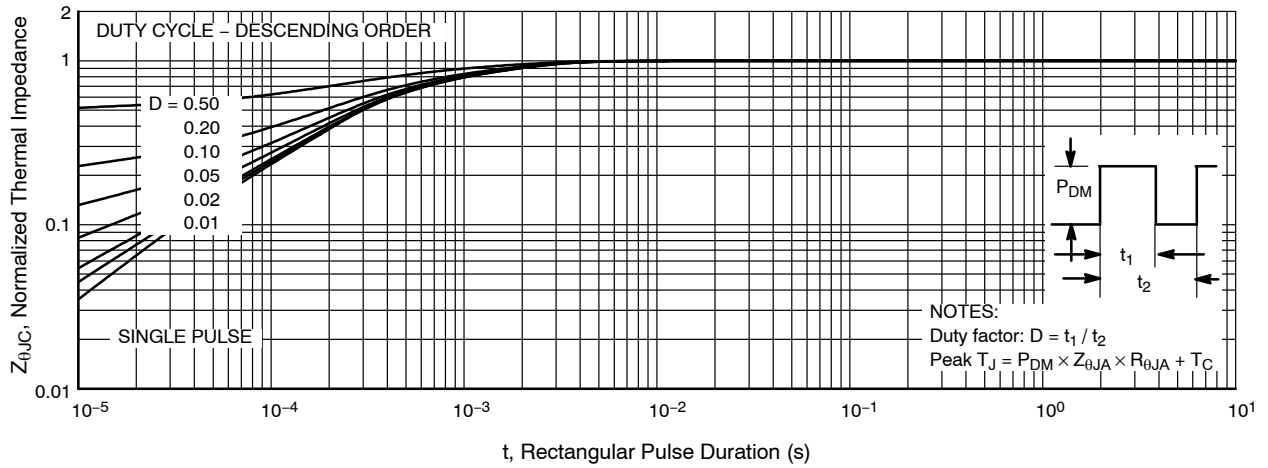


Figure 3. Normalized Maximum Transient Thermal Impedance

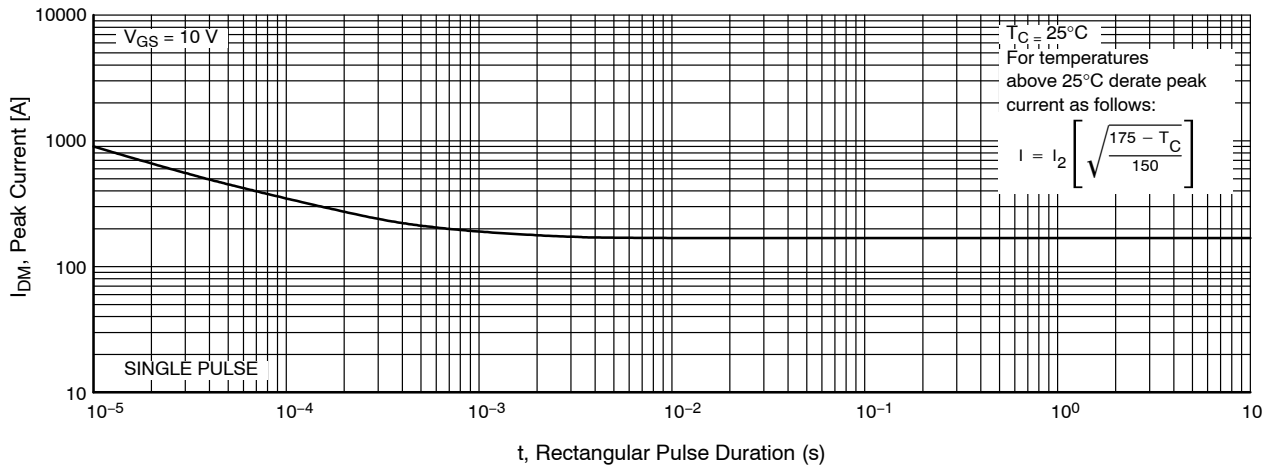


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

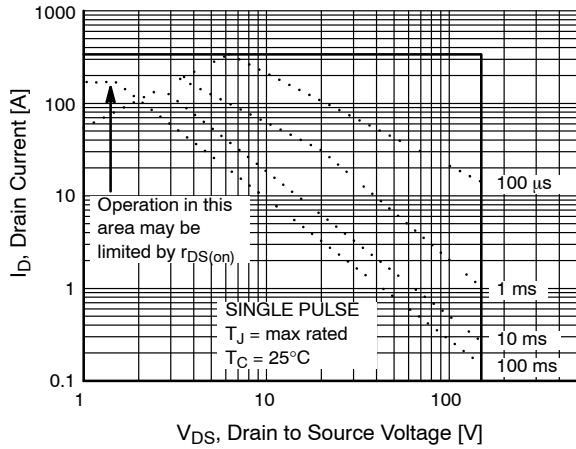
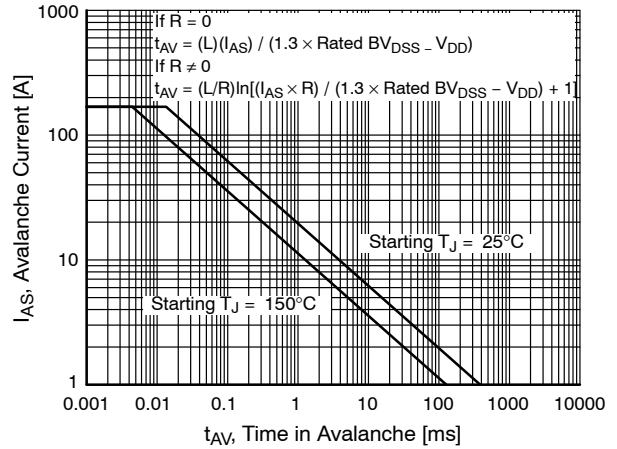


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes [AN7514](#) and [AN7515](#).

Figure 6. Unclamped Inductive Switching Capability

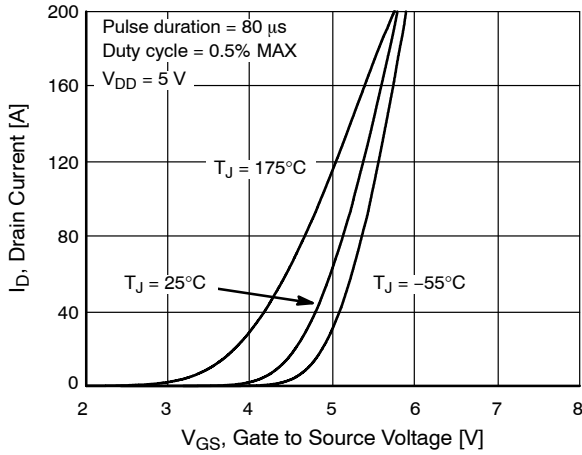


Figure 7. Transfer Characteristics

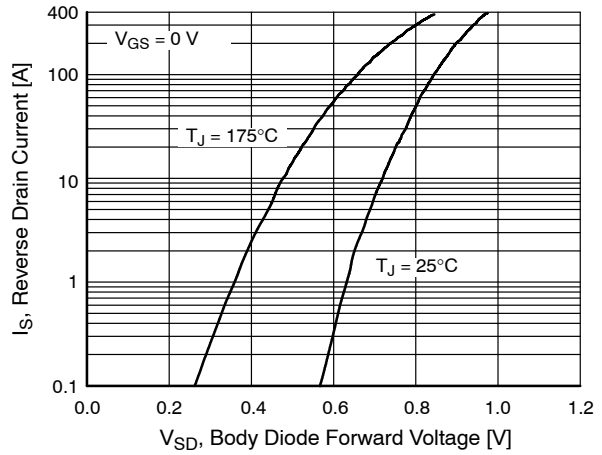


Figure 8. Forward Diode Characteristics

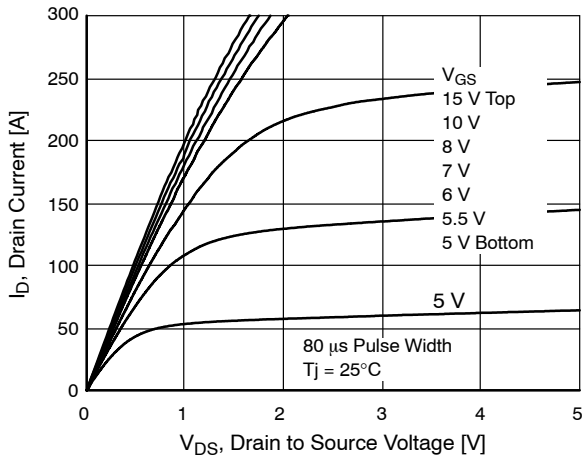


Figure 9. Saturation Characteristics

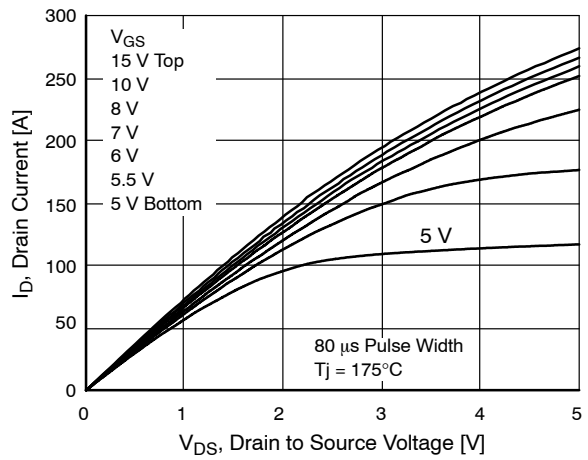


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

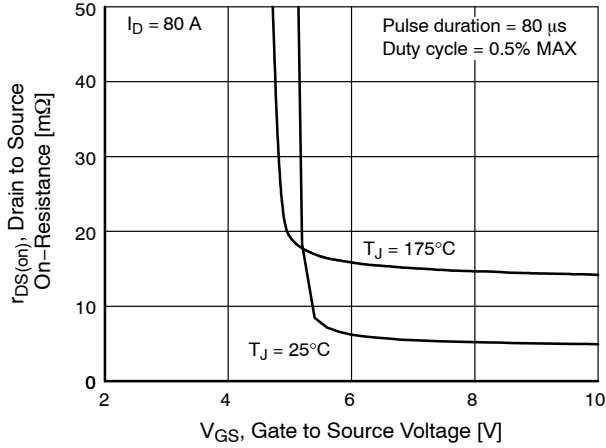


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

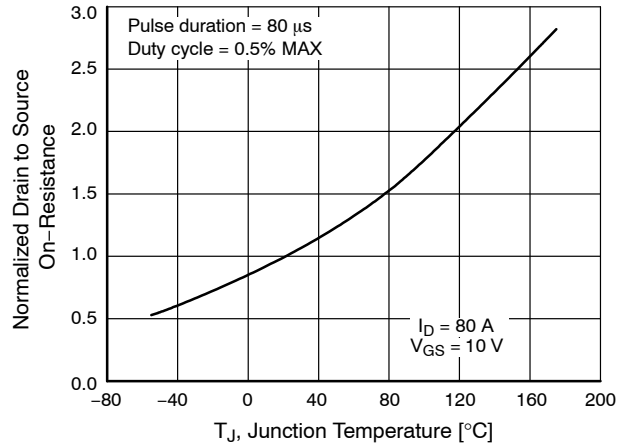


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

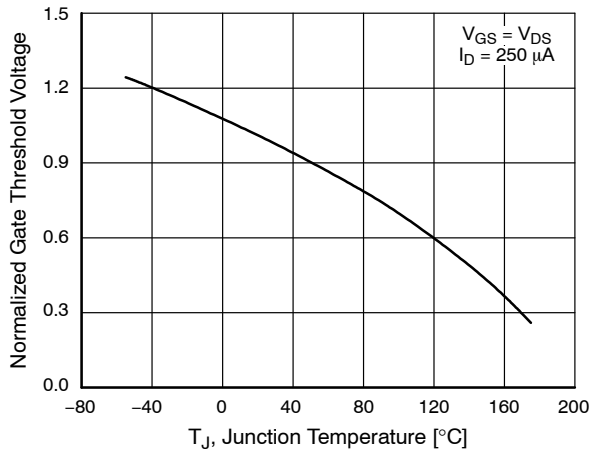


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

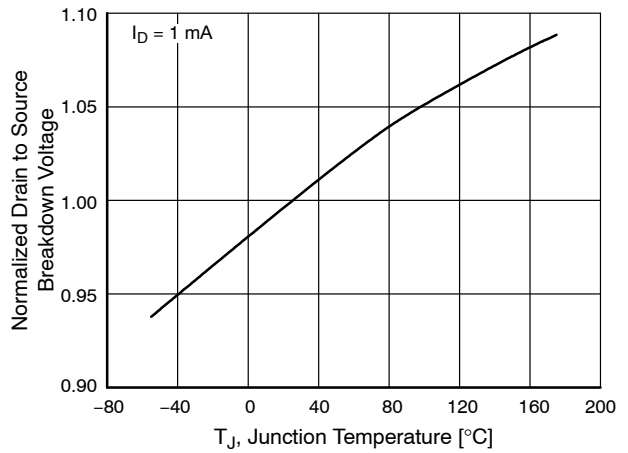


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

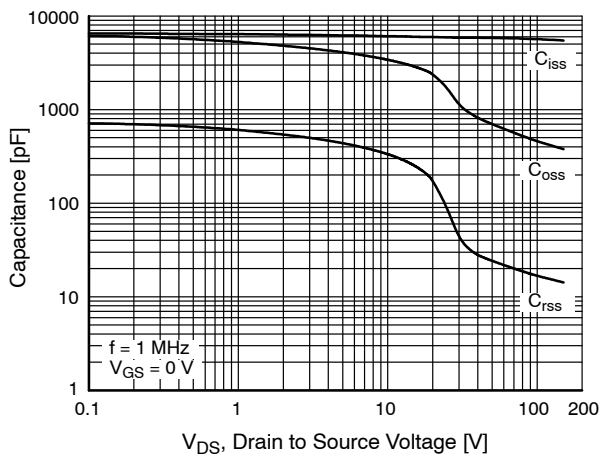


Figure 15. Capacitance vs. Drain to Source Voltage

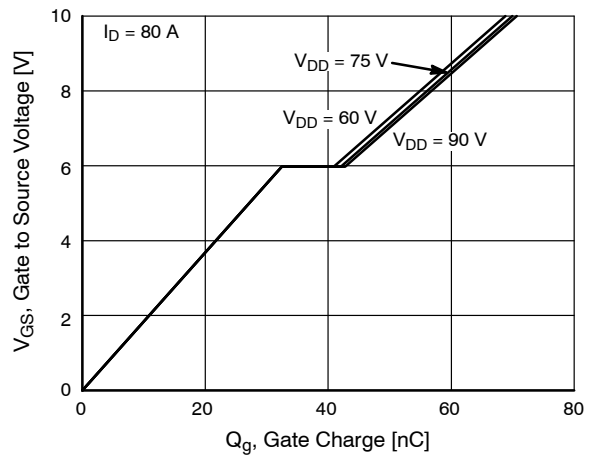


Figure 16. Gate Charge vs. Gate to Source Voltage

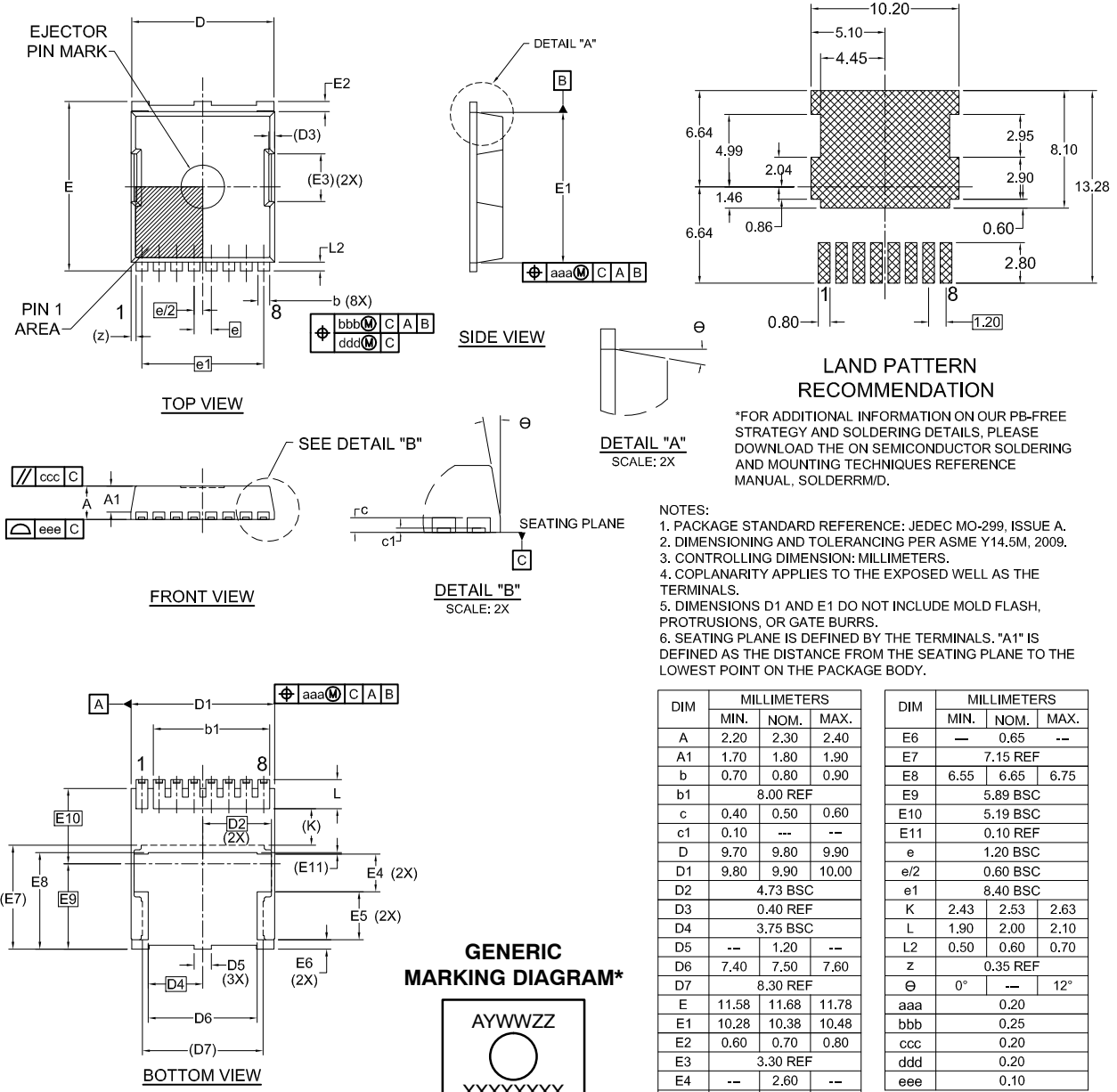
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



H-PSOF8L 11.68x9.80
CASE 100CU
ISSUE B

DATE 20 MAY 2022



LAND PATTERN RECOMMENDATION

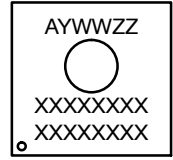
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 3. CONTROLLING DIMENSION: MILLIMETERS.
 4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
 5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	---	1.20	---
D6	7.40	7.50	7.60
D7	8.30 REF		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	---	2.60	---
E5	---	3.30	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E6	---	0.65	---
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		
E11	0.10 REF		
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	2.43	2.53	2.63
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	H-PSOF8L 11.68x9.80	PAGE 1 OF 1

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