

MOSFET – N-Channel, POWERTRENCH®

100 V, 240 A, 2.6 mΩ

FDBL86063-F085

Features

- Typical $R_{DS(on)}$ = 2 mΩ at $V_{GS} = 10$ V, $I_D = 80$ A
- Typical $Q_{g(tot)}$ = 73 nC at $V_{GS} = 10$ V, $I_D = 80$ A
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

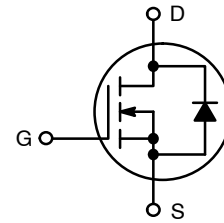
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current – Continuous, ($V_{GS} = 10$ V) (Note 1) $T_C = 25^\circ\text{C}$	240	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	(See Figure 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	160	mJ
P_D	Power Dissipation	357	W
	Derate Above 25°C	2.38	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

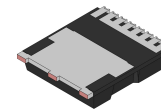
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 50 \mu\text{H}$, $I_{AS} = 80$ A, $V_{DD} = 100$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
100 V	2.6 mΩ @ 10 V	240 A



N-CHANNEL MOSFET



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FDBL86063 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDBL86063–F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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OFF CHARACTERISTICS

B _V DSS	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	100	–	–	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 25°C	–	–	1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 175°C (Note 4)	–	–	1.5	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	2.9	4.0	V
R _{DS(on)}	Drain-to-Source On-Resistance	I _D = 80 A, V _{GS} = 10 V, T _J = 25°C	–	2.0	2.6	mΩ
		I _D = 80 A, V _{GS} = 10 V, T _J = 175°C (Note 4)	–	4.2	5.6	

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		–	5120	–	pF
C _{oss}	Output Capacitance			–	3220	–	pF
C _{rss}	Reverse Transfer Capacitance			–	32	–	pF
R _g	Gate Resistance	V _{GS} = 0.5 V, f = 1 MHz		–	0.4	–	Ω
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V	V _{DD} = 50 V, I _D = 80 A	–	73	95	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 V to 2 V		–	9	–	nC
Q _{gs}	Gate-to-Source Gate Charge			–	22	–	nC
Q _{gd}	Gate-to-Drain "Miller" Charge			–	17	–	nC

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 50 V, I _D = 80 A, V _{GS} = 10V, R _{GEN} = 6 Ω	–	–	53	ns
t _{d(on)}	Turn-On Delay		–	25	–	ns
t _r	Rise Time		–	16	–	ns
t _{d(off)}	Turn-Off Delay		–	32	–	ns
t _f	Fall Time		–	8	–	ns
t _{off}	Turn-Off Time		–	–	51	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-to-Drain Diode Voltage	I _{SD} = 80 A, V _{GS} = 0 V I _{SD} = 40 A, V _{GS} = 0 V	–	0.9 0.8	1.25 1.2	V
t _{rr}	Reverse-Recovery Time	I _F = 80 A, ΔI _{SD} /Δt = 100 A/μs	–	107	139	ns
Q _{rr}	Reverse-Recovery Charge		–	175	260	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
FDBL86063–F085	FDBL86063	H-PSOF8L 11.68x9.80 (Pb-Free)	2000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

TYPICAL CHARACTERISTICS

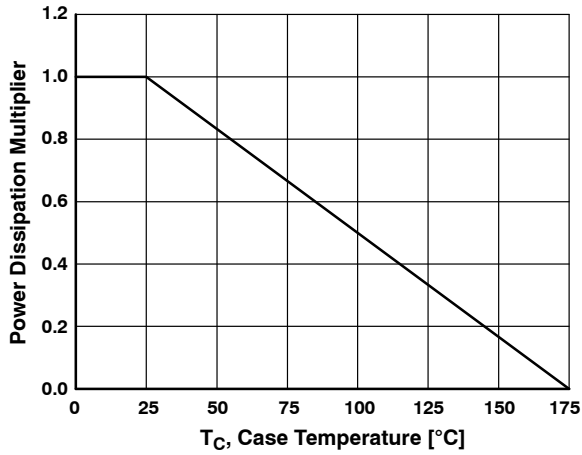


Figure 1. Normalized Power Dissipation vs. Case Temperature

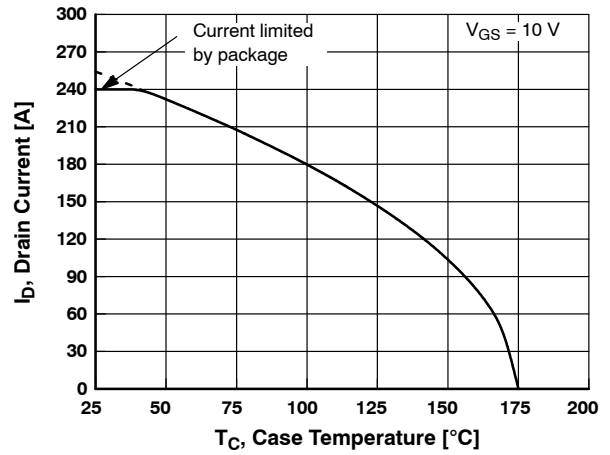


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

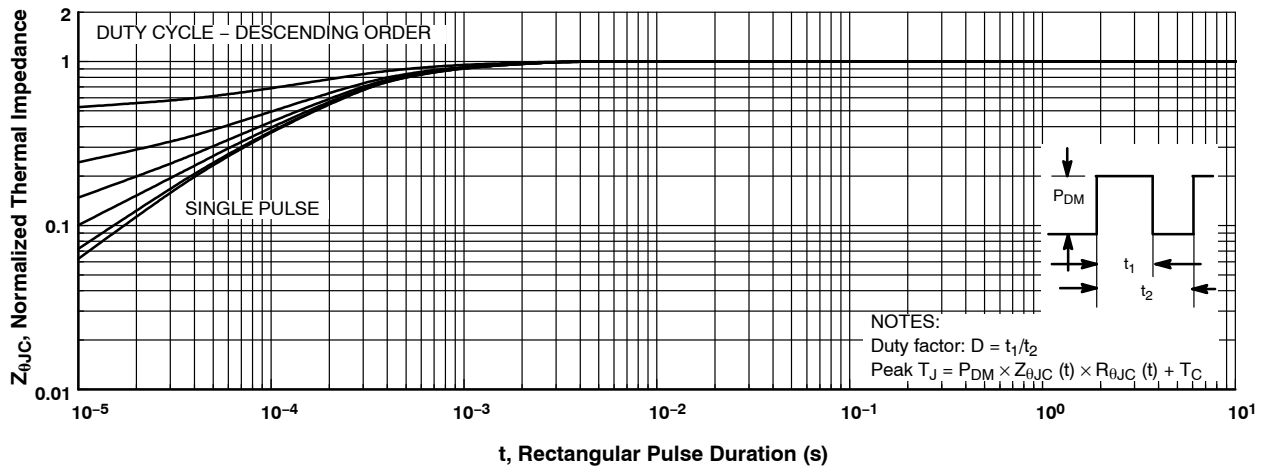


Figure 3. Normalized Maximum Transient Thermal Impedance

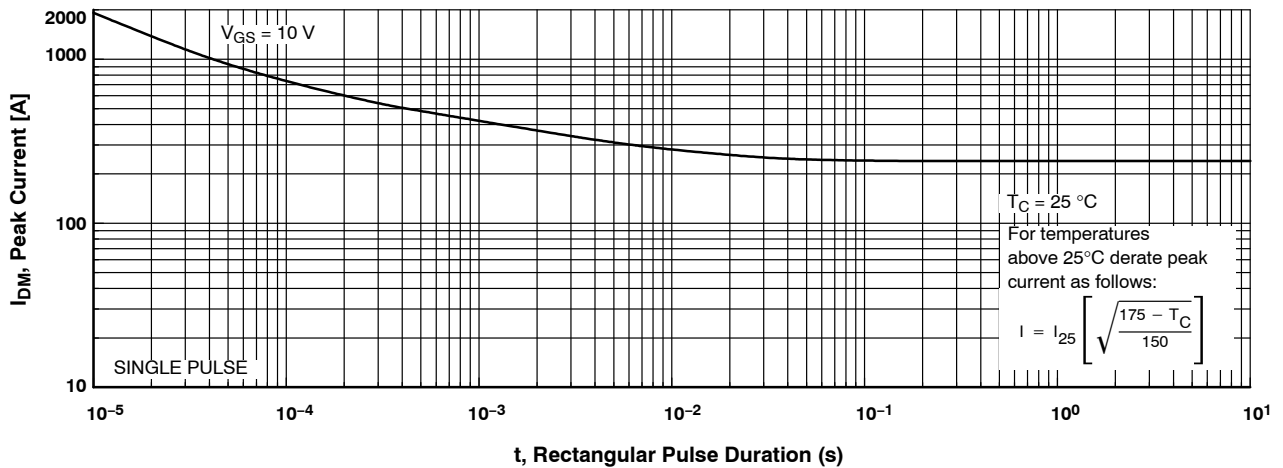


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

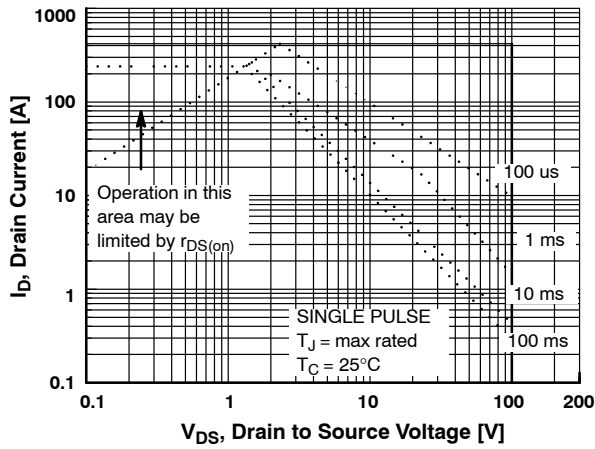
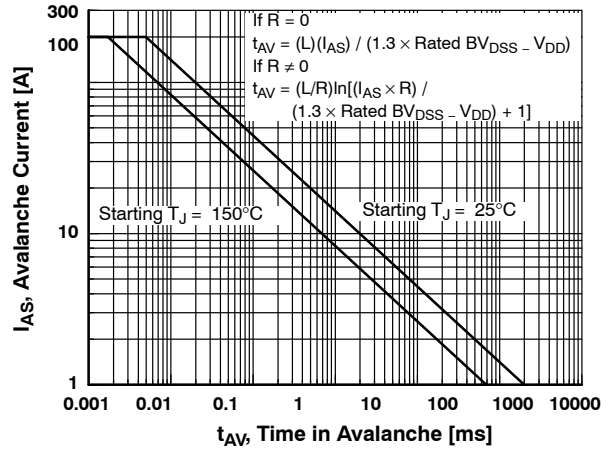


Figure 5. Forward Bias Safe Operating Area



Refer to onsemi Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

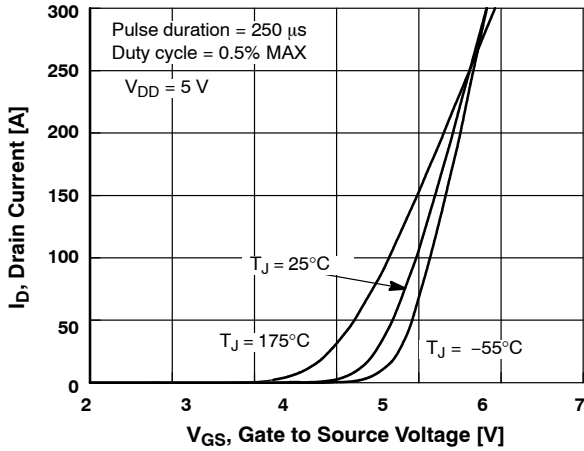


Figure 7. Transfer Characteristics

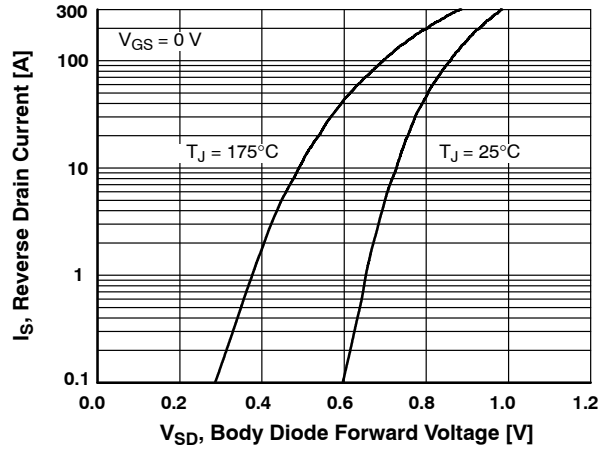


Figure 8. Forward Diode Characteristics

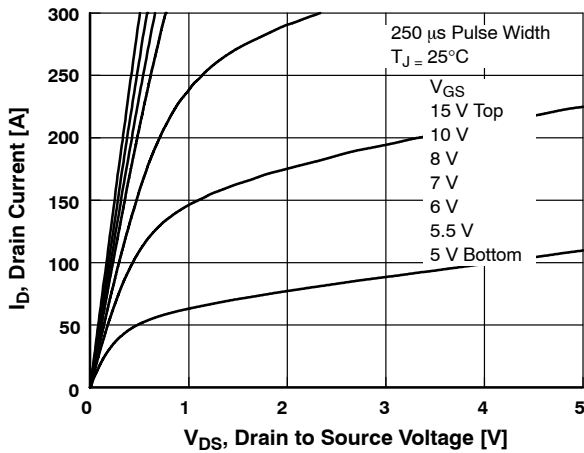


Figure 9. Saturation Characteristics

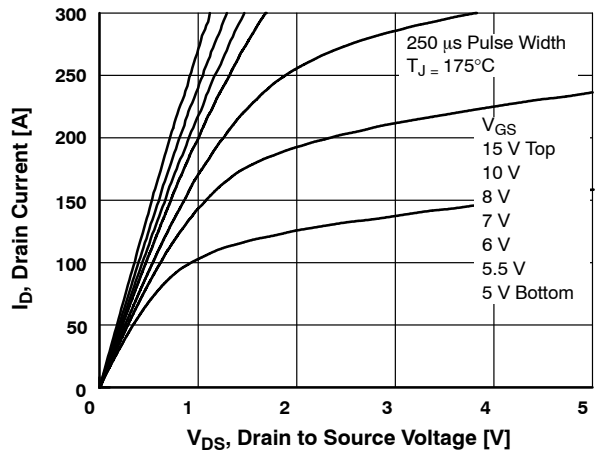


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

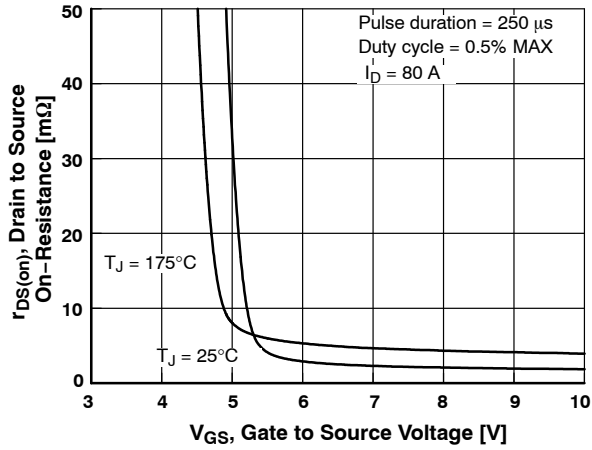


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

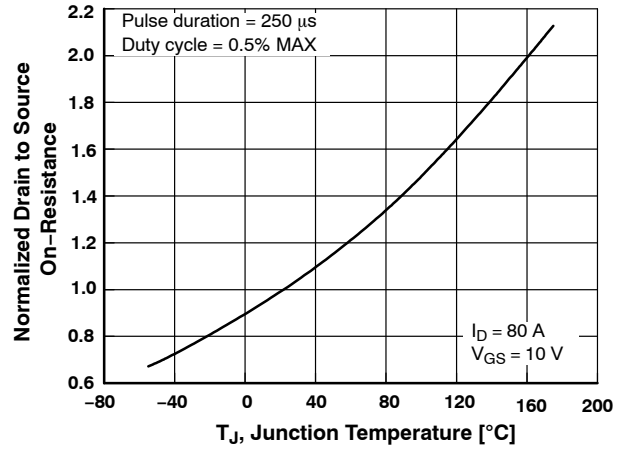


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

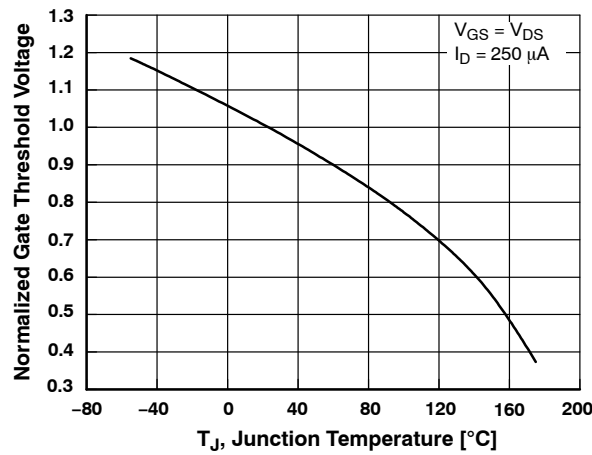


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

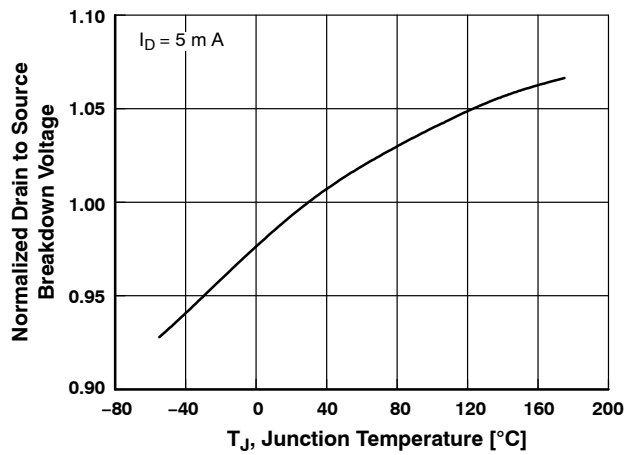


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

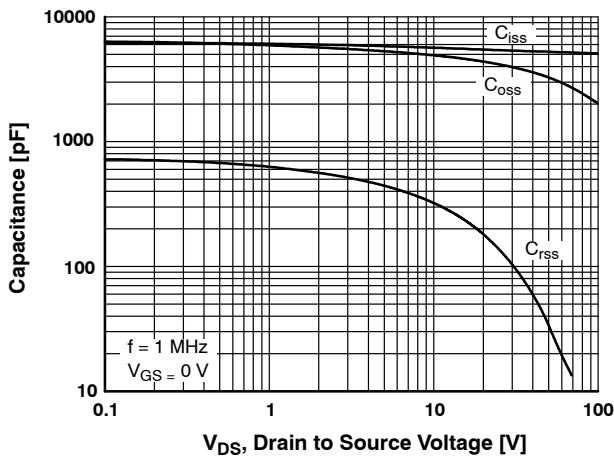


Figure 15. Capacitance vs. Drain to Source Voltage

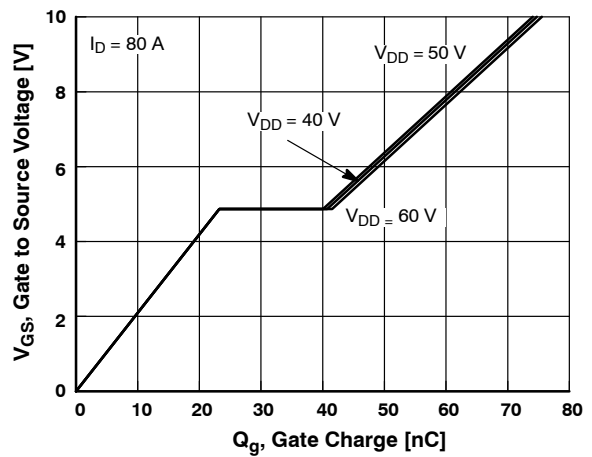
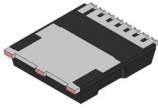


Figure 16. Gate Charge vs. Gate to Source Voltage

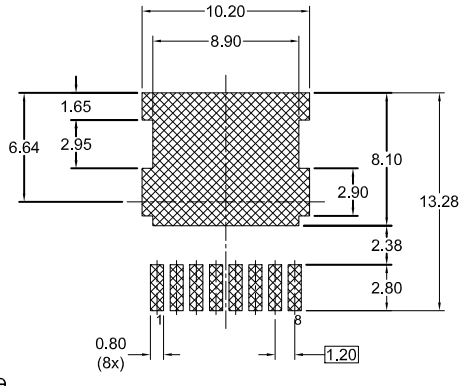
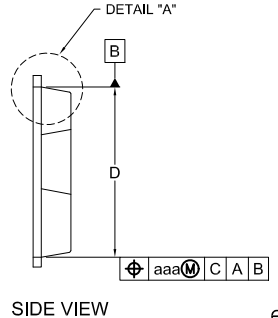
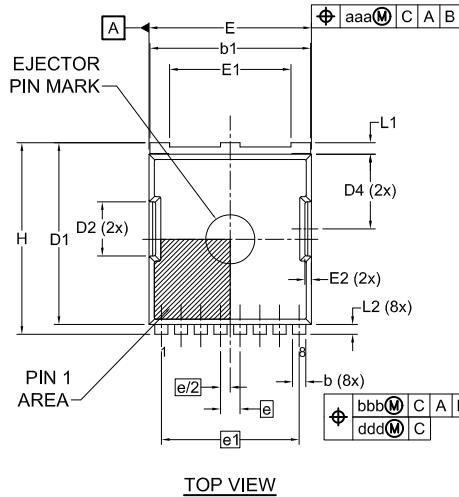
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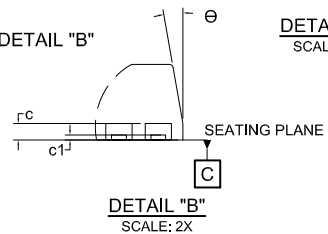
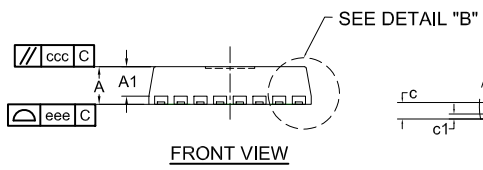


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CASE 100CU
ISSUE C

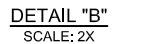
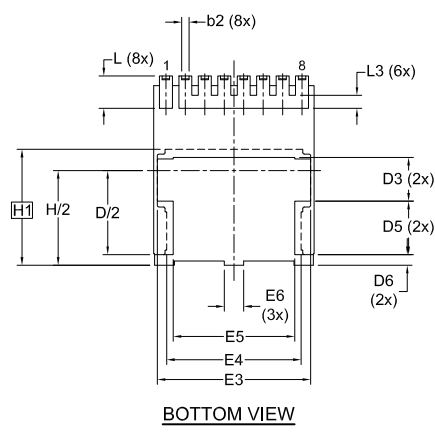
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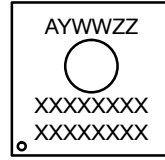
LAND PATTERN RECOMMENDATION
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- XXXX = Specific Device Code

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
theta	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

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