

# FDBL0630N150

## MOSFET – N-Channel, POWERTRENCH®

**150 V, 169 A, 6.3 mΩ**

### Features

- Typ  $r_{DS(on)}$  = 5 mΩ at  $V_{GS} = 10$  V,  $I_D = 80$  A
- Typ  $Q_{g(tot)}$  = 70 nC at  $V_{GS} = 10$  V,  $I_D = 80$  A
- UIS Capability
- This Device is Pb-Free and is RoHS Compliant

### Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

| Symbol          | Parameter   | Ratings         | Unit               |
|-----------------|---|-----------------|--------------------|
| $V_{DSS}$       | Drain to Source Voltage   | 150             | V                  |
| $V_{GS}$        | Gate to Source Voltage  | $\pm 20$        | V                  |
| $I_D$           | Drain Current – Continuous ( $V_{GS} = 10$ V)<br>(Note 1)<br>$T_C = 25^\circ\text{C}$ | 169             | A                  |
|                 | Pulsed Drain Current<br>$T_C = 25^\circ\text{C}$                                      | See Figure 4    |                    |
| EAS             | Single Pulse Avalanche Energy (Note 2)  | 502             | mJ                 |
| $P_D$           | Power Dissipation   | 500             | W                  |
|                 | Derate above $25^\circ\text{C}$   | 3.3             | $W/^\circ\text{C}$ |
| $T_J, T_{STG}$  | Operating and Storage Temperature   | $-55$ to $+175$ | $^\circ\text{C}$   |
| $R_{\theta JC}$ | Thermal Resistance Junction to Case   | 0.3             | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Maximum Thermal Resistance Junction to Ambient (Note 3)                               | 43              | $^\circ\text{C/W}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

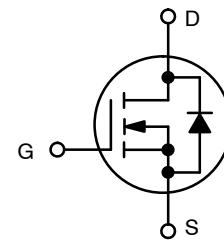
1. Current is limited by junction temperature.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.24$  mH,  $I_{AS} = 64$  A,  $V_{DD} = 100$  V during inductor charging and  $V_{DD} = 0$  V during time in avalanche.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2 oz copper.



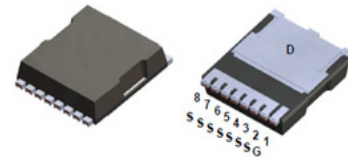
**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

| $V_{DSS}$ | $r_{DS(ON)}$ MAX | $I_D$ MAX |
|-----------|------------------|-----------|
| 150 V     | 6.3 mΩ @ 10 V    | 169 A     |



MOSFET — N-Channel



H-PSOF8L 11.68x9.80  
CASE 100CU

### MARKING DIAGRAM



$\$Y$  = ON Semiconductor Logo  
 $\&Z$  = Assembly Plant Code  
 $\&3$  = Date Code  
 $\&K$  = Lot Run Traceability Code  
 FDBL0630N150 = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDBL0630N150

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|--------|-----------|----------------|-----|-----|-----|------|
|--------|-----------|----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                  |                                   |  |                                 |   |      |    |    |
|------------------|-----------------------------------|--|---------------------------------|---|------|----|----|
| B <sub>VDS</sub> | Drain to Source Breakdown Voltage | I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V | 150                             | – | –    | V  |    |
| I <sub>DSS</sub> | Drain to Source Leakage Current   | V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V | T <sub>J</sub> = 25°C           | – | –    | 1  | μA |
|                  |                                   |  | T <sub>J</sub> = 175°C (Note 4) | – | –    | 1  | mA |
| I <sub>GSS</sub> | Gate to Source Leakage Current    | V <sub>GS</sub> = ±20 V                        | –                               | – | ±100 | nA |    |

### ON CHARACTERISTICS

|                     |                                  |   |                                 |     |     |      |    |
|---------------------|----------------------------------|---|---------------------------------|-----|-----|------|----|
| V <sub>GS(th)</sub> | Gate to Source Threshold Voltage | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA | 2.0                             | 2.8 | 4.0 | V    |    |
| r <sub>DS(on)</sub> | Drain to Source On Resistance    | I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V               | T <sub>J</sub> = 25°C           | –   | 5   | 6.3  | mΩ |
|                     |                                  |   | T <sub>J</sub> = 175°C (Note 4) | –   | 14  | 17.5 | mΩ |

### DYNAMIC CHARACTERISTICS

|                     |                               |  |   |      |    |    |
|---------------------|-------------------------------|--|---|------|----|----|
| C <sub>iss</sub>    | Input Capacitance             | V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V, f = 1 MHz                   | – | 5805 | –  | pF |
| C <sub>oss</sub>    | Output Capacitance            |  | – | 536  | –  | pF |
| C <sub>rss</sub>    | Reverse Transfer Capacitance  |  | – | 16   | –  | pF |
| R <sub>g</sub>      | Gate Resistance               | f = 1 MHz  | – | 2.2  | –  | Ω  |
| Q <sub>g(ToT)</sub> | Total Gate Charge at 10 V     | V <sub>GS</sub> = 0 to 10 V, V <sub>DD</sub> = 75 V, I <sub>D</sub> = 80 A | – | 70   | 90 | nC |
| Q <sub>g(th)</sub>  | Threshold Gate Charge         | V <sub>GS</sub> = 0 to 2 V, V <sub>DD</sub> = 75 V, I <sub>D</sub> = 80 A  | – | 10.5 | 13 | nC |
| Q <sub>gs</sub>     | Gate to Source Gate Charge    | V <sub>DD</sub> = 75 V, I <sub>D</sub> = 80 A                              | – | 32.5 | –  | nC |
| Q <sub>gd</sub>     | Gate to Drain "Miller" Charge | V <sub>DD</sub> = 75 V, I <sub>D</sub> = 80 A                              | – | 10   | –  | nC |

### SWITCHING CHARACTERISTICS

|                     |                     |   |   |    |     |    |
|---------------------|---------------------|---|---|----|-----|----|
| t <sub>on</sub>     | Turn-On Time        | V <sub>DD</sub> = 75 V, I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω | – | –  | 80  | ns |
| t <sub>d(on)</sub>  | Turn-On Delay Time  |   | – | 39 | –   | ns |
| t <sub>r</sub>      | Rise Time           |   | – | 30 | –   | ns |
| t <sub>d(off)</sub> | Turn-Off Delay Time |   | – | 70 | –   | ns |
| t <sub>f</sub>      | Fall Time           |   | – | 23 | –   | ns |
| t <sub>off</sub>    | Turn-Off Time       |   | – | –  | 130 | ns |

### DRAIN-SOURCE DIODE CHARACTERISTICS

|                 |                               |   |   |     |      |    |
|-----------------|-------------------------------|---|---|-----|------|----|
| V <sub>SD</sub> | Source to Drain Diode Voltage | I <sub>SD</sub> = 80 A, V <sub>GS</sub> = 0 V                                   | – | –   | 1.25 | V  |
|                 |                               | I <sub>SD</sub> = 40 A, V <sub>GS</sub> = 0 V                                   | – | –   | 1.2  | V  |
| T <sub>rr</sub> | Reverse Recovery Time         | I <sub>F</sub> = 80 A, dI <sub>SD</sub> /dt = 100 A/μs, V <sub>DD</sub> = 120 V | – | 108 | 125  | ns |
| Q <sub>rr</sub> | Reverse Recovery Charge       |   | – | 323 | 467  | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T<sub>J</sub> = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

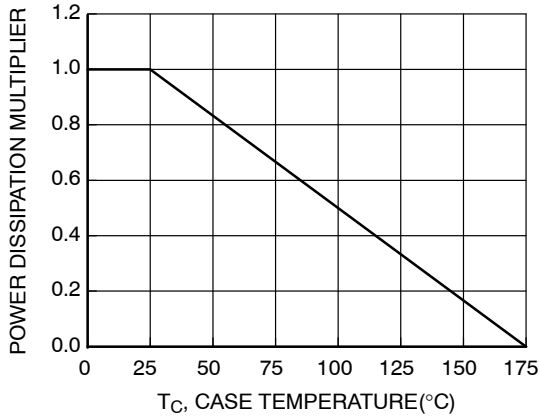


Figure 1. Normalized Power Dissipation vs. Case Temperature

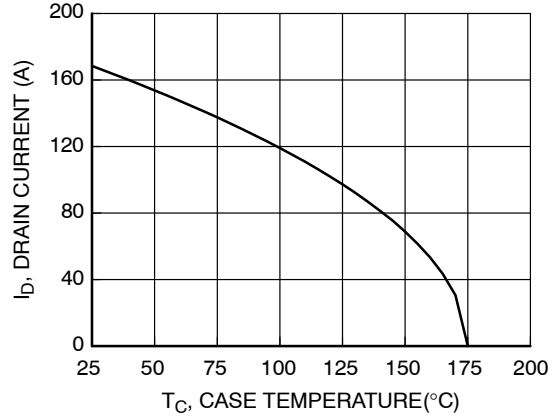


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

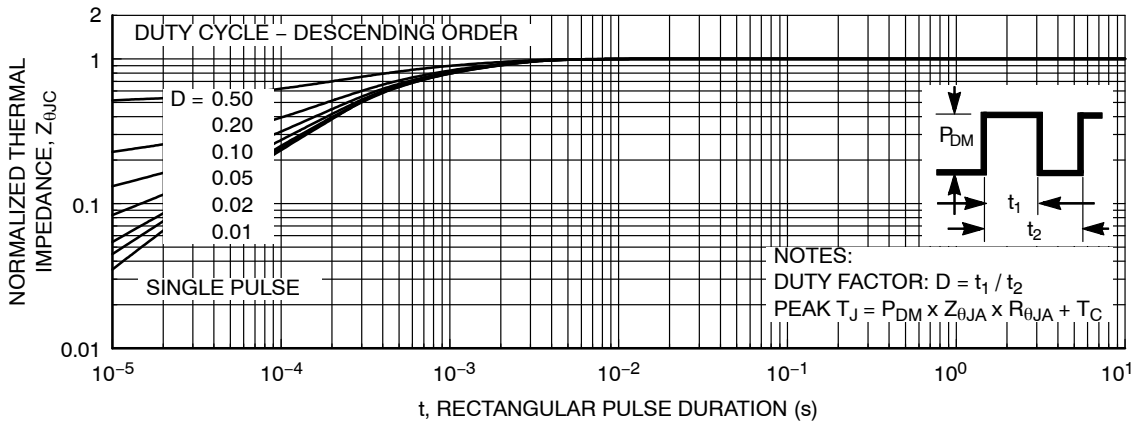


Figure 3. Normalized Maximum Transient Thermal Impedance

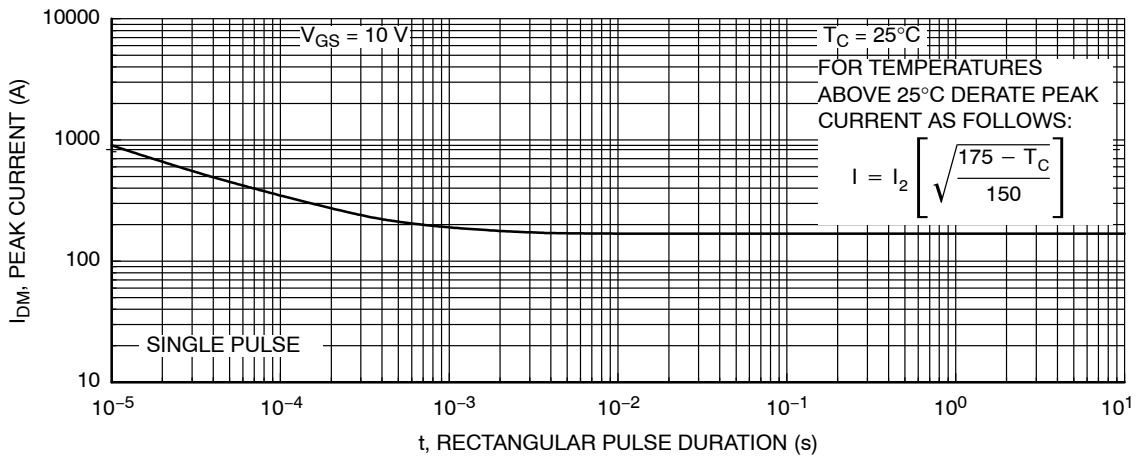


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

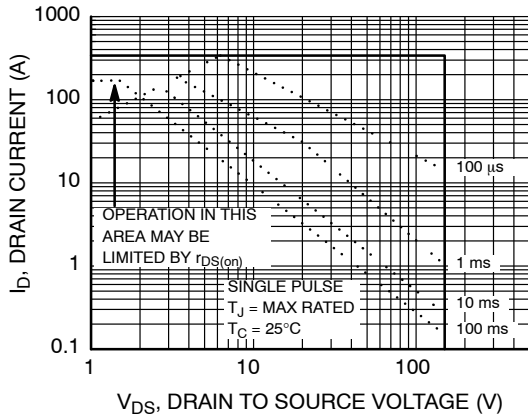


Figure 5. Forward Bias Safe Operating Area

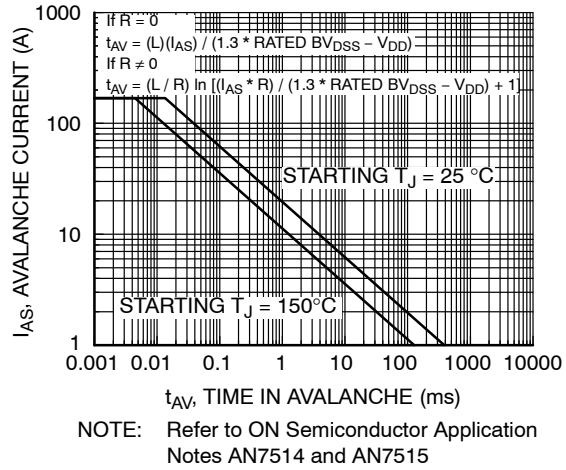


Figure 6. Unclamped Inductive Switching Capability

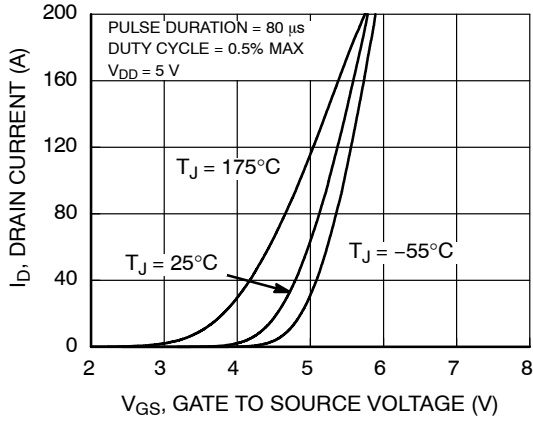


Figure 7. Transfer Characteristics

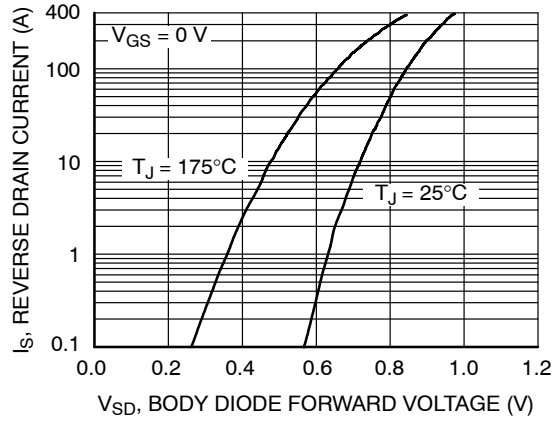


Figure 8. Forward Diode Characteristics

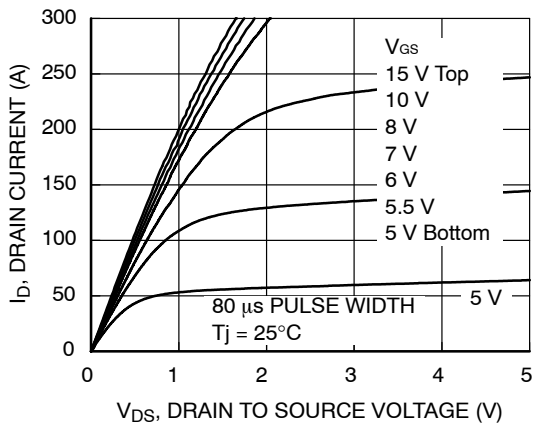


Figure 9. Saturation Characteristics

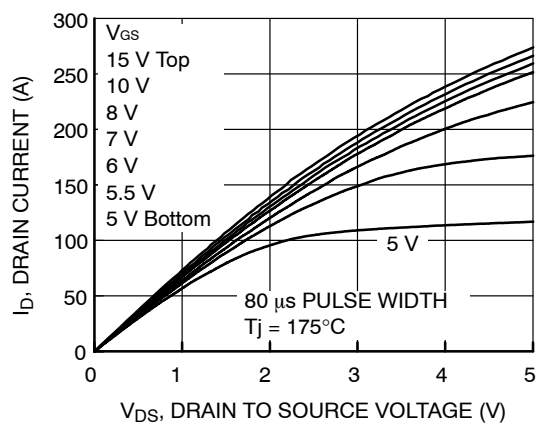


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

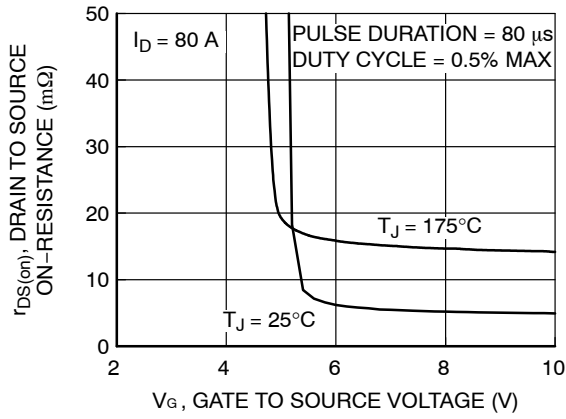


Figure 11. Rdson vs. Gate Voltage

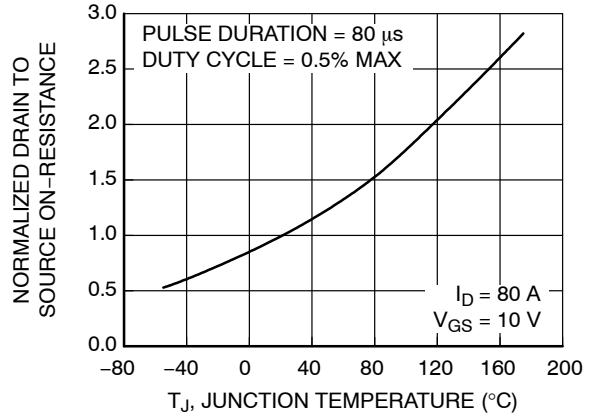


Figure 12. Normalized Rdson vs. Junction Temperature

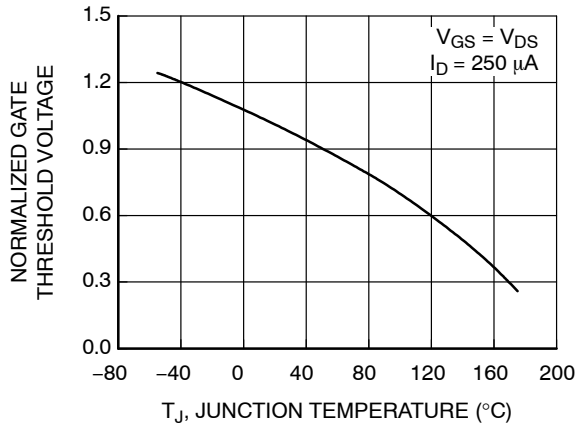


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

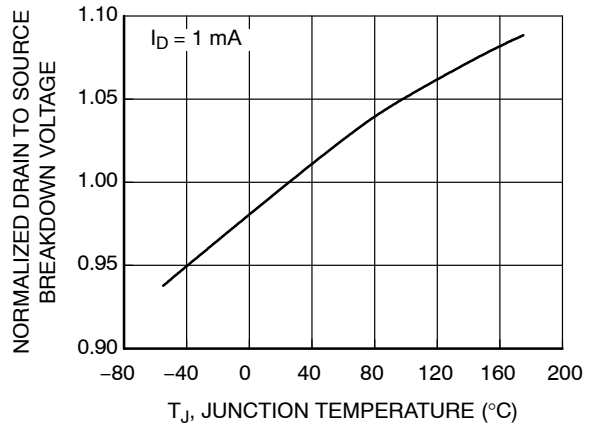


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

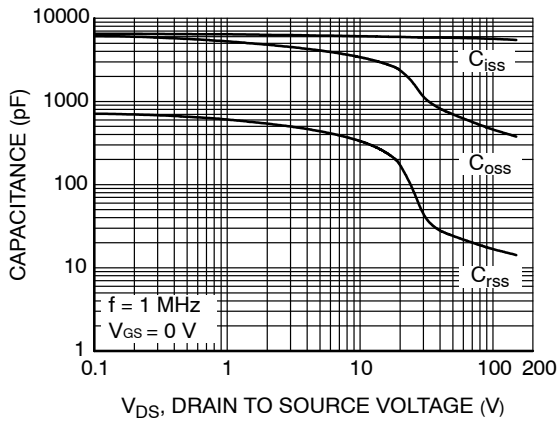


Figure 15. Capacitance vs Drain to Source Voltage

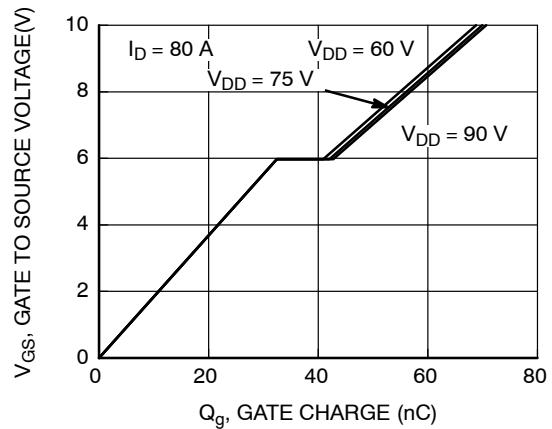


Figure 16. Gate Charge vs Gate to Source Voltage

# FDBL0630N150

## ORDERING INFORMATION

| Device       | Device Marking | Package                          | Shipping <sup>†</sup> |
|--------------|----------------|----------------------------------|-----------------------|
| FDBL0630N150 | FDBL0630N150   | H-PSOF8L 11.68x9.80<br>(Pb-Free) | 2000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

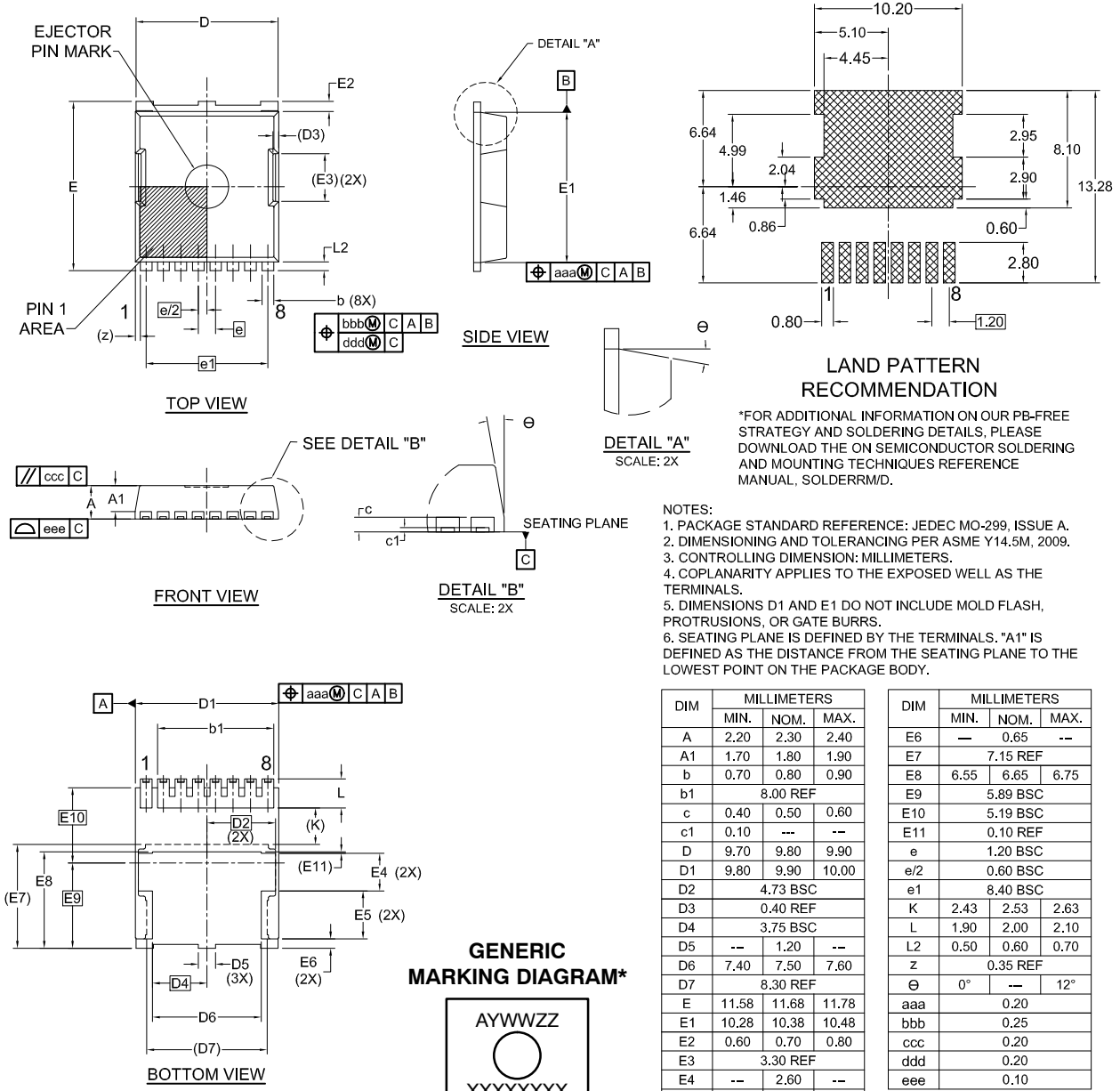
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## H-PSOF8L 11.68x9.80 CASE 100CU ISSUE B

DATE 20 MAY 2022



**LAND PATTERN RECOMMENDATION**

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

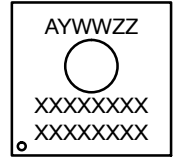
**NOTES:**

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  |
| A   | 2.20        | 2.30  | 2.40  |
| A1  | 1.70        | 1.80  | 1.90  |
| b   | 0.70        | 0.80  | 0.90  |
| b1  | 8.00 REF    |       |       |
| c   | 0.40        | 0.50  | 0.60  |
| c1  | 0.10        | ---   | ---   |
| D   | 9.70        | 9.80  | 9.90  |
| D1  | 9.80        | 9.90  | 10.00 |
| D2  | 4.73 BSC    |       |       |
| D3  | 0.40 REF    |       |       |
| D4  | 3.75 BSC    |       |       |
| D5  | ---         | 1.20  | ---   |
| D6  | 7.40        | 7.50  | 7.60  |
| D7  | 8.30 REF    |       |       |
| E   | 11.58       | 11.68 | 11.78 |
| E1  | 10.28       | 10.38 | 10.48 |
| E2  | 0.60        | 0.70  | 0.80  |
| E3  | 3.30 REF    |       |       |
| E4  | ---         | 2.60  | ---   |
| E5  | ---         | 3.30  | ---   |

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NOM. | MAX. |
| E6  | ---         | 0.65 | ---  |
| E7  | 7.15 REF    |      |      |
| E8  | 6.55        | 6.65 | 6.75 |
| E9  | 5.89 BSC    |      |      |
| E10 | 5.19 BSC    |      |      |
| E11 | 0.10 REF    |      |      |
| e   | 1.20 BSC    |      |      |
| e/2 | 0.60 BSC    |      |      |
| e1  | 8.40 BSC    |      |      |
| K   | 2.43        | 2.53 | 2.63 |
| L   | 1.90        | 2.00 | 2.10 |
| L2  | 0.50        | 0.60 | 0.70 |
| z   | 0.35 REF    |      |      |
| θ   | 0°          | ---  | 12°  |
| aaa | 0.20        |      |      |
| bbb | 0.25        |      |      |
| ccc | 0.20        |      |      |
| ddd | 0.20        |      |      |
| eee | 0.10        |      |      |

### GENERIC MARKING DIAGRAM\*



A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Code  
 XXXX = Specific Device Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

|                         |                            |  |
|-------------------------|----------------------------|--|
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| <b>DESCRIPTION:</b>     | <b>H-PSOF8L 11.68x9.80</b> | <b>PAGE 1 OF 1</b>   |

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