

MOSFET – N-Channel, POWERTRENCH®

60 V, 80 A, 5.6 mΩ

FDB86569-F085

Features

- Typical $R_{DS(on)}$ = 4.4 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- Typical $Q_{g(tot)}$ = 35 nC at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- UIS Capability
- These Device is Pb-Free and is RoHS Compliant
- Qualified to AEC-Q101

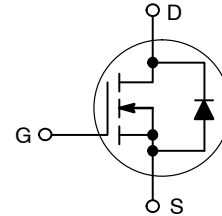
Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

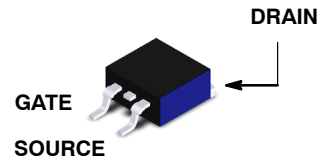


ON Semiconductor®

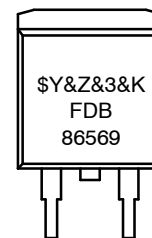
www.onsemi.com



D2PAK-3
CASE 418AJ
FDB SERIES



MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDB86569	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDB86569–F085

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous ($V_{GS} = 10\text{ V}$) (Note 1) $T_C = 25^\circ\text{C}$	80	A
	Pulsed Drain Current $T_C = 25^\circ\text{C}$	See Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	41	mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	94	W
	– Derate Above 25°C	0.63	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 15\ \mu\text{H}$, $I_{AS} = 74\ \text{A}$, $V_{DD} = 60\ \text{V}$ during inductor charging and $V_{DD} = 0\ \text{V}$ during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a $1\ \text{in}^2$ pad of 2oz copper.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB86569	FDB86569–F085	D ² –PAK (TO–263)	330 mm	24 mm	800 Units

FDB86569–F085

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

B _V DSS	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	60			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 60 V, V _{GS} = 0 V, T _J = 25°C			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _C = 175°C (Note 1)			1	mA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS

V _{GS(TH)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	2.8	4.0	V
R _{DS(ON)}	Drain to Source On Resistance	I _D = 80 A, V _{GS} = 10 V, T _J = 25°C		4.4	5.6	mΩ
		I _D = 80 A, V _{GS} = 10 V, T _C = 175°C (Note 1)		8.5	10.8	mΩ

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		2520		pF
C _{oss}	Output Capacitance			690		pF
C _{rss}	Reverse Transfer Capacitance			47		pF
R _g	Gate Resistance	f = 1 MHz		2.0		Ω
Q _{g(tot)}	Total Gate Charge at 10 V	V _{GS} = 0 V to 10 V, V _{DD} = 30 V, I _D = 80 A		35	52	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 V to 2 V, V _{DD} = 30 V, I _D = 80 A		4.8		nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 30 V, I _D = 80 A		14		nC
Q _{gd}	Gate to Drain "Miller" Charge			7.4		nC

RESISTIVE SWITCHING CHARACTERISTICS

t _{ON}	Turn-On Time	V _{DD} = 30 V, I _D = 80 A, V _{GS} = 10 V, R _{GEN} = 6 Ω			53	ns
t _{d(ON)}	Turn-On Delay			15		ns
t _r	Rise Time			20		ns
t _{d(OFF)}	Turn-Off Delay			22		ns
t _f	Fall Time			8		ns
t _{OFF}	Turn-Off Time				45	ns

DRAIN–SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 80 A, V _{GS} = 0 V			1.25	V
		I _{SD} = 40 A, V _{GS} = 0 V			1.2	V
t _{rr}	Reverse Recovery Time	I _F = 80 A, di _{SD} /dt = 100 A/μs, V _{DD} = 48 V		52	68	ns
Q _{RR}	Reverse Recovery Charge			43	65	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

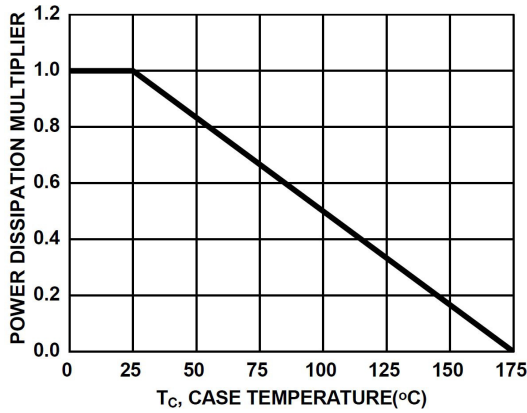


Figure 1. Normalized Power Dissipation vs. Case Temperature

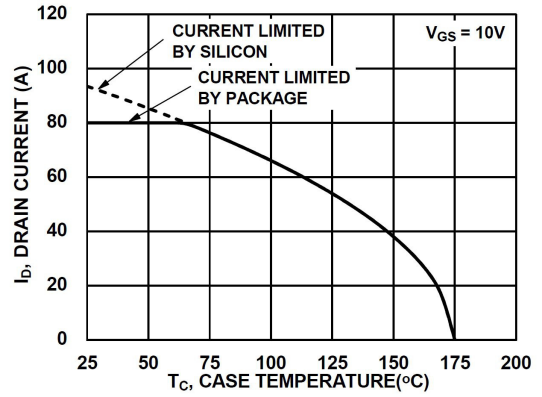


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

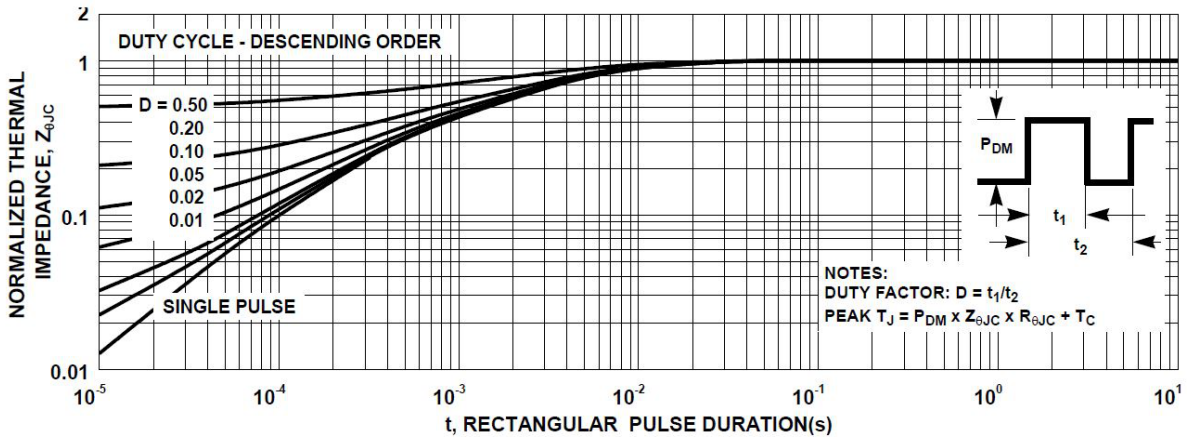


Figure 3. Normalized Maximum Transient Thermal Impedance

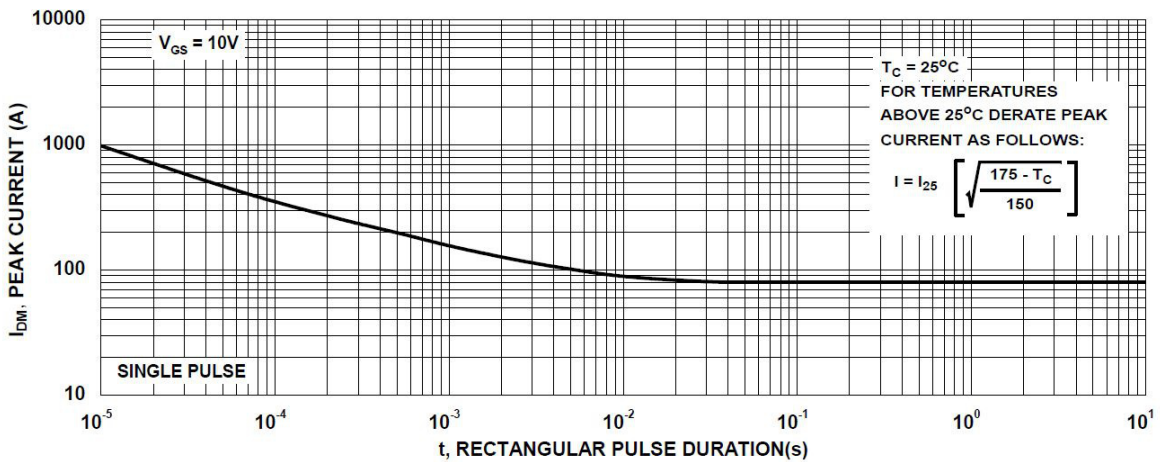


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (Continued)

NOTE: Refer to ON Semiconductor Application Notes [AN-7514](#) and [AN-7515](#)

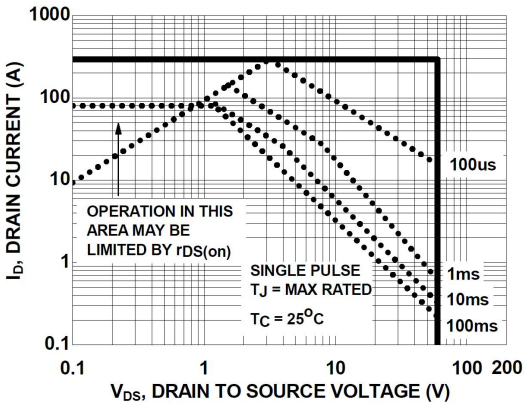


Figure 5. Forward Bias Safe Operating Area

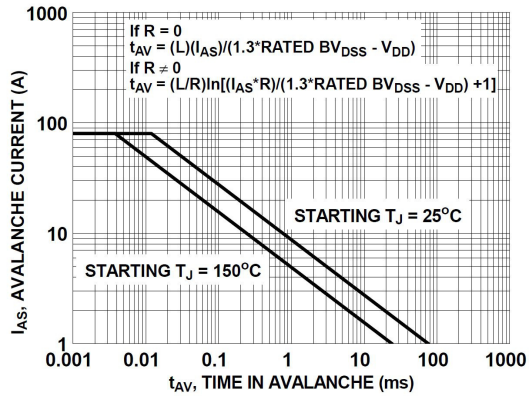


Figure 6. Unclamped Inductive Switching Capability

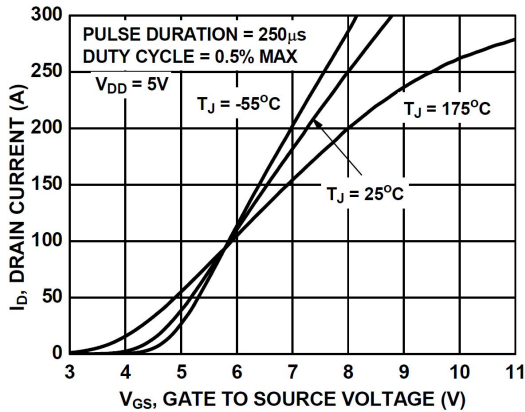


Figure 7. Transfer Characteristics

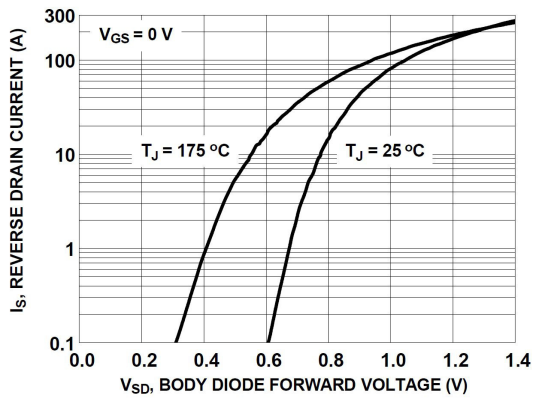


Figure 8. Forward Diode Characteristics

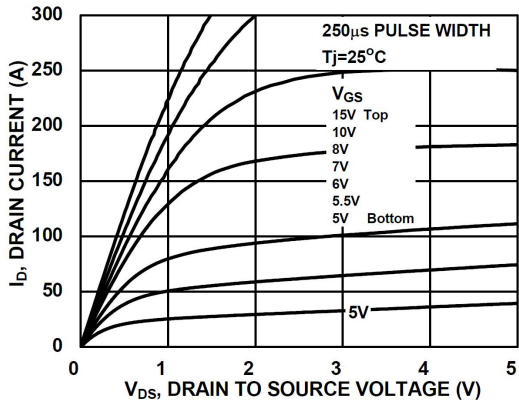


Figure 9. Saturation Characteristics

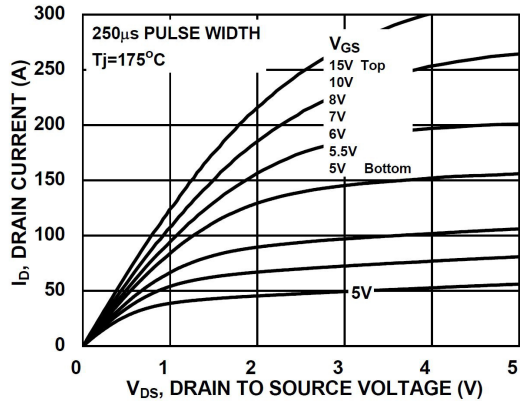


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (Continued)

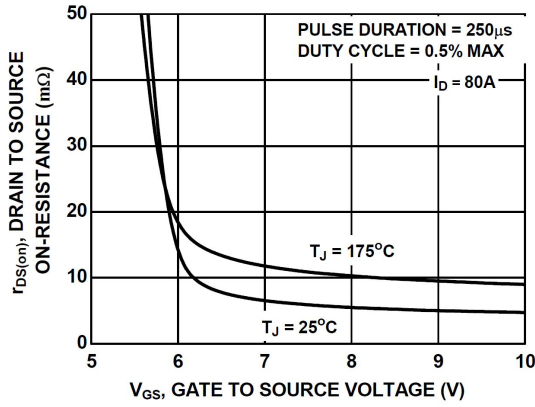


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

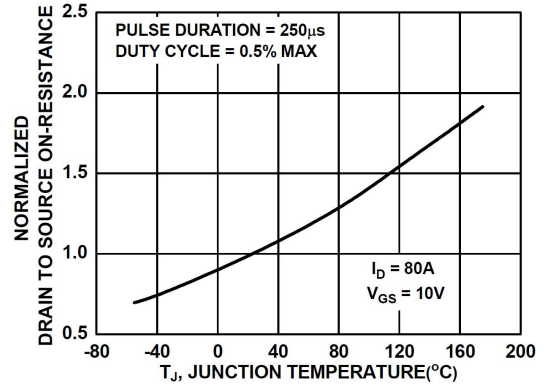


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

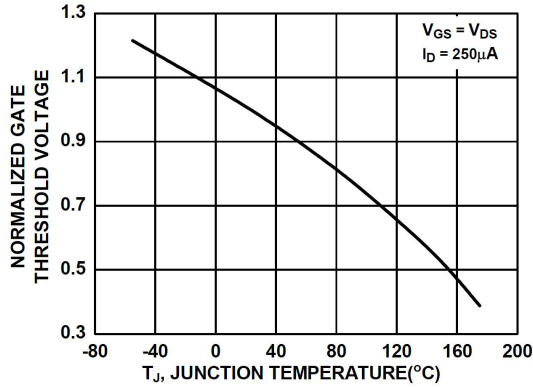


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

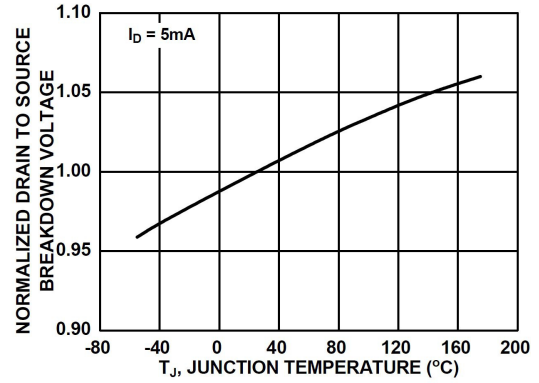


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

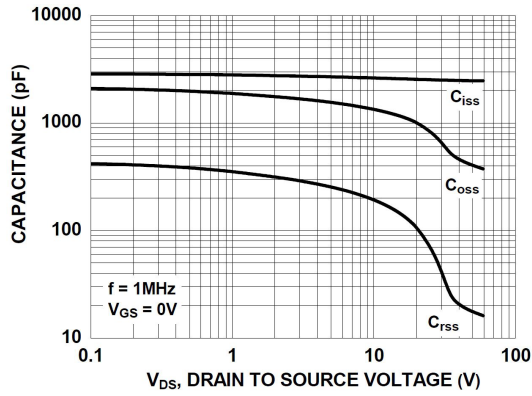


Figure 15. Capacitance vs. Drain to Source Voltage

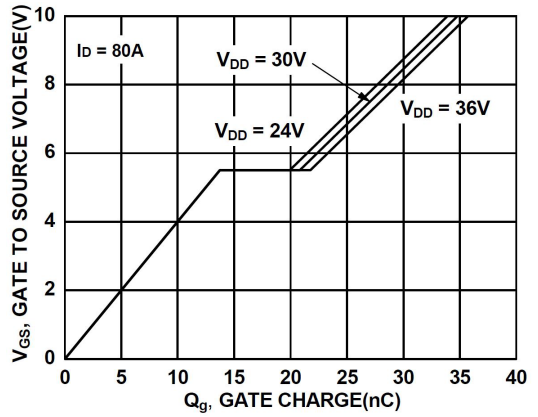


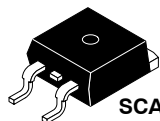
Figure 16. Gate Charge vs. Gate to Source Voltage

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



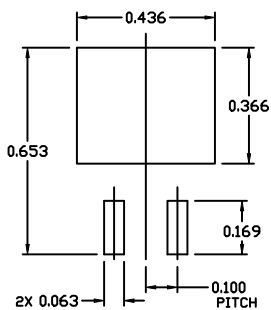
SCALE 1:1

D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

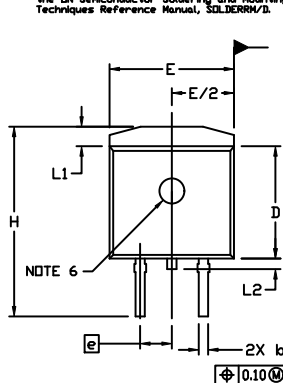
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

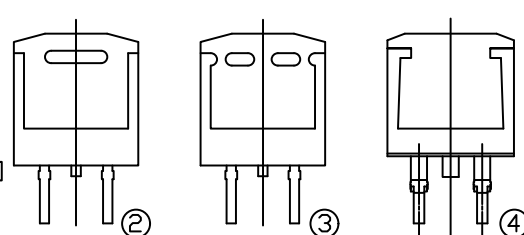
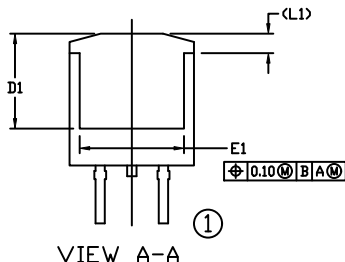
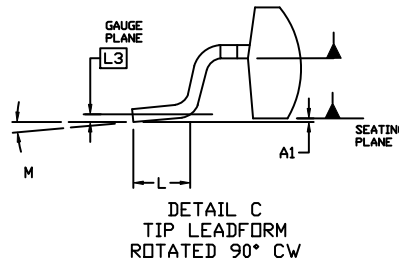
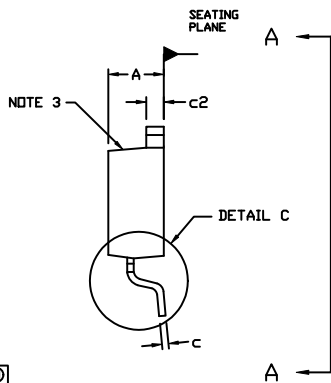
For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



NOTES:

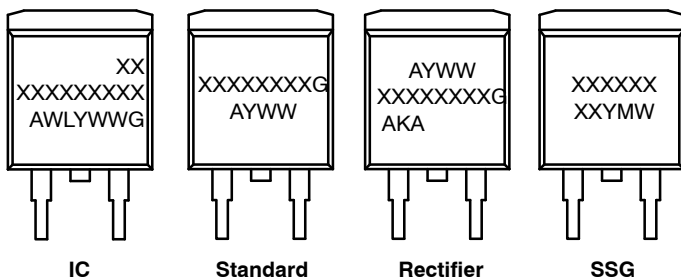
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*



OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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