

FCU900N60Z

MOSFET, N-Channel, SuperFET[®] II

600 V, 4.5 A, 900 mΩ

Description

SuperFET[®] II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

Features

- 675 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 820\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 13\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 48.6\text{ pF}$)
- 100% Avalanche Tested
- ESD Improved Capacity
- RoHS Compliant

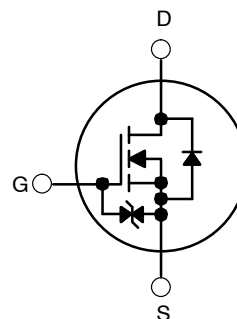
Applications

- LCD/LED/PDP TV and Monitor Lighting
- Solar Inverter
- Charger

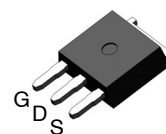


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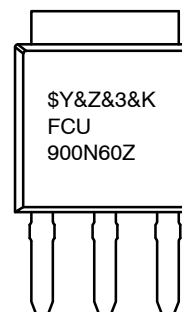


N-Channel



DPAK3
CASE 369AP

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FCU900N60Z = Specific Device Code

ORDERING INFORMATION

Device	Top Mark	Package	Shipping
FCU900N60Z	FCU900N60Z	DPAK3	70 Units/ Tube

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage		600	V
V _{GSS}	Gate to Source Voltage	DC	±20	V
		AC (f > 1 Hz)	±30	
I _D	Drain Current	Continuous (T _C = 25°C)	4.5	A
		Continuous (T _C = 100°C)	2.8	
I _{DM}	Drain Current	Pulsed (Note 1)	13.5	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		47.5	mJ
I _{AR}	Avalanche Current (Note 1)		1	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		0.52	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P _D	Power Dissipation	(T _C = 25°C)	52	W
		Derate above 25°C	0.42	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 1.0 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 2.3 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	2.4	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	100	

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0 V, T _J = 25°C	625	–	–	V
		I _D = 1 mA, V _{GS} = 0 V, T _J = 150°C	675	–	–	
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, referenced to 25°C	–	0.67	–	V/°C
BV _{DS}	Drain to Source Avalanche Breakdown Voltage	V _{GS} = 0 V, I _D = 4.5 V	–	700	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 600 V, T _C = 125°C	–	–	10	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.5	–	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 2.3 A	–	0.82	0.90	Ω
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 2.3 A	–	4.6	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	–	534	710	pF
C _{oss}	Output Capacitance		–	399	530	pF
C _{rss}	Reverse Transfer Capacitance		–	19.7	30	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	–	11.1	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	–	48.6	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 380 V, I _D = 2.3 A, V _{GS} = 10 V (Note 4)	–	13.1	17	nC
Q _{gs}	Gate to Source Gate Charge		–	2.2	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	4.5	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	2.4	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 380 V, I _D = 2.3 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	–	10.9	32	ns
t _r	Turn-On Rise Time		–	5.3	21	ns
t _{d(off)}	Turn-Off Delay Time		–	33.6	77	ns
t _f	Turn-Off Fall Time		–	11.9	34	ns

DRAIN-SOURCE DIODE CHARACTERISTIC

I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	4.5	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	13.5	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 2.3 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 2.3 A, dI _F /dt = 100 A/μs	–	156	–	ns
Q _{rr}	Reverse Recovery Charge		–	1.3	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

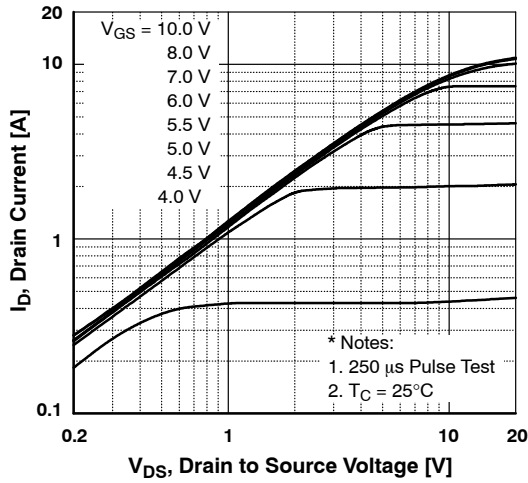


Figure 1. On-Region Characteristics

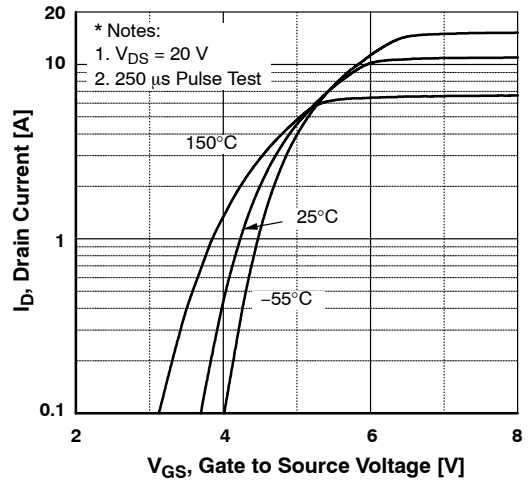


Figure 2. Transfer Characteristics

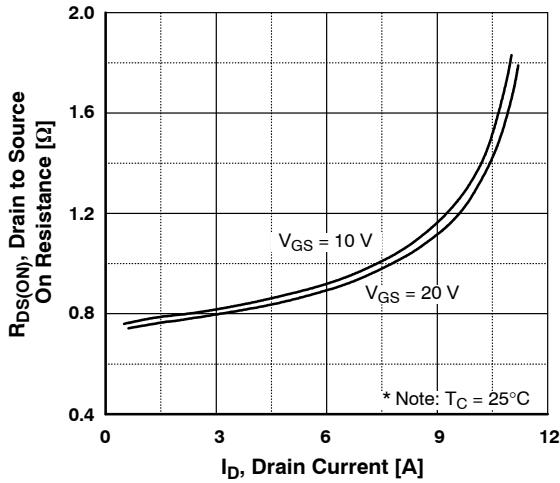


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

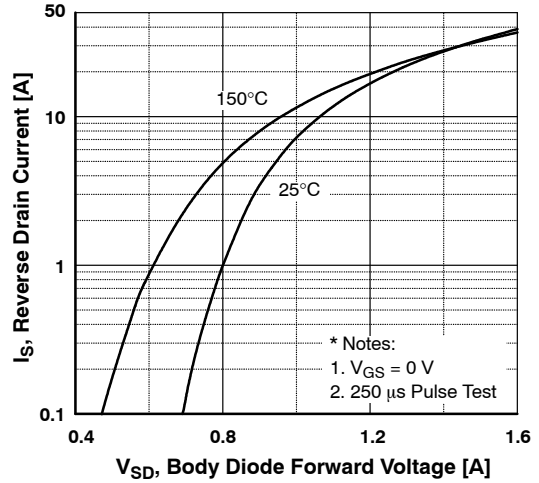


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

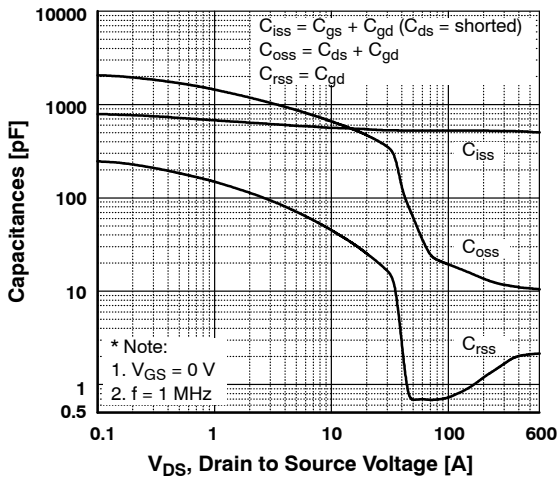


Figure 5. Capacitance Characteristics

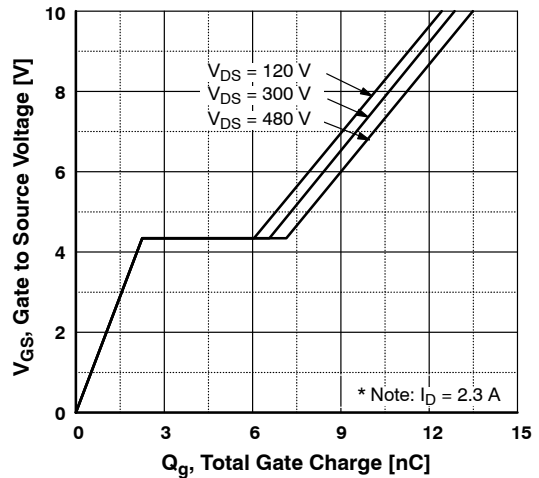


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

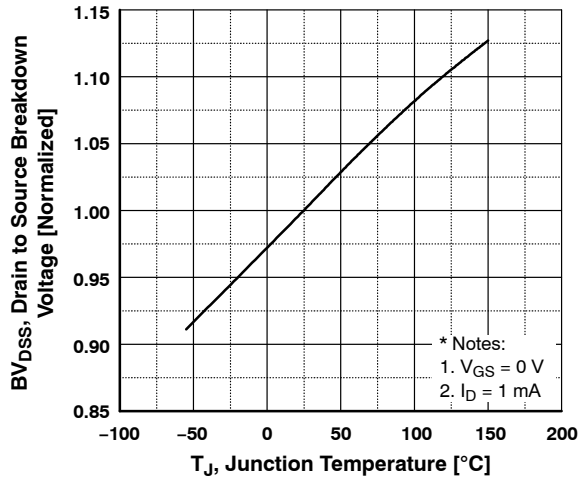


Figure 7. Breakdown Voltage Variation vs. Temperature

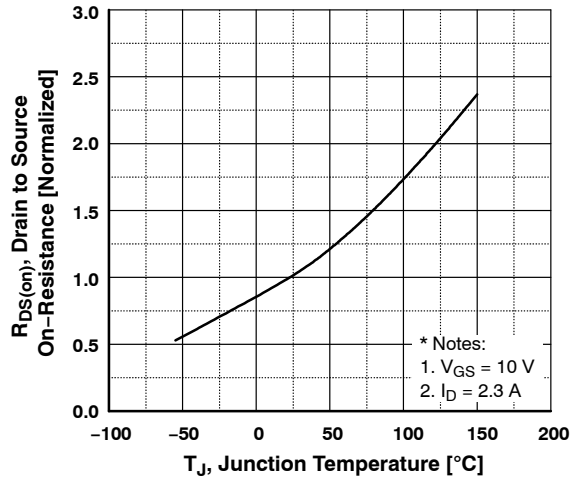


Figure 8. On-Resistance Variation vs. Temperature

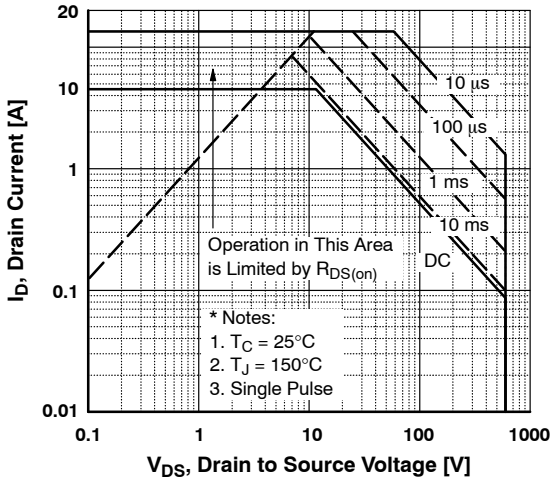


Figure 9. Maximum Safe Operating Area

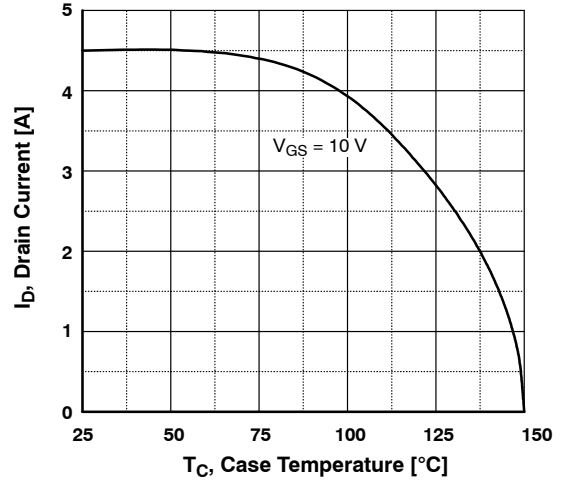


Figure 10. Maximum Drain Current vs. Case Temperature

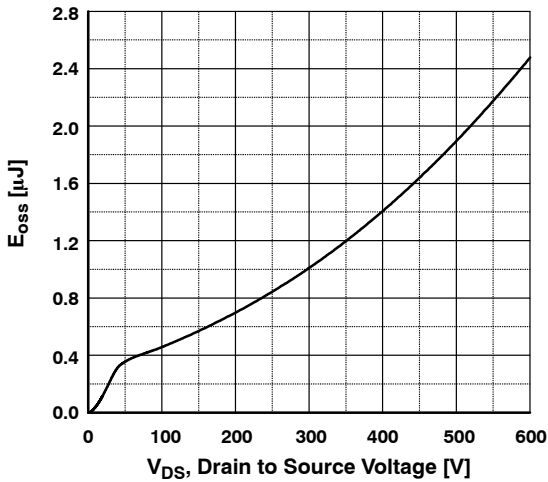


Figure 11. E_{oss} vs. Drain to Source Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

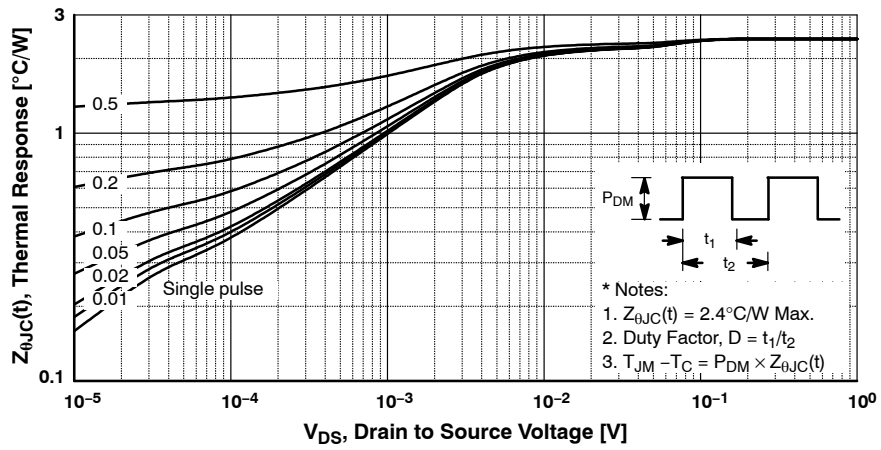


Figure 12. Transient Thermal Response Curve

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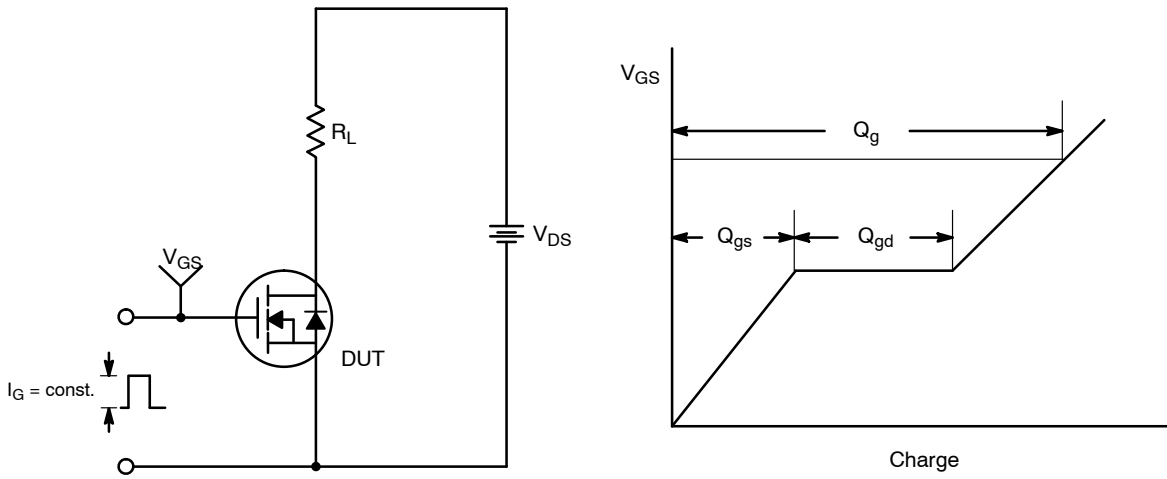


Figure 13. Gate Charge Test Circuit and Waveform

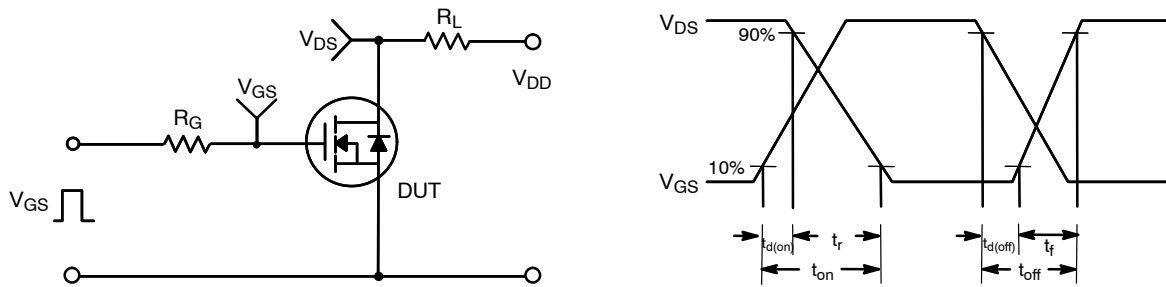


Figure 14. Resistive Switching Test Circuit and Waveforms

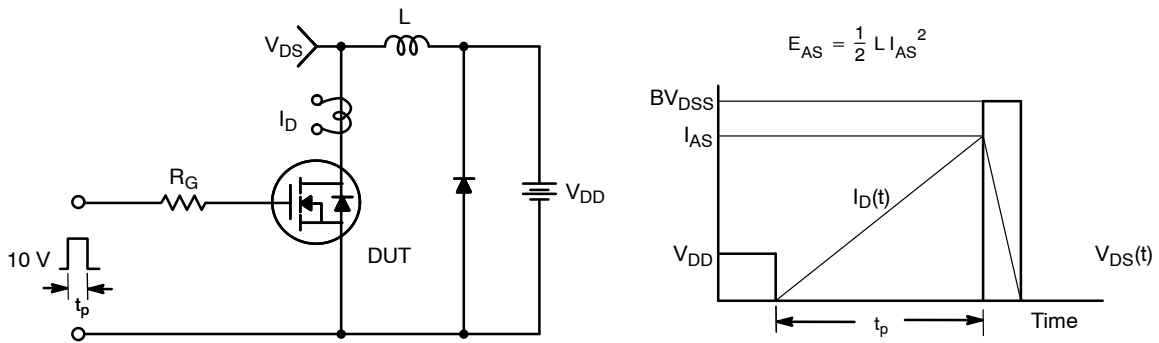


Figure 15. Unclamped Inductive Switching Test Circuit and Waveforms

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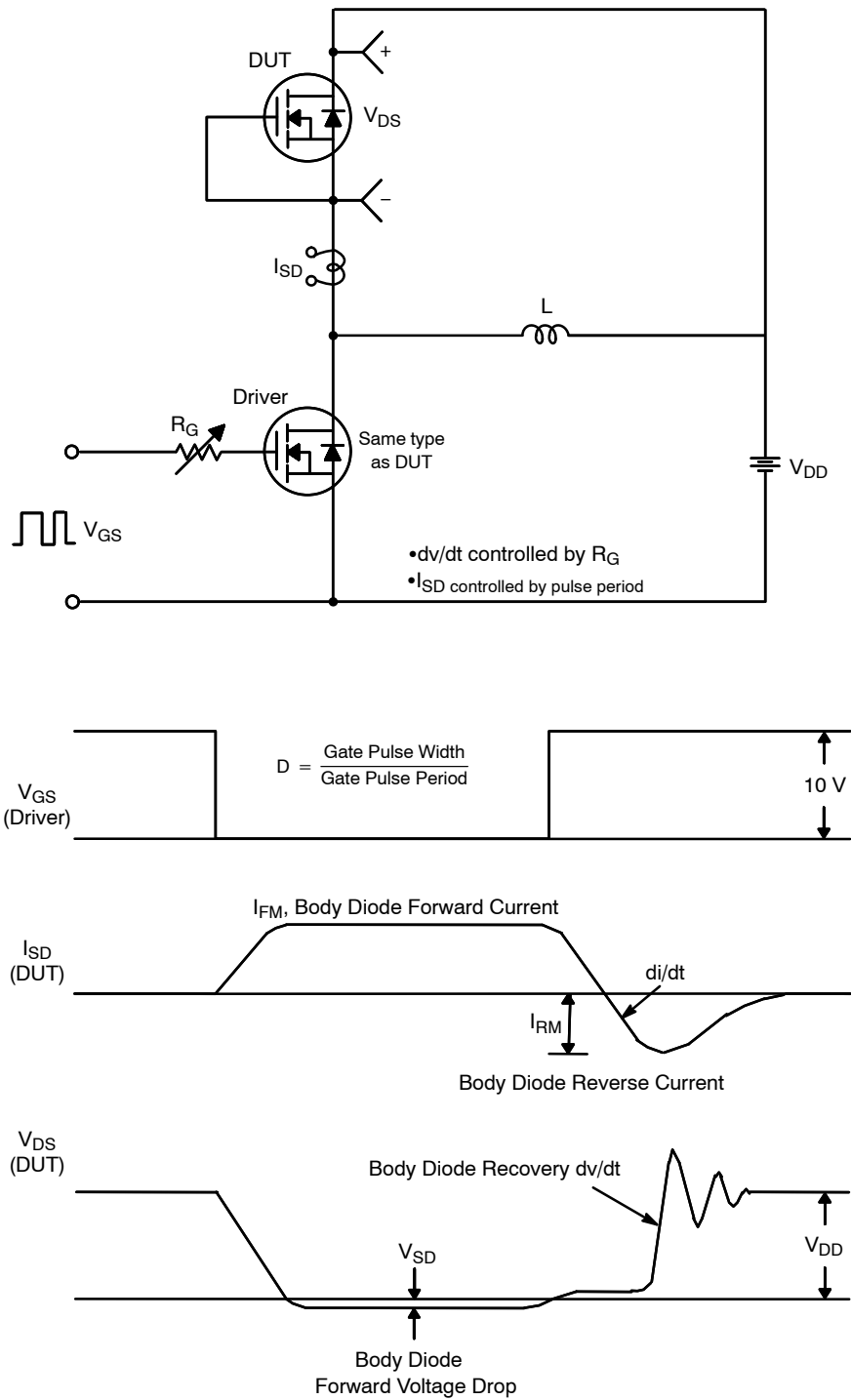


Figure 16. Peak Diode Recovery dv/dt Test Circuit and Waveforms

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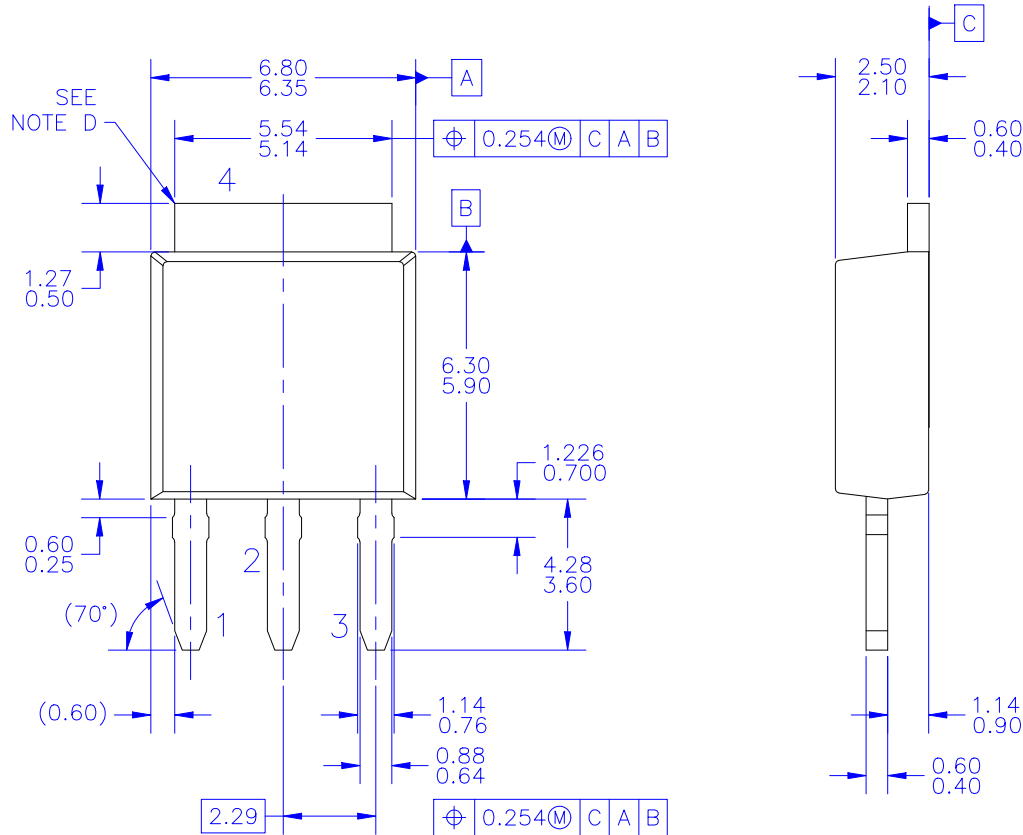
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



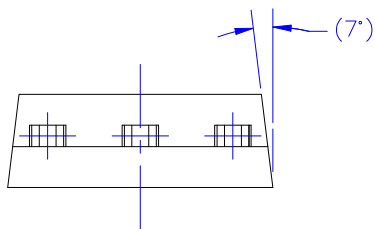
DPAK3 (STRAIGHT LEADS)
CASE 369AP
ISSUE O

DATE 30 SEP 2016



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) PACKAGE BODY REFERENCE: JEDEC, TO-251, ISSUE D, VARIATION AA, DATED JUNE 2002.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.



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